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Utilizing 3D Package Technology for Complex SiP Applications -
Innovative Solutions for System Level Integration and Miniaturization

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Abstract
Hand-held communication and entertainment products continue to dominate the consumer markets worldwide, and with each generation, companies are offering more and more features and/or capability. Even though the actual functionality of the new product offering expands, the customer is expecting each generation to be smaller and lighter that its predecessor. More functionality typically requires additional or more complex electronics and greater memory capacity. Increasing functional capability, however, can adversely impact the products size as well as manufacturing cost. The challenge manufactures face when competing in the world marketplace is to offer a product that will meet all performance and functionality expectations within budget and without increasing product size.

This paper will explores a number of system level applications developed within Tessera's Package Engineering Service Laboratories and examine the results of extensive computer modeling as well as review the data compiled from electrical performance and physical stress testing.

Introduction
The motivation for developing higher density IC packaging continues to be the market, the consumers' expectation that each new generation of products furnish greater functionality, be smaller than its predecessor's and provide higher performance. Increased electronic functionality can be achieved through the development of more complex silicon integration but that route generally requires a great deal of capital resources and time. With the rapid deployment of new products from an ever growing number of competing companies, time-to-market can be the difference between leading and following. For that reason, many manufacturers will rely heavily on more innovative package solutions, solutions for integrating a number of already proven functional elements within a single-package outline. To address functionality and size, a number of companies have already shifted away from simple single-die IC packaging and are adapting various forms of multiple-die 3D packaging. A 3D package is a component that incases multiple devices. The bare die can be grouped into a single package outline or individually packaged and electrically tested before joining together in a vertically configured format. When adapting multiple die configurations, each IC package becomes a fully tested subsystem that can be certified by the supplier before board or module level assembly. To achieve system level integration and miniaturization goals, companies are able to rely on a combination of multiple-die package solutions, high-density substrate methodology and passive component integration technologies. The multiple-die package is actually proving superior to the system-on-chip alternative because it minimizes risk and economically integrates several different but complementary functions. In the case of memory for example, multiples of the same function can be vertically stacked for increased memory density.

Substrate Material Selection and Fabrication Methodology
The material set selected for multiple die substrates must furnish good dielectric characteristics and be able to withstand the relatively high assembly process temperatures needed for the newer generations of lead-free products. The non-reinforced polyimide film dielectric has proved to be excellent for high-performance IC package applications and is often selected for products that must operate in more hazardous environments. IC packaging may require the use of one or two metal layers for die interface. For the single metal layer substrate, the copper is typically applied to the flexible base dielectric as a foil with adhesive. An alternative process casts a polymer dielectric directly onto the copper foil without adhesive. In both single metal material variations, holes and other features are drilled or punched through the composite structure; circuit features are imaged using photo resists and chemically etched to provide the finished circuit pattern.

Two metal flex based substrates can be furnished using adhesives as well but adhesive-less copper. The adhesive-less copper material is preferred, especially for fine-line circuit design. For this application, a seed layer is first applied to the polyimide film consisting of a sputtered 'tie-coat' of nickel, chrome or nickel/copper alloy of approximately 200-300 angstroms thick followed by copper sputtered to ¼ micron. The sputtered copper layer is then electroplated to approximately 2 to 3 microns thick providing a sufficient conductive base for the subsequent electroplating of the circuit conductors. This methodology is referred to as a semi-additive plating, where holes and features are first drilled or punched through the metalized substrate, photo-resist materials are applied over the base-copper, the circuit pattern is then imaged and developed and made ready for the additive copper plating process.

During the electro-plating process, additional copper is 'built-up' onto the exposed circuit pattern and into the connecting via holes. After stripping the resist, the remaining thin base alloy layer remaining on the substrate surface is etched away leaving only the finished copper conductor pattern. The physical elements of the polyimide flex-film are detailed in Table 1.

Table 1 - Flexible Polyimide Film Materials

	Polyimide Film (w/adhesive)	Polyimide Film (adhesiveless)
Glass transition temp.	>270ºC	>270ºC
Oper. temp. range	85-160ºC	105- 200ºC
TCE (ppm/ºC)	13-15	15-15
Dielectric constant	3.5	3.3
Dielectric strength	3-5Kv/25µm	5Kv/25µm
Insulation Resistance	10^3 Ω-cm	10^3 Ω-cm
Modulus (MPa)	2500	4000
Tear resistance	500g	500g
Cu peel strength	1740 N/M	1225 N/M

Data source: IPC-2223

To insulate and protect the polyimide-based substrate after circuit fabrication, permanent coatings or films are generally applied over the circuit conductors. The openings in the coating provide access to the copper features designated for component attachment during the assembly process. Photo-imagable materials have been developed for surface insulation as well, available in dry film and wet applied variations, the photo-imaged material requires no pre-processing or hard tooling (other than photo-tools).

Multiple-Die Package Technology

The following examples will demonstrate the clear advantage of the flexible substrate for multiple die IC packaging. The µZ®-Folded package technology typical of the three die, mixed memory package shown in Figure 1, for example, enables a number of die (even different size die) to be attached in series onto a common multiple site substrate.

To retain the folded format, a thin polymer film is applied to the top surface of one row of die. The extended area is then folded over and repeated for the remaining extension and secured in a clamp fixture to complete the bonding process. Following a cure cycle, the solder ball contacts are applied, the folded strip is cleaned and unit parts are finally singulated and made ready for testing. After testing, the finished package is ready for board level assembly.

The enabling technology for the multiple-die foldable package is the flexible film substrate. The base material shown in Figure 2 uses a 25 micron thick polyimide film having copper-foil on two sides. The multiple-die package assembly process begins with die attach, lead termination and encapsulation. The encapsulation material has been formulated so that after curing it will allow a controlled movement of the 'S' shaped lead during thermal excursions to buffer the physical strain of the solder joint at the board level interface. Although the lead-bond methodology was originally developed for single die packaging, it has also proved to be successful for a broad number of multiple die package applications needing a small outline and low profile.

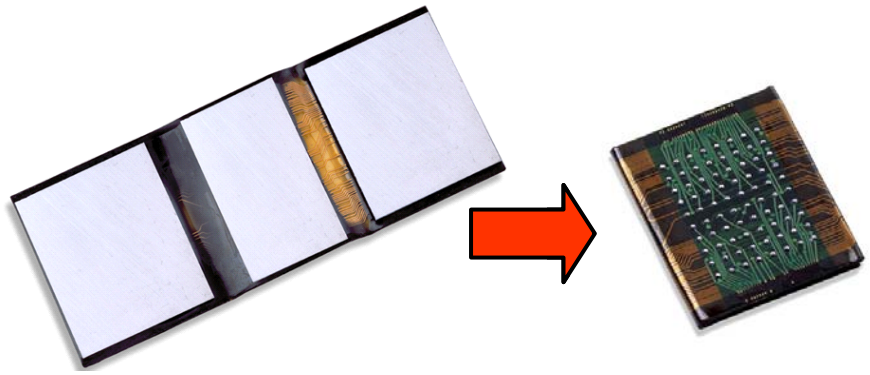

Figure 1 - The Three Die µZ®-Folded Package Includes Two Flash Die and One SRAM Die, when Folded, Furnishes a Package Outline that is only Slightly Larger than the Largest Die in the Set

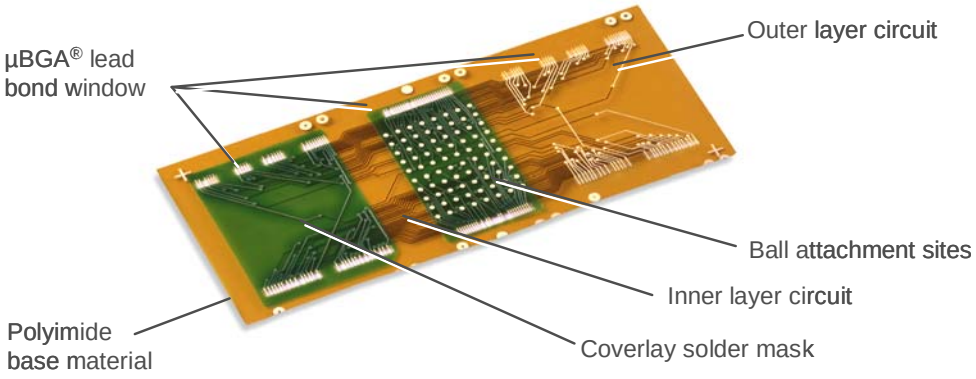

Figure 2 - The Three Die Substrate Adapts 25 Micron Wide Circuit Conductors on Two Sides, Interconnected with Laser Ablated and Plated Micro-Vias

The technology provides a very close, low-profile coupling between die and substrate and adapts one of the most reliable package interconnect methods available, the lead-bond process. This methodology minimizes both signal inductance and resistance because the lead is an integral part of the package substrate.

There are a number of multiple function package applications that will require the sequential assembly of separately processed die. A case in point is the package shown in Figure 3 that was developed as a base unit, providing a mounting site on its top surface for additional single or multiple die packages with complimentary but very different functions. Microprocessors and memory, for example, have very different wafer process flows and functionality. Developing an electrical test for a single package that combines both logic and memory technologies is difficult, but, by using a combination of stackable pre-tested ICs packages there are never any compromises made that would impact their subsequent board level functionality.

The fold-over base section substrate is designed to accommodate a single die interface to an array matrix for PCB mounting and, by extending the base material from one edge of the package; a second array-mounting site is provided. The extension will eventually be folded over and onto the die encapsulation to accommodate a second package. For this application the die is mounted to the substrate with its active surface facing away from the substrate surface (face-up). The substrate is designed so that the bond-wire interface from the die is as direct as possible.

The finished stacked package configuration can be performed by the supplier or at the board level assembly stage. If the decision is to join the two sections at the board-level assembly, the base fold-over package can be placed onto the board and additional packaged devices placed sequentially onto the mating contact matrix of the base for simultaneous reflow soldering.

The actual interface between the base die and the package attachment site on the top of the finished package requires a substrate with two circuit layers to provide for the higher wiring density. The two metal layer fabrication process used for the package substrate is very similar to that described for the folded package, enabling very narrow circuit routing features. The base material selected for the fold-over base package is also a 25 micron thick polyimide film having copper deposition on two sides. Although both sides of the substrate are utilized for interconnect, the circuit path between die and the stacked package mounting site is routed only one side of what will become the inside surface of the flex material. With the exception of the ‘fold zone’, the circuit pattern remaining on the outer surface is coated with a photo-imaged dielectric mask material.

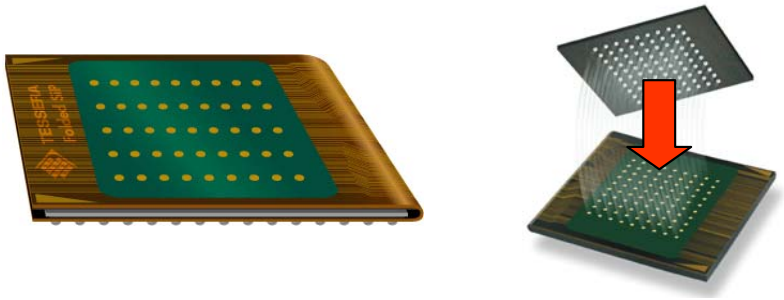

Figure 3 - The Fold-Over Package Technology Provides a Land Pattern on its Top Surface to Accommodate the Stacking of Additional Packaged IC Devices

Prior to die attachment and wire-bonding operations, an adhesive pattern is applied to the substrate surface. This adhesive can be dispensed as a liquid, pattern printed or, pre-applied to the substrate as a die cut dry film composite. The silicon die is then aligned and placed onto the prepared site followed by a short cure cycle. After curing the die-attach material the substrate carrier is transferred to the wire-bond system to complete the electrical interface between die and substrate. Limiting the wire loop height is vital to maintaining a lower package profile. To accomplish this, a combination of wedge and ball bonding methods are employed. A relatively low (75 micron) loop height of the wire must be maintained in order to provide the thin encapsulated package height requirement established.

The final phase of the encapsulated base package assembly is performed in a sequence that first applies an adhesive composition to the top surface of the molding compound followed by precise mechanical folding and clamping operation. When the bonding material completes its curing cycle, the finished base package is ready for ball contact attachment, singulation and electrical testing. Singulation of the packaged devices from the strip is also very precise. A precision saw developed for wafer level processing has proved efficient for cutting through the substrate and mold material, however, laser ablation is also a viable method for package singulation. Both methods require minimal dedicated tooling and each can be programmed to accommodate several package outline variations.

Building the package in stackable sections has two benefits. It allows the user to select from multiple memory variations (different memory functions, data rate and so on) as well as accommodating secondary sources of supply. Whether or not to join one package to the other before or during the board level assembly process is a decision that may be influenced by the requirement for in-process configuration flexibility. For example, the base fold-over package can be furnished by vendor ‘A’ while the memory sections of the stack are supplied by vendor ‘B’, ‘C’ or ‘D’.

Ball Stack Packaging

The ball-stack methodology has proved to be one of the most practical solutions for packaging several die within a single package footprint. The final 3D configuration is accomplished by vertically joining two or more pre-assembled and pre-tested single package units into a low-profile multi-tiered Ball Stack package assembly (see Figure 4).

Figure 4 - The Stacking of Pre-packaged and Tested Die Provides a Low Cost and Low Risk 3D Solution for Enabling Higher Component Density

The stacked packaged die methodology has proved to have less risk for memory because the individual package units can be pre-tested at high temperature, sorted and graded before conversion into the final vertical format. This methodology has also proved ideal for a number of high speed SDRAM applications. By mounting the two-level ball stack packages onto single DIMM or SO-DIMM substrate it will furnish double the memory capacity and saves the expense associated with additional circuit board modules, the connectors needed for interface and minimizes the area required on the host board.

In preparation for package stacking, individual package sections are first assembled using a single or two metal layer, non reinforced polyimide film substrate. To accommodate efficient package assembly processing, several package sites are uniformly arranged onto a common rectangular strip format. One of the more mature processes for interconnecting the semiconductor die and package substrate is wire-bonding. The process can be applied when the die is mounted ‘face-up’, away from the package substrate surface; however, wire-bond can also be applied to the die when mounted ‘face-down’ against the package substrate. While most die are designed with the bond pads at the outer perimeter, the newer generations of high-performance memory have bond sites positioned though the center. To accommodate face-down wire-bond termination for the center-bond memory die, a slot is provided in the substrate to access the bond pads on the die. Following die attach, wire-bond and encapsulation, the ball contacts are attached to the bottom surface of the substrate and finally separated into single package units. Electrical testing may be performed before or following package singulation.

3D Memory Package Performance Criteria

Until recently, the component packaging industry did not directly concern itself about system level performance. This has increasingly becoming an issue and is evidenced by the restriction on the number of DIMM assemblies that can be designed onto the motherboard due to performance reasons. The first aspect of performance analysis is to characterize the performance of a single die Fine-pitch BGA (FBGA) package as a reference for comparing the Ball Stack package performance. For this analysis, a DDR333 device in a single die FBGA package was used having a maximum inductance value of 3.188 nH and a value of capacitance 0.287 pF,. For an equivalent TSOP package, the values (furnished by a prominent supplier) for a 512 Mb, DDR333 is 5.69 nH and 1.14 pF, respectively. Delay was calculated using the approximate relationship given in the following formula:

$$Delay = \sqrt{L_{package} \times C_{package}}$$

The delay for the FBGA and TSOP packages was found to be 30.2 ps and 80.5 ps, respectively, overwhelmingly confirming the theory that the FBGA package offers better performance when compared to the commercial TSOP lead-frame package. The whole system performance, however, needs to be kept in view and any comparison should be done at the equivalent system level; one composed of single device packages and the other with 3D packages.

Substrate Design

The substrate design example shown in Figure 5 is for a 512Mb DDR SDRAM device operating at a frequency of 167 MHz and 333 MHz data rate. As can be seen from the illustration, a provision was made for optional mechanical/thermal solder balls in the central area of the package. In addition, a wire-bond select option was provided in this design to accommodate unique control line termination for each layer in the stack.

To support the theory that stacking of the individual package elements onto a module would meet performance expectations, a computational analysis of the ball stack package was conducted by the engineering team with different number of layers in the stack. The ball-stacked package was further analyzed with a single package layer to compare the effect of routing the I/O to the periphery of the die and with two package layers to study the effect of stacking. A commercial electro-magnetic field solver made by Ansoft called Spicelink was used for this purpose. This software uses ‘finite element’ method for inductance and resistance and ‘boundary element’ method for capacitance.

To simulate the full package, all four quarters were modeled with sufficient overlap to minimize any edge effects introduced due to sectioning the package into quarters. This model is for a 2-stack package (see Figure 6) and all the materials are assumed to be lossless (tan δ = 0). The PCB ground plane model is based on the JEDEC standard.

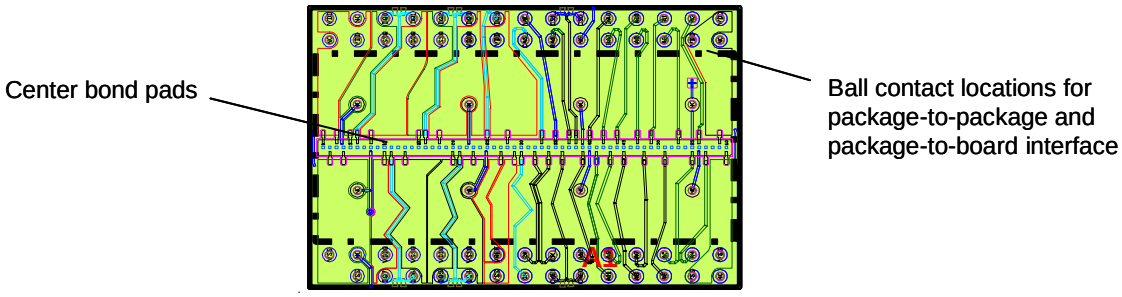

Figure 5 - The Substrate Designed for the Ball Stack Package for a Center-Bond Pad DDR Memory Die

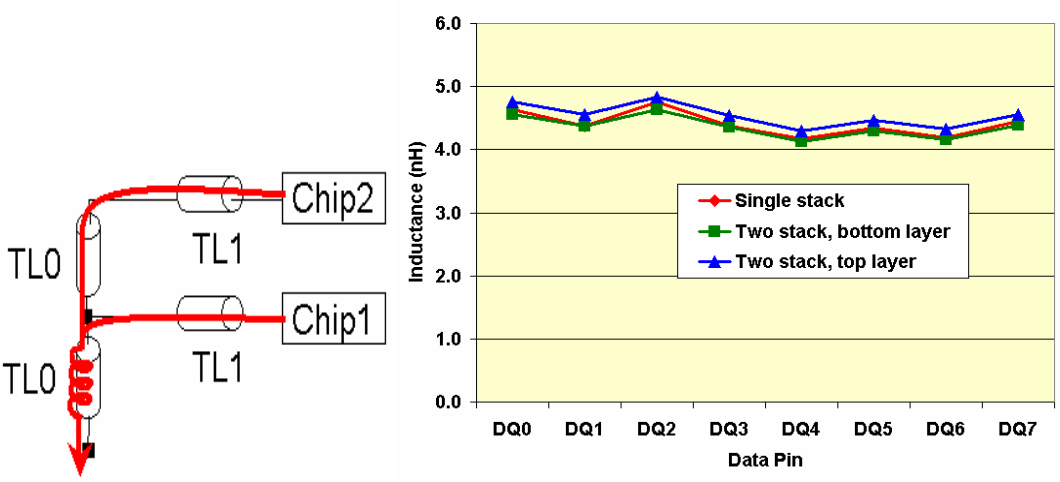

Figure 6 - The Basic Inductance Circuit Model for Two Layer Ball Stack Package and the Graph Developed for Comparing Inductance Values for Eight Data Pins

The inductance plot shown in the figure is based on a quarter-model. The data given compares a single package layer to a two layer ball stack package. The bottom layer and the top layer of the two-stack package are plotted separately. The dielectric materials such as the die and substrate were not included in this model as they do not affect the inductance and resistance values. The electrical parasitics were evaluated for all the contacts of the package. The inductance for each layer in the design is essentially the same and the inductance values are consistent, ranging from 4.0 nH to 5.0 nH. As noted, the lead-frame TSOP package in contrast has an inductance range above 5.6 nH. The two layer stacked TSOP package inductance is estimated at 10 nH, well above the range shown for the Ball Stack package. When the analysis was extended to four-stack package the maximum partial inductance increased by only 10%.

The capacitance model shown in Figure 7 is also a quarter-model because the full model was too big to run in a reasonable amount of time. The capacitance values shown is the total loading capacitance experienced by the I/O and as there are two package layers in two-layer ball stack package compared to the single die package, the capacitance increases significantly. The capacitance increase from single layer package to a two layer stack package is about 80%.

The same trends were seen for address and control I/O and are not plotted here. The maximum delay for a single stack and two stack packages were found to be 53.5 ps and 53.2 ps, respectively.

The analysis for capacitance was extended to a four layer ball stack package exhibiting a maximum total capacitance increase of 86%. The delay was calculated and found to be 75.5 ps. Even the four layer stack package compares favorably with a current TSOP package in terms of electrical parasitics and delay values.

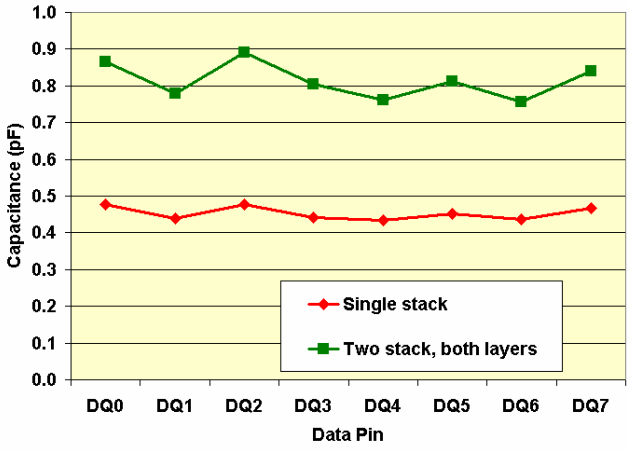

Figure 7 - Comparing Capacitance Values for the Data Pins

Thermal Performance

Thermal management of 3D ball stack packages is an extremely important area of study to ensure viability and use for a variety of environmental applications. The thermal analysis of the Ball Stack package was carried out using FLOTHERM®, a commercially available Computational Fluid Dynamics (CFD)-based solver. For this study, a four-layer stack package was mounted onto a four circuit layer JEDEC standard DIMM board with an estimated 20% of the copper conductor material on the boards outer surface. The material properties of the polyimide package substrate were standard with the die-attach pad having thermal conductivity values of 0.2 W/mK each. Assuming ambient conditions of 40^0C and 0 m/s airflow (still air test), various power distribution cases were analyzed (see Table 2).

Table 2 - Power Distribution (W) in the 4-Die Stack

	Case 1	Case 2	Case 3
Die 4 (top)	**0**	**0.25**	**1**
Die 3	**0**	**0.25**	**0**
Die 2	**0**	**0.25**	**0**
Die 1 (bottom)	**1**	**0.25**	**0**

The distribution was chosen to simulate a total of 1 Watt power dissipation by the ball stacked package. Starting with the layer closest to the PCB, layers are numbered from 1 to 4.

The junction temperature (T_j) for each die is plotted for these 3 cases. The results show that the junction temperature does not vary much for different power distributions in the four die variation as long as the total power is the same (see Figure 8).

This allows for defining a package resistance (Θ_{ja}) value based on an average or the highest T_j value. For these cases the highest Θ_{ja} value is 19.5^0C/W based on average T_j and 20.7^0C/W based on maximum T_j.

As simulated, the JEDEC test method focuses on only a single package unit. In actual system environments, the package performance will be affected by the number of devices present on the same board, the ambient temperature and the airflow around it. For this purpose, a DIMM assembly with eighteen, two layer Ball Stack packages was used. This assembly, in turn, was modeled as if it was mounted onto a typical personal computer motherboard.

As mentioned above, for still air (0 m/s), the Θ_{ja} is approximately 20^0C/W. The analysis was repeated for air velocities of 1, 2 and 3 m/s. The Θ_{ja} decreased significantly from 0 to 1 m/s and drops by a small amount after that. Furthermore, an air velocity of 1m/s yields a Θ_{ja} of 11.2^0C/W, and higher air velocity does not reduce it significantly. The resulting affect of airflow velocity on the ball stack package is shown in Figure 9.

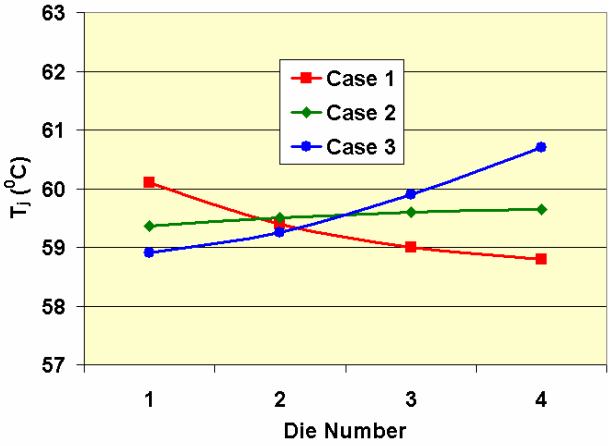

Figure 8 - The Plot Illustrates the Variance of the Junction Temperature (T_j) of the Die within the Four Die Ball Stack Package

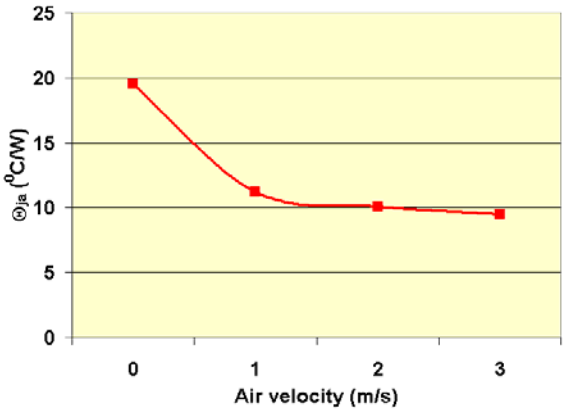

Figure 9 - Package Thermal Resistance as a Function of the Air Velocity

The power dissipation levels used were typical of a standard motherboard. The socket retaining DIMM assembly to the motherboard was assumed to be isotropic with thermal conductivity of 15 W/mK. The ambient temperature was taken as 40ºC and the board was simulated under still air (natural convection) conditions. Under normal operations, both die in the two-layer stack package dissipate 0.34 W (active) and 0.1 W (standby) for a total power of 0.44 W.

The analysis shows that airflow for the stacked DDR memory may be essential for proper operation of the ball stack system. Under the above conditions, the maximum die temperature was found to be 102ºC under still air conditions and 82ºC when airflow of 1 m/s was applied. When the number of layers in the stack is increased to 4 and beyond, it may be essential to use more advanced cooling techniques, such as heat pipes and liquid cooling.

Reliability Qualification Testing

In order to achieve full confidence in the integrity of the ball stacked components, a number of different tests may be employed. Although basic component-level testing is a necessity, a practical board-level assembly test method is essential because it can give the end user the opportunity to evaluate both performance and reliability, assisting suppliers and users in qualifying components for a broad range of environmental applications.

The IPC-9701 specification, for example, allows the user to choose from a number of conditions to meet the specific product requirement for board-level testing (see Table 3). The thermal cycle test methods defined in the document establish specific conditions to evaluate product reliability. The test condition and number of thermal cycles required for qualification, however, is product-dependent and most often defined by the products developer.

Table 3 - IPC-9701 Defined Environmental Test Conditions

Five Test Cycle Conditions	Number of Thermal Cycle Requirement
TC1 0 – 100°C	NTC-A 200 cycles
TC2 -25 – 100°C	NTC-B 500 cycles
TC3 -40 – 125°C	NTC-C 1000 cycles
TC4 -55 – 125°C	NTC-D 3000 cycles
TC5 -55 – 100°C	NTC-E 6000 cycles

The requirement for the test platform (PCB) is not specifically defined in the IPC specification, but users are advised to develop a test vehicle that closely emulates the physical features of the actual product (size, thickness and number of circuit layers).

Testing Parameters Set for the Ball Stack Package

In establishing the test parameters for the Ball Stack package, Tessera worked closely with a prominent OEM to review the industry-recognized test methodology and agreed on testing of the package using both JEDEC and IPC standards. JEDEC standard component preparation included Level 2 or Level 1 preconditioning with a 24 hour bake at 125°C, 168 hrs at 85°C and 60%/85% relative humidity, followed by three exposures to temperatures experienced in reflow soldering.

Temperature 'shock-test' cycling established for this program was based on the IPC-9701, Test Condition 3-C, subjecting the sample assemblies from a low of -40°C and a high of +125°C for 1000 cycles. Table 4 illustrates the Phase 1 test results for the two-layer and four-layer Ball Stack package.

All the sample assembly configurations prepared for the first phase of thermal cycle testing successfully completed the basic 1000 thermal cycles without electrical failure. It should be noted that none of the parts tested were mounted to the substrate using under-fill or other materials for physical reinforcement. The assemblies using eutectic solder balls and eutectic solder for device attachment had no recorded failures; however, a single failure did occur on one device during the drop test for one of the Pb-free solder ball assemblies. Recent research has documented the sub-optimal nature of some Pb-free alloys for drop tests and the failure recorded for the single lead-free package unit may be attributed to incompatible material properties of the ball contact and solder alloys used.

Although physical failures at some point are due to 'wear-out' within the package structure, stress occurring at the board attachment layer may be a result of the strain transferred into the package structure. In order to assess the impact of slight variations in land size (ball contact sites) on reliability, two ball attachment site diameters were prepared on DIMM configured PCB test vehicles, 360 µm and 400 µm. After review of the land pattern variation test results it was determined that a larger solder ball attachment site (land) size significantly impacts solder joint reliability. This may be due in part because the larger land diameter significantly enhances the solder printing process uniformity. Solder paste transfer and overall print uniformity is better controlled when the stencil aperture size can be maximized.

Table 4 - Phase 1 Thermal Shock-Test of Two-Layer and Four-Layer Ball Stack Packages

Package Stack	2 layer	2 layer	4 layer
Sample Size	30	32	27
Contact Alloy	Sn/Ag/Cu	Sn/Pb	Sn/Pb
Temp. Range	- 40/+125ºC	- 40/+125ºC	- 40/+125ºC
Temp. Cycles	1000	1000	1000
Failures	0	0	0

Lead-Free Soldering

During the Ball Stack package development program a number of adjustments were made in the substrate design and package assembly process to improve solder joint reliability. In preparation for the second phase of the program, three different stacked package profiles were developed; two, four and eight layers. The Phase 2 test for the 2 layer ball stack package with lead-free alloy solder balls resulted in no failures through 1000 cycles of thermal-shock stress testing (see Table 5).

Although the basic 1000 cycle thermal-shock test goal was reached on this sample, the engineers allowed the thermal cycling to continue to the eventual 'wear-out' point as illustrated in the Weibull Plot shown in Figure 10.

Table 5 - Phase 2 Thermal Shock Test Results for the 2-layer Ball Stack Package using Pb-free Solder Alloy[4]

Package Stack	2 layer
Sample Size	31
Alloy	Sn/Ag/Cu
Temp. Range	- 40/+125ºC
Temp. Cycles	1000
Failures	0

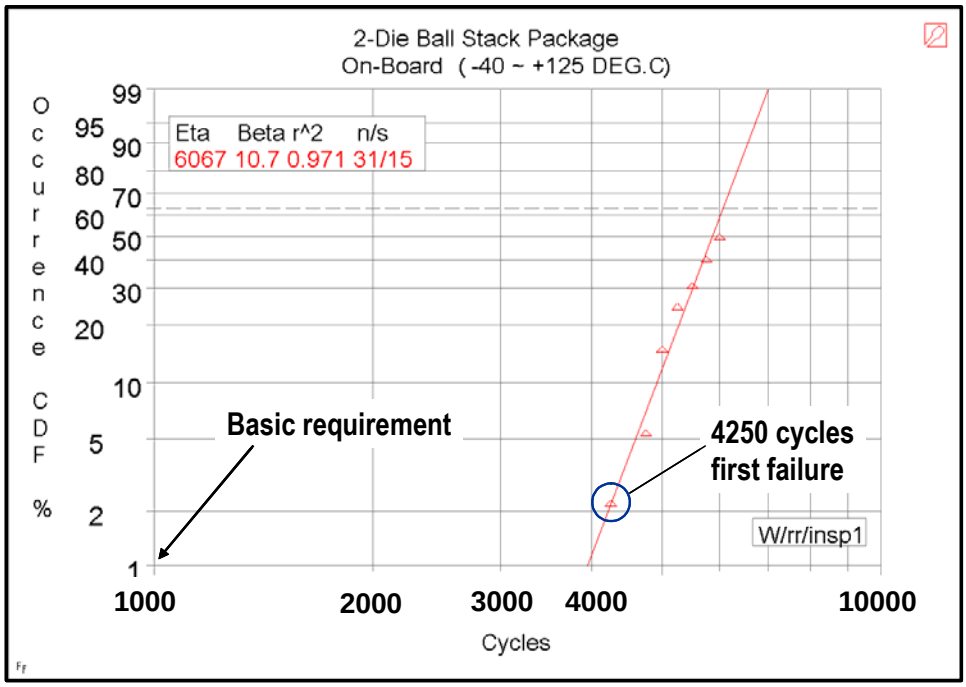

Figure 10 - Weibull Plot for the Lead-Free Two Layer Ball Stack Package Recorded the First Failure in the Package Structure at 4250, Well Beyond the Basic 1000 Cycle Target

A growing number of consumer-destined electronic products will likely use lead-free alloy compositions, however, a significant number of manufacturers for domestic high-end commercial, aeronautic and industrial electronics will continue to specify lead-bearing solders. In further evaluation and comparison of the ball stack package, a sampling of 2-, 4- and 8-layer packages were developed using eutectic solder balls and attachment alloy.

The Phase 3 thermal-shock test results for packages furnished with lead-bearing eutectic solder contacts were consistent with the results of the previous phases of testing; no failures through 1000 cycles of -40ºC to +125ºC (see Table 6).

Parallel testing of the lead-bearing solder assemblies with the lead-free samples exhibited consistent results. This is due in part to a number of improvements in the package design and the physical property of the base materials used in its construction. The physical characteristics of the Ball Stack package are not unlike a single die mature µBGA package technology. For example, the Ball Stack package includes a compliant material structure that compensates for the typical stress factors experienced during thermal excursions of the product use.

Table 6 - Phase 3 Thermal Shock Test Results for 2-, 4- and 8-Layer Ball Stack Packages Using Sn/Pb Solder Alloy[5]

Package Stack	2 layer	4 layer	8 layer
Sample Size	32	26	32
Contact Alloy	Sn/Pb	Sn/Pb	Sn/Pb
Temp. Range	- 40/+125ºC	- 40/+125ºC	- 40/+125ºC
Temp. Cycles	1000	1000	1000
Failures	0	0	0

Summary and Conclusion

Although this paper illustrates a number of practical package solutions for multiple die, there are still challenges that need to be addressed. Many of these involve logistical and business issues that some in the industry are already solving. These include: reliability improvement strategies, better design and analysis capabilities, lower cost of design, system test and access to known (fully tested) good die (KGD). To obtain packaged part die quality and reliability, some sort of electrical testing must be done on the bare die prior to package level assembly. ASIC, simple logic circuits, some processors and linear circuits, at some point, tend to stabilize but testing is the only way to guarantee quality and reliability. The multiple die packages shown allow package level testing and have already proved to be a practical solution for system level integration and miniaturization. In the future, it may be practical to combine both SoC and 3D packaging to achieve specific economical goals. Another issue is the acknowledgement and respect of the developing companies' innovative intellectual property (IP) and the need for improved cooperation among the package manufacturers, semiconductor device suppliers, and the systems companies.

In regard to package reliability, both eutectic and lead-free solders used for the µZ package families have shown positive results, however, during the temperature cycling of Sn/Pb eutectic alloy, the initially fine microstructure coarsens. This means that the area of tin and lead-rich phases become larger. The load is less evenly distributed in a coarse two-phase structure, and there are higher stress concentration points. Eventually this can result in a much weaker response to fatigue loading than with the non-coarsened small grain structure. Comparing the micro structure of eutectic Sn/Pb, most of tin-based lead-free alloys can be considered a single-phase structure and exhibits much less coarsening during thermal cycling test. Some re-crystallization of the tin-grains can occur but, it does not demonstrate the negative effect on fatigue life as the coarsening of the different phases in Sn/Pb eutectic alloys. The finer grain structure of the Sn/Ag/Cu alloy solder ball has proved to be less prone to fatigue loading than the eutectic samples tested. The lead-free solder composition, in general, appears to be more mechanically stable and creep resistant than the eutectic SnPb solder alloy.

References

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