

## Flip Chip Assembly of Thinned Silicon Die on Flex Substrates

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### Abstract

The assembly of thinned silicon die (25-100 $\mu$ m) onto flex substrates provides options for ultra thin, flexible electronics for applications ranging from smart cards to space-based radars. For high density applications, 3-D modules can be fabricated by stacking and laminating preassembled and tested flex layers then processing vertical interconnections. This paper describes processes for flip chip assembly of thinned die to polyimide and liquid crystal polymer (LCP) flex substrates.

Two assembly approaches have been developed for use with polyimide and LCP flex substrates. In the first approach, the solder bumped die are reflow soldered to the patterned flex. A fixture is required to maintain the flex substrate flat during reflow. Reflow is followed by underfill dispense and cure. The underfill dispense process is critical to avoid underfill flowing onto the top of the thin silicon die and will be discussed. In the second approach, vias are etched through the polyimide or LCP, exposing the underside of the contact pads. Solder paste is squeezed into the vias, reflowed and cleaned, creating solder 'bumps' in the via. Die with low profile solder bumps created by immersion soldering are fluxed, placed and reflowed. The die is then underfilled. This approach produces a lower total assembly thickness.

### Introduction

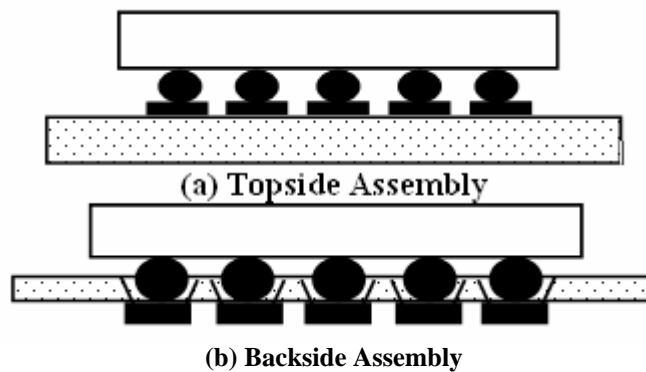
To meet ever decreasing profile requirements in single die and stacked die packages, processes for assembly of thinned die are being developed.<sup>1-4</sup> Flex substrates (25-50 $\mu$ m) provide a means of further reducing package thickness. Thinned Si-on-flex construction is also advantageous for space applications. Thinned Si, while brittle is also flexible. Thinned Si-on-flex can be rolled into a tube for launch and unrolled in space, creating a large area antenna with integrated electronics.

Issues that must be addressed for assembling thinned Si-on-flex include: substrate design and fabrication, bumping after thinning, die handling, substrate flatness during reflow and underfill dispensing. These are discussed in the following sections.

### Substrates

Two flex substrate materials were used in this work: polyimide and liquid crystal polymer (LCP). LCP characteristics include good dielectric properties to 100GHz, low moisture absorption and very low moisture permeability.<sup>5-13</sup> The coefficient of thermal expansion (CTE) of the LCP can be controlled during the biaxial extrusion of the LCP film. Commercial films are available with CTE's of 8 and 17ppm/ $^{\circ}$ C. In this work, the 8ppm/ $^{\circ}$ C LCP film was used.

In a conventional flex substrate design for flip chip assembly, the copper die attach site is patterned on the same side of the flex film as the die will be assembled (Figure 1). Solder mask is used to define the solderable pad area (topside design). An alternate approach is to etch vias through the polyimide or LCP, exposing the underside of the copper pads (backside design). The vias are produced by laser drilling or reactive ion etching (RIE). The flip chip die is assembled from the side opposite the copper pattern (Figure 2), eliminating the need for solder mask and reducing the overall thickness. A further advantage of this approach (low profile bumps) will be described later. Topside polyimide substrates were fabricated by the Applied Physics Laboratory at Johns Hopkins University, while laser drilled backside LCP designs were fabricated by STS ATL Corp. Backside (RIE) LCP and polyimide substrates were fabricated at Auburn University. Only a single layer of metal was required for routing the daisy chain die interconnection pattern.

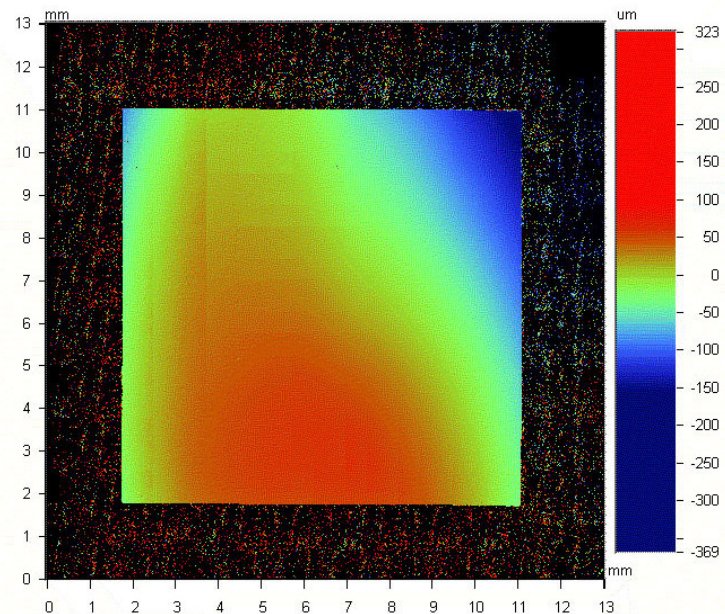


**Figure 1 - Illustration of Topside and Backside Assembly**

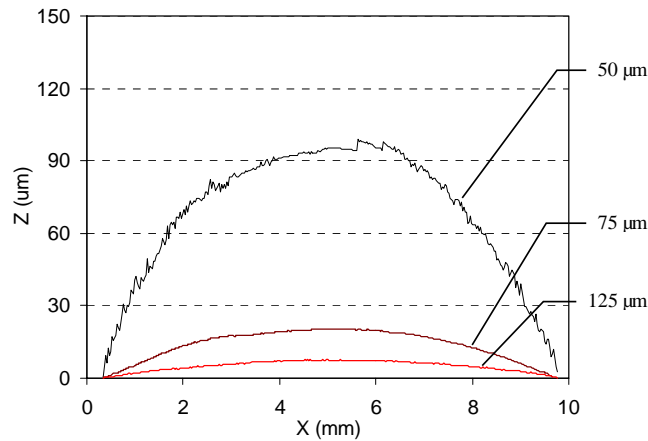
### Test Die

The test die was a 10mm X 10mm, daisy chain silicon chip with 1368 full area array eutectic Sn/Pb solder bumps on a 250 $\mu$ m pitch. A robust precision wafer thinning process was developed at the Microelectronics Research Lab (Columbia, MD) which is successful at thinning wafers, wafer segments, and commercial die to thicknesses as little as 8 $\mu$ m. The generic thinning process consists of the following process steps.

Wafers were thinned from the backside after first being attached to a front side support wafer. Once the wafer was thinned to the target thickness, the wafer backside was mounted to a blank silicon transfer (handle) wafer using a dissolvable adhesive. Then the front side support wafer was released, leaving the thinned circuit attached to the backside handle wafer. This backside wafer is very important in supporting the delicate thinned circuit during subsequent handling, test, wafer sawing, and assembly. Figure 2 is an optical surface profile (Veeco optical measurement system) of a 30 $\mu$ m die released from its handle. Figure 3 plots the curvature of 50 $\mu$ m, 75 $\mu$ m and 125 $\mu$ m die released from their handle. Due to constant stresses from the metallization and passivation, the die warpage increases as the thickness of the Si die decreases.

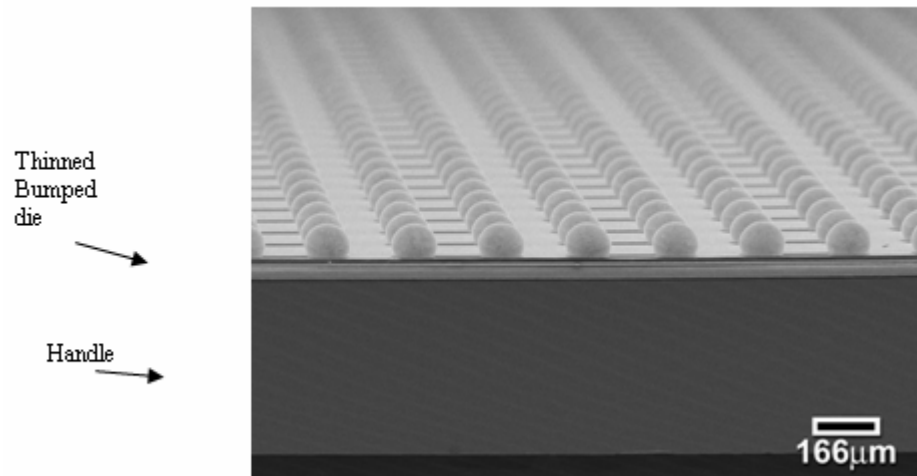


**Figure 2 - Surface Profile of 30 $\mu$ m Flip Chip without Handle**



**Figure 3 – Thinned Die Curvature without Handle**

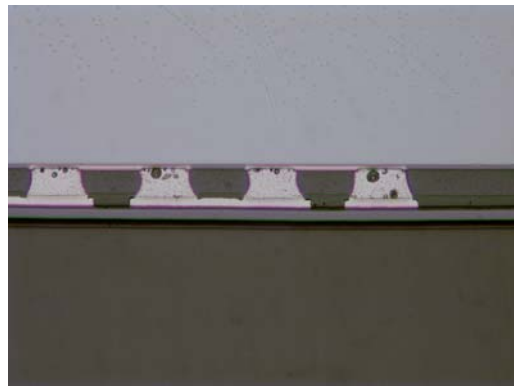
Reports of previous work state a requirement to perform wafer bumping prior to thinning due to the lack of an industrial process for the bumping of wafers in the thinned state.<sup>14</sup> For this project, a process was developed for bumping wafers after thinning, while still attached to the handle wafer thereby reducing the possibility of damage to the front side solder balls. This required a modification to the generic thinning process as well as verification that the adhesive used to secure the thin wafer to its handle would not contaminate the plating baths. Prior to thinning, a Cu/Cr electroplating base was sputtered onto the wafers. Then the wafers were thinned. After release of the front side support wafer, eutectic Sn/Pb was electroplated onto the die pads and the solder was reflowed. All of this was performed while the thinned wafer was still supported by the transfer (handle) wafer. Wafers were then sawn, leaving thinned die still attached to handles. Figure 4 shows a photo of a 50μm die with the thinned die attached to its accompanying handle segment.



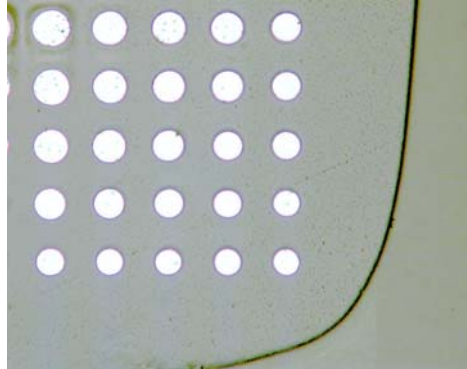
**Figure 4 - Bumped Thinned Die on Handle**

### Placement And Reflow

The flex substrate only had copper patterned on one side and tended to buckle or warp in the center of the die site during the reflow process step. One of the challenges in the assembly process was to keep the substrate flat during all thermal exposures. Initial attempts to use thermal greases to temporarily adhere the flex substrate to a silicon wafer or Kapton tape to tape the corners of the flex substrate to an aluminum plate resulted in distorted solder joints as shown in Figure 5. In this example, the flex substrate buckled in the center, compressing the center solder joints while elongating the corner solder joints. The flat-section was obtained by underfilling the die, curing and then polishing the Si die away to expose the solder joints surrounded by underfill.



**(a) Cross-section**

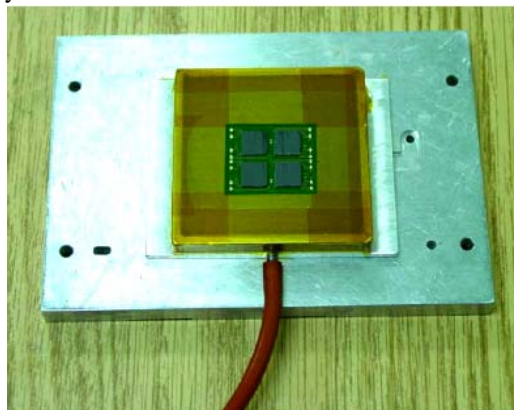


**(b) Flat-section**

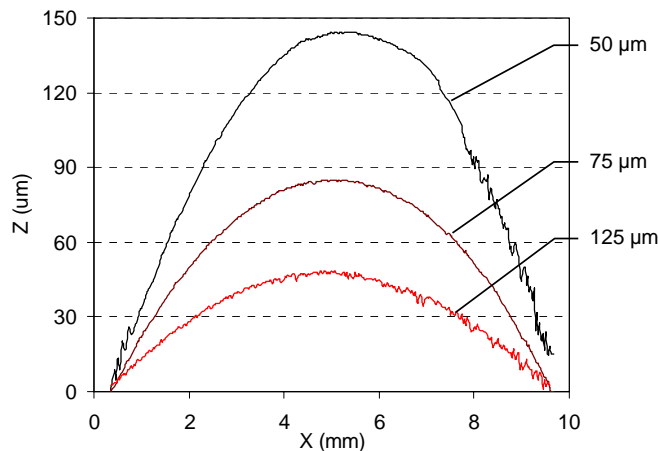
**Figure 5 - Elongated and Uneven Solder Joints**

A vacuum fixture was constructed with a porous sintered block of stainless steel and connected to the house vacuum with a silicone hose. The flex substrate was held flat on the vacuum fixture during all the stages of assembly: placement, reflow, underfill dispensing and curing. The vacuum fixture is shown in Figure 6.

With the substrate held with the vacuum fixture, the flip chip die was assembled with an automatic pick and place machine using a  $25\mu\text{m}$  thick Kester TSF-6522 dip flux. The assembly was reflowed in a nitrogen atmosphere with a Heller 1800 reflow oven. The vacuum hose was fed through the reflow oven with the fixture. The peak reflow temperature was  $230^\circ\text{C}$ . For volume production, a built-in vacuum system integrated into the rails of the reflow oven is envisioned, eliminating the need for the vacuum hose. The flex substrate is sufficiently flat at room temperature to allow die placement; the vacuum hold down is only required during reflow and underfill cure (thermal exposures). After reflow, the assembly was released from vacuum and soaked in acetone to release the backside handle. The handle must be removed prior to underfilling, since the formation of an underfill fillet would prevent subsequent removal of the handle. Figure 7 shows the curvature for  $50\mu\text{m}$ ,  $75\mu\text{m}$  and  $125\mu\text{m}$  die on polyimide flex after handle release, but before underfill. Due to the CTE mismatch between Si and polyimide, the warpage increases slightly.



**Figure 6 - Vacuum Fixture**

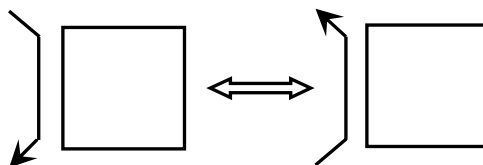


**Figure 7 - Curvature for Non-underfilled Assembly**

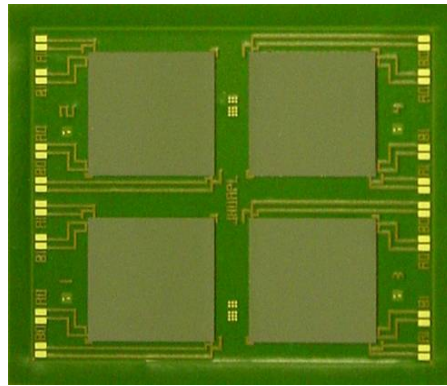
### Underfill

Prior to underfilling, the assemblies were baked overnight at 125°C for dehydration and to drive out the solvent from the handle release process. An argon plasma treatment was used to enhance the wetting of underfill to the substrate, decreasing the contact angle and increasing the underfill flow rate. A low modulus, low stress capillary underfill (Loctite Hysol FP6100) was chosen to match the flexible assembly. The underfill challenge was to dispense the underfill without getting underfill on top of the very thin Si die. A multi-pass dispensing pattern was developed, as illustrated in Figure 8. The dispense pass direction was alternated. The dispense pattern lead away from the corners of the die to minimize the build up of a thick underfill bead, ensuring the underfill thickness was lower than the top of the die when it reached the die. Time was allowed for the underfill to flow under the die between passes. The substrate was heated to 120°C during dispensing to decrease the underfill viscosity and increase flow. The underfill material was dispensed in eight alternating passes per die with a 23 gauge needle on Camlot 3700 dispensing system and cured at 170 °C for 30 minutes in a box oven. The substrate was held flat on the vacuum fixture during the entire underfilling process. This was necessary due to the die curvature previously noted after the the Si die was released from the handle after reflow assembly. Die with thicknesses ranging from 25 to 250µm were successfully underfilled without underfill on top of the die. Figure 9 shows an example of a 50µm assembly.

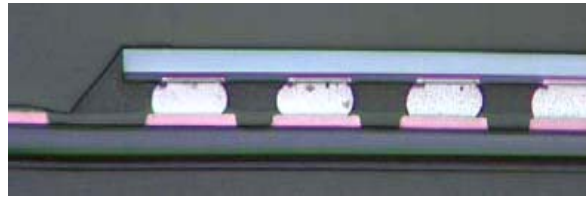
Figure 10 shows a cross-section of a 50µm die after underfill. Uniform shaped solder joints were obtained. Figure 11 shows the die curvature after underfill as a function of Si die thickness. With underfill, the curvature of the thinner die decreases while the curvature increases for the thicker die when compared to the non-underfilled curvature. Figure 12 shows the flexibility of the completed assembly. Besides curvature, a surface ripple was detected for all thinned die less than 250µm thick, as shown in Figure 13. The ripple only occurred after underfilling and is thought to be the results of the contraction of the underfill in the z-direction during cooldown. Since the underfill contracts more than the solder balls, the Si die is 'pulled down' between the solder balls by the underfill. The extend of rippling increased as the die thickness decreased. The effect of curvature and the local ripples on the electrical performance of Si die must still be determined. Electrical effects may limit the minimum die thickness and not assembly processing.



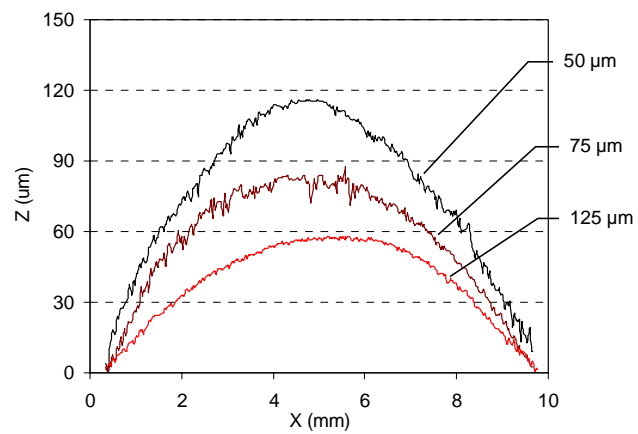
**Figure 8 - Underfill Dispensing Pattern**



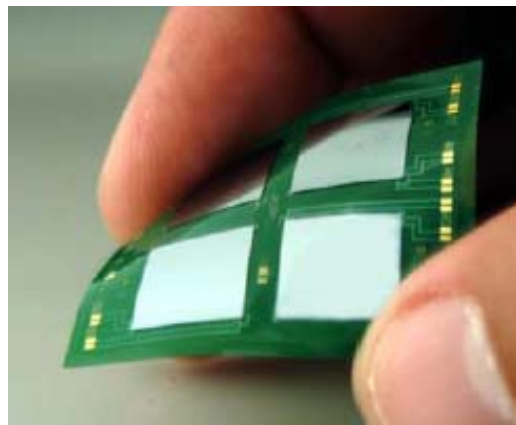
**Figure 9 – Assembly with Four 50 $\mu$ m Die**



**Figure 10 - Cross-section of 50 $\mu$ m Thick Die Assembly after Underfill**

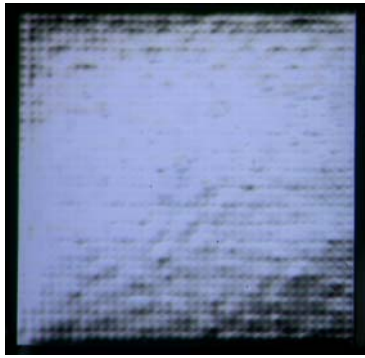


**Figure 11 - Curvature for Assembly with Underfill**

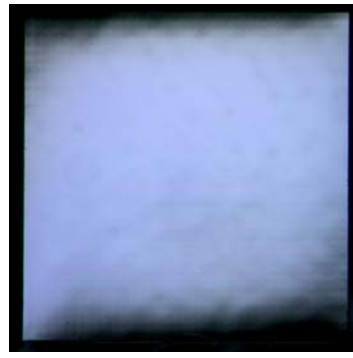


**Figure 12 – Flexibility of 50 $\mu$ m Assembly**





(a) 25  $\mu\text{m}$  underfilled



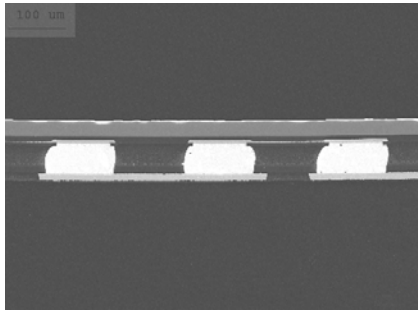
(b) 50  $\mu\text{m}$  underfilled

**Figure 13 - Surface Image of Thinned Die Assembly (Backside of Die) Showing 'Ripple' Effect**

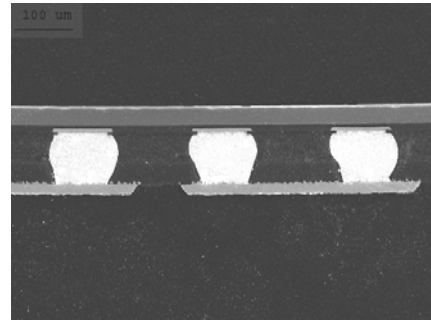
#### **Assembly on Backside Design Substrates**

Identical assembly processes were used to successfully assembly bumped, thinned Si die to the copper pads through vias etched in the polyimide (Figure 14a) and LCP (Figure 14b) substrates. Assembly into vias in the flex substrate provides an opportunity for an alternate bumping strategy. As previously noted, the test die were bumped by electroplating after wafer thinning. A lower cost bumping option would be to deposit the under bump metallurgy (UBM) by thin film processing or electroless Ni plating and create low profile bumps by fluxing and immersing the wafer (or die) into molten solder prior to thinning. The electroless Ni/solder immersion bumping is particularly attractive for single die processing during prototype development or for low volume space applications. An example bump is shown in Figure 15. The low profile bump is compatible with the wafer mounting and thinning process. It is also compatible with commercially available single die and wafer thinning services.

To complete the assembly, additional solder must be added to the mating substrate. This is easily accomplished by using a squeegee to deposit solder paste into the vias at the die site and reflowing. Without using a stencil, three squeegee and reflow cycles are required to deposit sufficient solder. It is anticipated that use of a stencil would result in sufficient solder in a single pass. After reflow, the flux residue is removed by aqueous cleaning. The low profile bumped die is then assembled as before. A cross section of a low profile bump assembled on an LCP substrate is shown in Figure 16. Further work is required to investigate the hour glass shape of the solder joint.

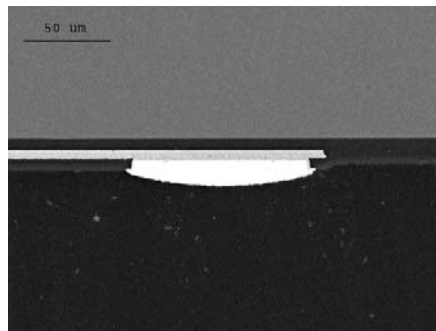


(a) Polyimide

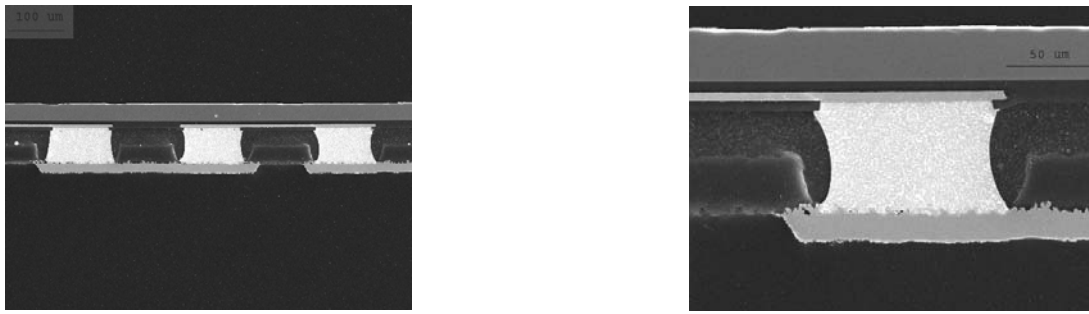


(b) LCP

**Figure 14 – Backside, Thru-via Assembly**



**Figure 15 - Cross-Section of Low Profile, Immersion Solder Bumps**



**Figure 16 – Backside, thru-via Assembly with Low Profile, Immersion Bump on LCP Substrate**

### Summary

Assembly techniques have been described to successfully assembly Si die as thin as 25μm to polyimide and LCP flex substrates (25 and 50μm). Key issues are: 1) substrate flatness during assembly, especially reflow and 2) underfill dispense without flow onto the top of the die. The final assemblies have increasing curvature and ripples with decreasing Si die thickness. The effect of these on electrical performance of the Si die must still be determined. Initial reliability tests (50μm Si die on 50μm polyimide substrates) are underway and indicate no significant difference in thermal cycling reliability with or without underfill. Modeling is underway to identify the optimum underfill properties for thinned Si-on-flex assemblies.

### Acknowledgements

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