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Development of High Density Wiring Technology and Interconnect Technology with Silicon Through-Hole

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Abstract
We have developed the copper high density wiring formation technology with Cu/photosensitive Benzocyclobutene (BCB) as a dielectric material, and interconnect technology with Silicon through-hole. The basis is four-layer structures with copper conductors and BCB dielectric formed on the core substrate. We have adopted stacked via structure as multi-layer and the Si wafer for core substrate. We selected the metal titanium as an adhesion layer between the conductors and the dielectrics before copper conductor layer formation. We measured the adhesion strength between conductor metal and BCB using the 90-degree peeling test. The peeling strength becomes stronger than 0.50 kN/m by performing the suitable pretreatment on the BCB. The core substrate is composed of copper plugs, which connect the front and backside of the wafer electrically. The copper plugs are 30 μm in diameter and 250 μm depth. We have succeeded in production of plugs without voids and have confirmed good reliability by THB test and the heat cycle test.

We have also measured and simulated the fundamental transmission properties of micro strip line of Cu/BCB multi-layer wiring structure and compared with the another dielectric material such as PI and Fluorene. The frequency was swept from 100 MHz to 40 GHz, and two-port parameters such as S_{11} (reflection) and S_{21} (transmission) were extracted. The result is that transmission loss of BCB is maintained about 1.5 dB at 30 GHz, when the line length is 5 mm and the line width and space are 10 μm /10 μm. It was most excellent in especially high frequency range as compared with other dielectric materials. We obtained approximately same result also in the simulation. We have confirmed good agreement of transmission properties of micro strip line structure between simulation and measurement data.

Introduction
Recently, electric device become smaller and lighter with increasing a number of functions. The ITRS roadmap for the Flip chip pad pitch and the high frequency characteristics are shown in a Table 1. As for the flip chip pad pitch, it is shown about the trend of high-density required 90 μm level, and Line and space is required 10.7 μm in 2004. On the other hand, about 3 GHz high speed clock is required in On-Chip performance. So, a packaging technology is also asked for high-density and high-speed characteristic. As a technology, which fills these demands, we have introduced B^2it^{TM} (buried bump interconnection technology) for this technical trend [1], [2].

In this work, We have developed the interposer by the copper high density wiring formation technology with Benzocyclobutene (BCB) as a dielectric material, which shows superior electrical properties such as low dielectric constant and the low dissipation factor in high frequency. We adopt the 6-inch Si wafer as an interposer. We have also measured and simulated the fundamental transmission properties of micro strip line of Cu/BCB multi-layer wiring structure. The result shows that BCB is most excellent in especially high frequency range as compared with other dielectric materials, such as PI and Fluoren.

Table 1 – Technology Nodes for High Density Packaging

	2003	2004	2007	2009	2016
Technology Nodes (nm) MPU/ASIC	107	90	665	50	25
Needs for BGA Ball-Pitch (mm)	0.40	0.40	0.20	0.20	0.15
Ec Pad Pitch (mm)	0.15	0.15	0.12	0.10	0.08
Line (mm)	10.7	10.7	8.5	7.1	5.70
Space (mm)	10.7	10.7	8.5	7.1	5.70
Performance On-chip (GHz)	3.09	3.99	6.74	12.0	29.0
Performance Chip-to-board for Peripheral Busses (GHz)	2.00	2.50	4.88	7.63	2.90

The Outline of the Developed Substrate

Figure 1 shows the schematic view of the developed substrate. The upper part (a) is a high density wiring layer for achieving connection with a LSI chip. This layer consists of fine wiring layer by sputter-semi-additive process, and a low dielectric constant insulation layer by the photo-via process. These technologies can realize high density and reduce the number of layers as described below. The design rule is as follows, line and space are 5 μm /5 μm and via and via land diameter are 20 μm /30 μm. We adopted the copper conductors and BCB dielectrics. The down part (b) is connection layer for achieving connection with a motherboard. Si core substrate has copper plugged through-hole for connecting between the high-density wiring layer (a) and the connection layer (b) and it has 300 μm or less thickness. Each connection is made with a solder ball and we adopt the copper wiring. The process of each position is described 3 and 5 chapter. The core substrate performs only vertical connection.

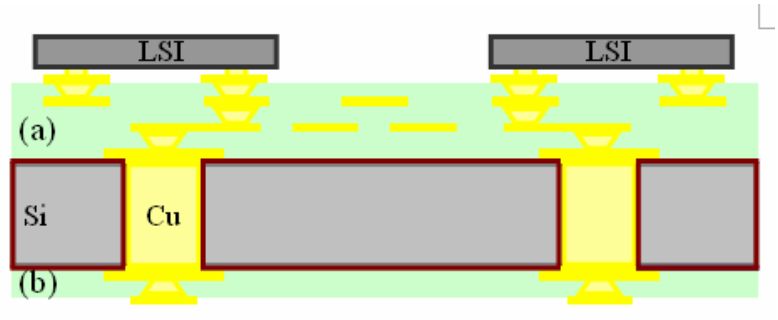

Figure 1 – Schematic View of the Developed Substrate

Core substrate Fabrication Process

Figure 2 shows the fabrication process for core substrate applied to this experimental. We tried the two-type process for making the Si core substrate. Type A was named trench method, and type B was named through in advance method.

In the case of trench method, first, the through hole was etched by an ICP-RIE process using a photoresist mask (PMER-LA900, Tokyo Ohka). The etching gas is C_4F_8 and the deposition gas is SF_6. The etching rate is about 5.5μm/min. The diameter is 10~300 μm and the depth is 170~400 μm. Secondly the surface was covered with SiO_2 using thermal oxidation. The thickness of SiO_2 is 800 nm. The hole was filled using the electroplating copper on metal organic chemical vapor deposition (MO-CVD) TiN/Cu barrier and seed layer. Figure 3 shows the coverage of MO-CVD films. The hole diameter is 10 μm and the depth is 170 μm. MO-CVD gives good coverage over sidewall and bottom of aspect 17 holes. Si core substrate was gliding in the thickness of 400 μm by CMP. Finally SiO_2 is sputtered backside, pattern etched and opening pads. Figure 4 (a) shows the cross sectional view of the hole, which diameter is 30 μm and the depth is 300 ~ 400μm (aspect ration is over 10), after filling the holes by electroplating method. We could confirm a few voids. As the hole diameter become large, we couldn't fill the hole by this method.

In the case of through in advance method, the hole was also etched by an ICP-RIE process, and was penetrated previously by back grinder. MO-CVD TiN film was deposited from the both sides after thermal oxidation for copper diffusion barrier. The TiN film thickness is 30 nm. The hole was filled using the electroplating copper. Finally Si core substrate was polished from the both side by CMP. Figure 4 (b) shows the results of filling with copper electroplating by through in advance method. The good filling characteristic is acquired. By using this method, we could fill the holes perfectly regardless of the hole diameter.

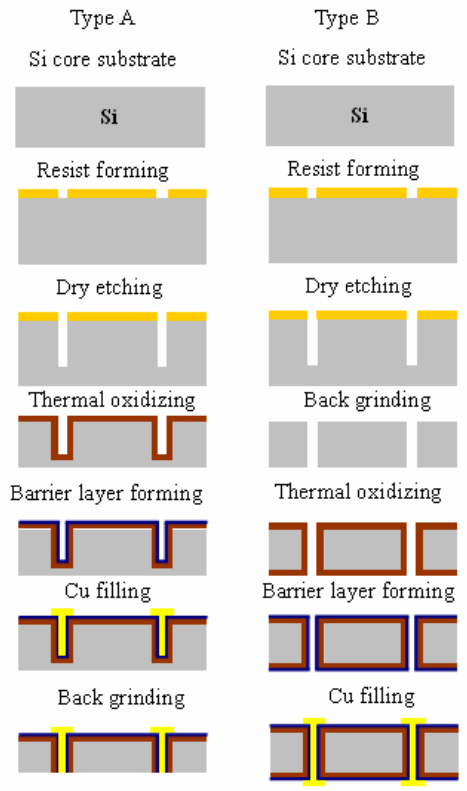

Figure 2 – Fabrication Process of core Substrate

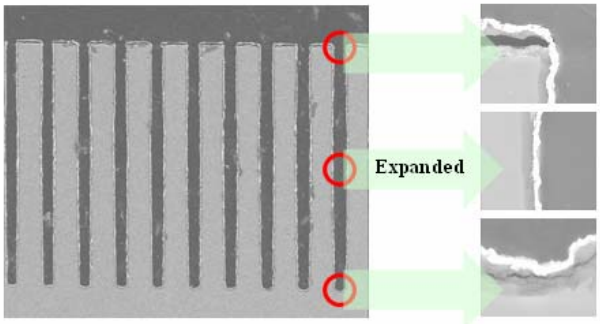

Figure 3 – Coverage of MO-CVD TiN/Cu

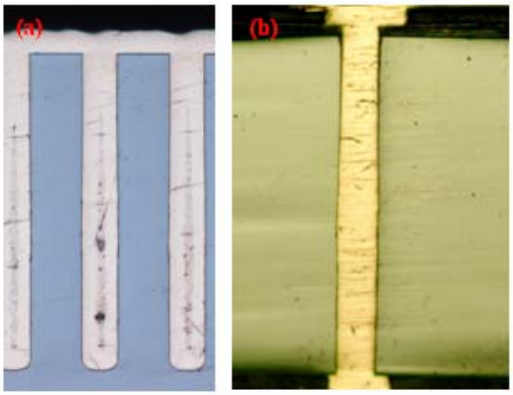

Figure 4 – Cross Sectional View of the Hole

Reliability of the Cu through Plugs

We measured the reliability of Si core substrate made by through in advance method and investigated the influence by the existence of TiN barrier films. We selected the thermal cycle test (TC) and temperature humidity bias test (THB) for reliability test. The schematic view of the sample is shown in Figure 5. The thickness of thermal oxidation film and TiN barrier films is 800 nm and 30 nm respectively. The daisy chain is located in a line with 2 sequence parallel. A number of holes are 196 in one piece, the number of holes of outside sides chain is 100, and the number of holes of inner sides chain is 96. The hole diameter is 30 ,50, 85 μm. We prepared the two type of hole pitch. One is the hole diameter plus 30 μm (60, 80, 115 μm respectively), and the other is 1000 μm fixed. The hole depth is 400 μm. In the case of THB test, the sample was placed at the condition of Table 2 (a). We established that the threshold resistance is 1E10+8 Ω. We performed measurement for 1000 hours. The results are shown in Figure 6. A difference is not seen by the case where there is TiN for the insulation resistance. For the sample without TiN barrier films, the insulation resistance was reduced to 1E10+7 ~ 1E10+8 soon after the examination start. This is the same as the resistance of Si substrate. We expected that ion migration was occurred, when there was no TiN barrier films. In the case of TC test, the sample was placed at a temperature of 85 degrees C and at a humidity of 85 % in 168 hours. Then, the sample was placed at the condition of table 2 (b). After TC test, we measured the insulation resistance and conduction resistance. We computed the conduction resistance of the 1 copper through plug by the resistance of the 100 copper through plugs divided by 100. One part of the results is shown in Figure 7. The conduction resistance is almost same value before and after examination. It is stable regardless of the existence of TiN barrier films. The insulation resistance is also almost same value before and after examination for the sample with TiN barrier films, but it was reduced to 1E10+8 immediately after the test start for the sample without TiN barrier films, like the case of THB test. We think that this is attributable to the ion migration. From these results, we confirmed the necessity for TiN barrier films and good reliability was acquired when there is the TiN barrier films.

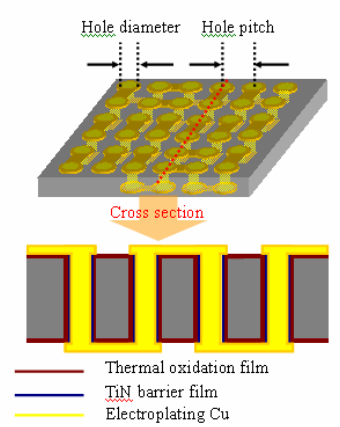

Figure 5 – Schematic View of the Sample

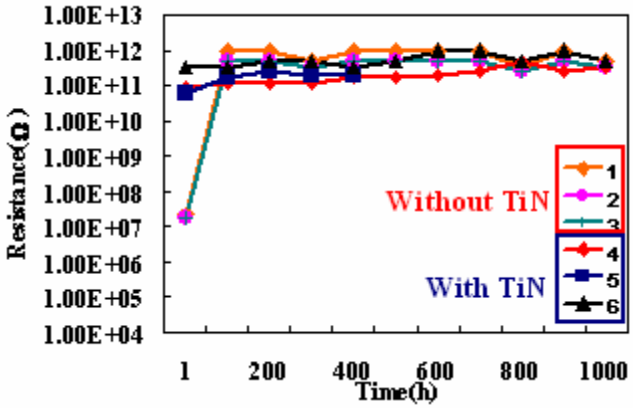

Figure 6 – Results of the THB Test

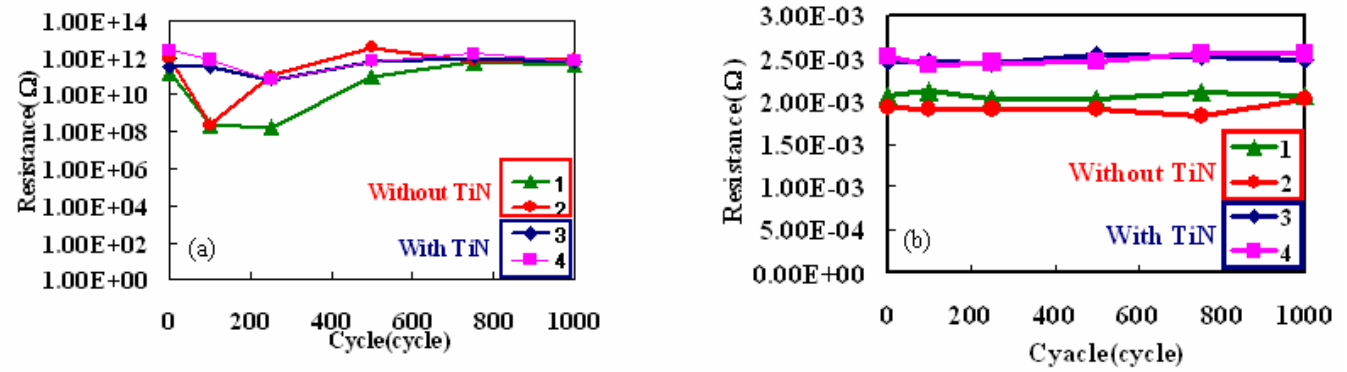

Figure 7 – Results of the TC Test (a) Insulation resistance (b) Conduction resistance for 1plug

Table 2 – Measurement Condition of Reliability Test (a) THB Test Condition (b) Test Condition

Measurement condition			
Temperature	85 ℃	Hole diameter	30,50,85 μm
Humidity	85%	Hole pitch	60,80,1000 μm
Additive V	10 V	Number of Hole	In 96
Measurement V	10 V		Out 100

Measurement condition			
Temperature	-55 ~ 125℃	Hole diameter	30,50 μm
1 cycle time	15 min	Hole pitch	60,80 μm
Total cycle	1000 cycle	-	-

Fine Wiring Layer Process

Fine wiring forming technology is adopted by the sputter semi additive method. If a wiring pitch is under 20 μm or less, by the etching method, wiring formation will become very difficult because wet copper etching goes on isotropic. On the contrary, if the semi additive method adopted, wiring width is mostly oriented by the resolution of a photo resist. Thus, under 20 μm pitch fine wiring can be realized. Figure 8 shows the fabrication process for the fine wiring layer. We adopt the Photosensitive-BCB as a dielectric layer, because BCB shows superior electrical properties such as low dielectric constant and the low dissipation factor in high frequency. BCB was coated by spin coating method. The thickness is designed for impedance matching of 50 Ω for micro strip line structure. Next the Cu/Cr or Ti seeds layer whose thickness is 200 nm and 30 nm respectively, was sputtered after pretreatment of BCB surface. Because, there is BCB residue in the bottom side of via holes. A plasma treatment is necessary to remove a thin film of polymer residue. In addition, between the Cu and the BCB layers, the adhesion was originally not sufficient. So, it is necessary to perform a suitable treatment on the surface of BCB. Figure 9 shows peel strength among each BCB pretreatment condition before sputtering. CF_4 and Ar treatment before sputtering is good effect on BCB surface. On the other hand, a result of oxygen plasma treatment was not good characteristic. This is because BCB surface is cleaning by Ar treatment without deforming the surface, but O_2 treatment oxygenates the Si surface, which is one of the elements of BCB materials composition. We believe SiO_2 which is formed by O_2 treatment reduce the adhesion strength. The maximum peel strength 0.44 kN/m is obtained by performing the CF_4 & O_2 pretreatment and Ar pretreatment on the BCB surface. This value is 20 times stronger as compared with that of without pretreatment. However, this is not so big value as that between dielectric and seed layer generally. We can observe the BCB material on the sputtered Cr conductor by the break mode analysis after the peel strength test. The cohesive failure was caused between BCB and sputtered Cr conductor. Therefore the peeling strength between Cr and BCB is more than 0.44 kN/m. We confirmed the same result, when Ti is used for an adhesion layer.

We have developed two-layer wiring with a thickness of 4 μm on the Si core substrate and stacking via structure. Also investigating line width reproducibility, it was possible to produce the stable formation of wiring pitch 10 μm (Line and Space is 5/5 μm). Furthermore, extremely nearing wiring pitches is 6 μm (Line and Space is 3/3 μm). Next, we examined the via-on-via-staked structure with the filled plating process. It becomes advantageous to design freedom for high-density wiring substrate. Via / via land diameter is 20 μm /30 μm. To remove the remaining thin-film of BCB residue at via bottom, we performed a dry etching process using CF_4 and O_2 gases when stacking after the second layer formation. A small via hole was completely filled with copper without voids. Figure 10 shows the photograph of fine wiring and stacking via structure.

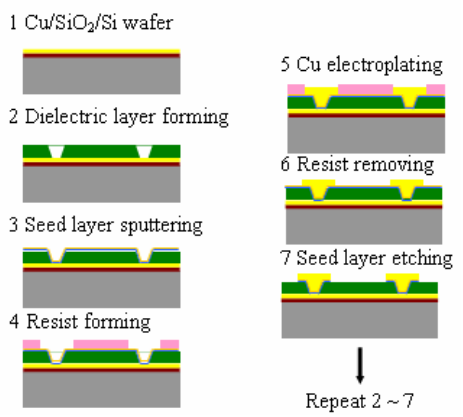

Figure 8 – Fabrication Process of Fine Wiring Layer

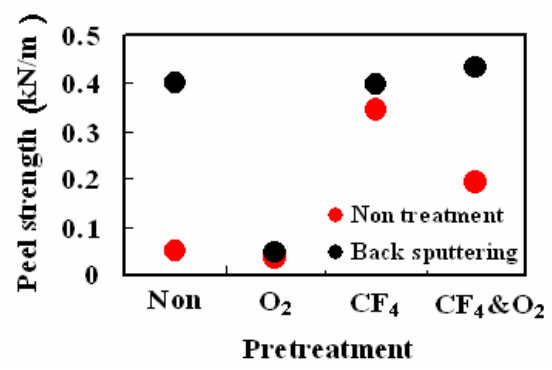

Figure 9 – Pretreatment Condition among each PCB

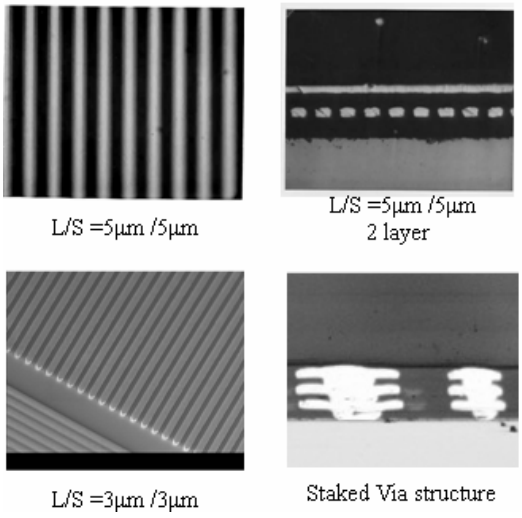

Figure 10 – Photograph of Fine Lines

Electrical Characterization

It has become important to estimate the high frequency performance of transmission line in the package. We evaluated the transmission loss with the each dielectric materials (PI, BCB, Fluorene in Table 3) thorough experimental measurement and simulation. The frequency was swept from 100 MHz to 20 GHz. Two port S-parameter such as S_{11} (reflection) and S_{21} (transmission) were extracted. We used a HFSS (3-dimensional high frequency electromagnetic boundary simulator) produced from ANSOFT as a simulator and an HS8722ES network analyzer produced from Agilent technology as experimental measurement. The TEG pattern, which we used for experiment, is described in Figure 11. The probe pitch is

200 μm, and line length is 15 mm. Micro strip line of TEG type is GSG (ground-signal-ground) but GS (ground-signal) probes were used in this time.

Table 3 – Comparison of Dielectric Material

Polymer	Polyimide (PI)	Benzocyclobutene(BCB)	Epoxy acrylate(Fluoren)
Posi or Nega	Nega	Nega	Nega
Tensile Strength (MPa)	63	87±9	74
Tensile Modulus (GPa)	-	2.9±0.2	2.5
Stress (MPa)	-	28±2	-
Tg (°C)	-	>350	180
Td(5%) (°C)	430	>400	340
CTE (ppm / °C)	80	52	80
Dielectric constant ε	2.59-2.71 (1~20GHz)	2.65 (1kHz~20GHz)	3.4 (1MHz)
dissipation factor tan δ	0.007 (1kHz)	0.0008 (1kHz ~ 1MHz)	0.03 (1MHz)

Figure 12 shows the measurement result of S_{21} as compared with the kind of dielectric materials such as BCB PI, and Fluorene. In Figure, the line width is 6 μm, the length is 15 mm and the conductor thickness is 4.7 μm. The characteristic impedance is controlled at 50 Ω by changing the thickness of the dielectrics. This result shows that the transmission loss is more than –3 dB up to 16 GHz on BCB. BCB has excellent electrical transmission characteristic advantage compared with other materials. This is because BCB has very low dissipation factor as shown in Table 2.

Figure 13 shows the measurement result of changing conductor line length (L) and line width (W). In this Figure, the line thickness is 7.8 μm. The signal attenuation of the 6 μm line is –1.3 dB at 20 GHz for 5 mm length, -3dB for 15 mm length. We have confirmed that attenuation loss of a signal is enhanced according to the increasing of wiring length but line width change effect toward to attenuation loss is negligible small as compared with line width change effect. We obtained the approximate same result in simulation. We estimate that the signal transmits the boundary of dielectrics and metal layer in wiring owing to the skin effect. So, attenuation of a signal is not influenced even if a cross-section area of conductor line decreases by narrowing the line width.

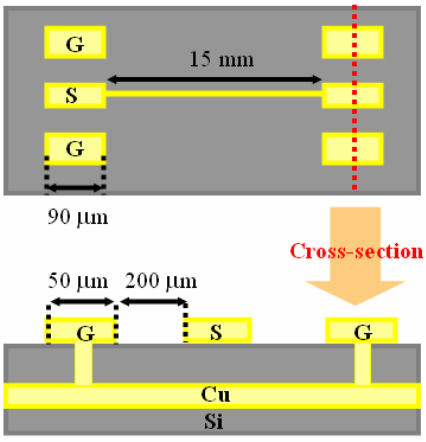

Figure 11 – Geometry of TEG

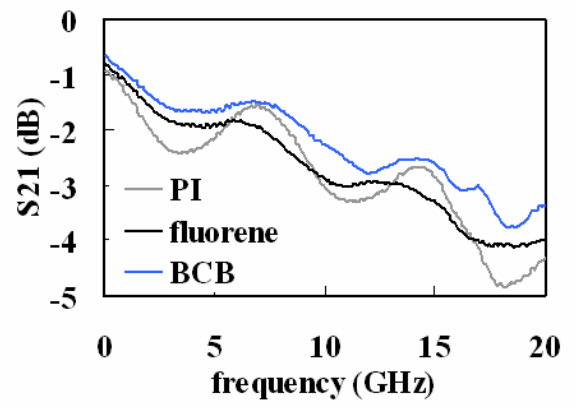

Figure 12 – Transmission Loss Depending on Dielectric Layers

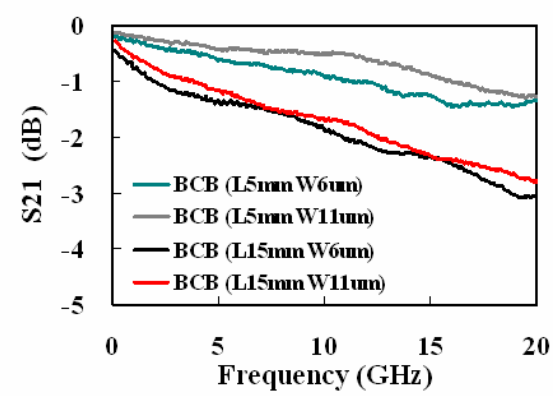

Figure 13 – Influence of the Line Width and Length

Summary

As a result, we have established the technology for forming the copper plague in Si core substrate. We fabricated the two process type for making Si interconnection. One is the Type A named as trench method, and the other is Type B named as through in advance method. Type A could almost fill the holes, which is 10 μm in diameter and 170 μm depth, however, a few voids still remain. Type B could completely fill the holes, which is 30 ~ 85 μm in diameter and 300 ~ 400 μm depth. We confirmed the necessity for TiN barrier films and good reliability was acquired when there is the TiN barrier films.

We have developed high density wiring Cu/BCB multi-layer and filling via process whose diameters is 20 μm in order to contract the via structure. The limitation of the minimum pitch was now 10 μm (L/S=5/5 in design width) considering the process stability for mass production. The stacked via hole with 20 μm in diameter was successfully formed by using filled via holes.

Furthermore, we have also confirmed the excellent high frequency transmission characteristic by measuring the S_{21} parameter of micro strip line structure and comparing with the three dielectric materials (BCB, PI, and Fluorene). The signal transmission loss of BCB is less than –3 dB up to 16 GHz when the line width is 6 μm and the line length is 15 mm. The attenuation loss of a signal is enhanced according to the increasing of wiring length but a line width change effect toward to attenuation loss is negligible small as compared with line width change effect. A fine wiring technology was developed and designed for a high density and high-speed substrate.

Reference

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