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Applying a New In-Circuit Probing Technique for High-Speed/High Density Printed Circuit Boards to a Real-Life Product

Chris Jacobsen and Kevin Wible
Agilent Technologies
Loveland, CO

Abstract
Design for test rules (DFT) for in circuit test (ICT) test pads are well known and have served the industry well for nearly two decades. However, increasing PCB densities continually put pressure on board designers to eliminate ICT testpads. Furthermore, recent technical advances in operational board speeds are leading some designers to believe that ICT test pads cannot be added in the high-speed sectors of boards soon to be designed. Since the effectiveness of ICT is directly related to test pad access, some have questioned the long-term viability of ICT in this high density/high speed PCB environment.

Parker has introduced a new ICT probe technique in 2004 to address these issues.[1] We've been calling them "bead probes". Parker shows that this new technique will not degrade the high-speed circuit performance of tomorrow's gigabit logic boards. He also presents test results showing that this new technique can be used with typical PCB assembly processes and ICT fixtures with similar electrical performance and reliability to current ICT probing techniques.

This paper will continue that discussion and further demonstrate how these non-traditional pads have little impact on layout for test pad placement using results from a real PCB design process. It will discuss DFT guidelines for "bead probes" and discuss possible barriers to creating beads in an outsourced manufacturing environment. Finally, now that ICT access to high-speed sectors on PCBs will be available, a survey of viable ICT test techniques will be presented.

Bead Probe Review

The following section is a review of Parker's paper.[1]

In-Circuit test depends on some amount of direct nodal contact (or "access") via a "bed-of-nails" fixture. This allows the ICT system to switch in any of a set of resources needed to perform a test. This may be as simple as making a two-wire measurement of a resistor value, or setting up hundreds of digital drivers and comparators, driven by a digital test sequencer for performing a digital test. Two key reasons why nodal access may be limited are:

- Density of devices, pins and traces on the board.
- Standard access points interfere with board electrical performance.

Probing Boards

Rules related to probing are driven by the need to reliably make hundreds or thousands of probe contacts with each board. This must be accomplished many thousands of times during the life of an ICT fixture. If even one probe fails to make contact, a board may not be testable, or worse, tested incorrectly. This has generated industry norms for board probing; what you could call "Design for Probe-ability".

Probes can be thought of as little spears that are aimed at targets on a board. Bullock[2] gave rules for forming such targets, or using "natural" targets that may exist on a board. One common natural target is a via that connects segments of a trace on different board layers. However, as trace dimensions continue to shrink along with device and pin sizes, the targets we want to probe become smaller to the point where they cannot be hit reliably. Thus there is a practical lower bound on target size. Bullock cited 35 mil (0.89 mm) round targets as a reliable size. Today, some are pushing the limits down to 26 mils (0.66 mm) and even lower, at greatly increased expense and risk to probing success. Note that a 35 mil round target has an area of 962 mil^2 while a 0204 surface mount device has an area of 800 mil^2. Thus a test access point can consume an area that could have contained a device. But worse, consider that PC trace widths used for controlled impedance boards have very strict line width and space requirements. In modern high-speed designs, trace widths and spaces as small as 3 mils (0.076 mm) may be used. At gigabit data transmission rates, there is little tolerance for deviations in these specifications. Thus, asking a designer to add a 35-mil target to a 3 mil wide trace is not likely to be met with friendly acquiescence.

Inverting the Probing Paradigm

The ICT bed-of-nails fixture has been an accomplished technology for decades. We know how to assure that thousands of spear-like probes will successfully hit their targets on the board, day after day.

But, what if we were to invert this model? What if the board contained the probe and the fixture contained the target? Imagine for a moment that you could somehow place a tiny probe on a board and you had a 35-mil target in your fixture. The tolerances and accuracies you currently know how to manage are all still applicable. In principle, this could work. The question is, how to place a probe on a board, and, how will it affect the board's performance? And of course, it's got to be inexpensive, reliable and repeatable.

Bead Probes

Placing a new component on a board, one that is similar in width to the trace we want to contact, would be difficult. However, we can engineer a very small hemi-ellipsoid of solder, what we call a "bead probe", detailed below. This bead would lie on top of a trace, aligned to its width and following the trace for 4 to 6 times its width. This bead would be only a few mils tall, clearing the surrounding solder mask by several mils.

The Bead Probe and Fixtured Target End and side sectional views of solder bead are shown in

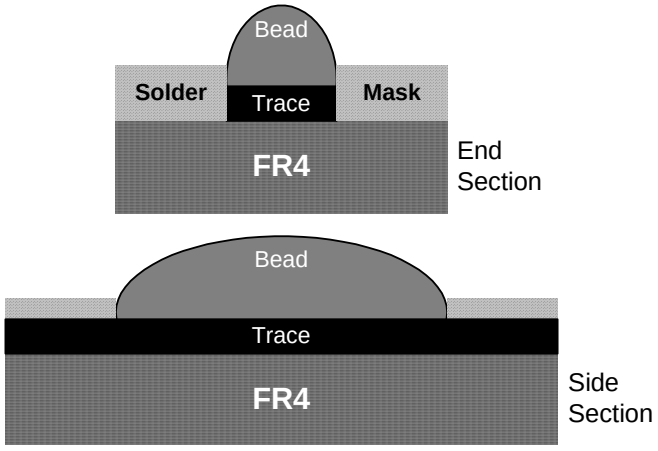

Figure 1 Figure 1. The volume of solder, the area of exposed copper and surface tension determine the size and shape of the bead while it is molten.

The bead protrudes above the solder mask that is typically only a mil or two thick. When the fixture is activated, bringing the board into contact with the fixture probes, the probe targets situated in the fixture that will contact the bead probes. The fixture targets are round, flat-faced spring-loaded "probes" we often use for probing pointed objects such as through-hole pins. Now their role is reversed to being the target. See Figure 2.

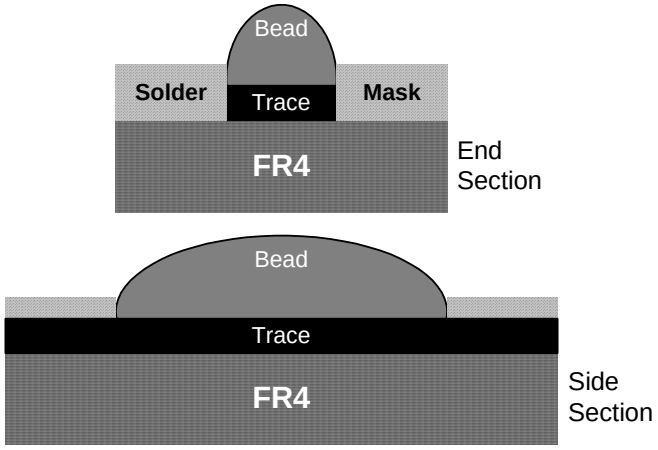

Figure 1 - End and Side Sectional Views of a Bead Probe

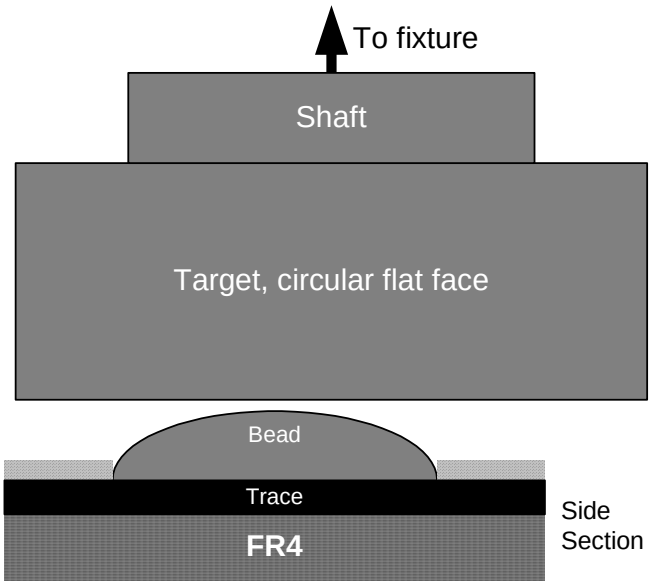

Figure 2 - Side View of Bead Probe and Target

Note that the inevitable registration errors become lateral translation errors, where the bead probe and the target are not perfectly centered. The errors that occur are the same we have been handling for many years.

Assuming the target is 35 mils, the bead in Figure 2 appears to be about 17 mils long. From Figure 1 one would surmise the bead is 6 mils wide and maybe 4 mils tall. It turns out that these (or similar) dimensions are critical to the performance of bead probes. This will be explained in section 1.6. Suffice it to say here that bead probes are very small, nearly invisible to the naked eye, and, there is such a thing as a bead that is too big.

Fabricating a Bead Probe

A bead probe is manufactured using the same steps that all other solder features follow. The solder mask is opened up over the trace where we want a bead. When solder flows and then freezes, it will wick up onto the copper trace due to the affinity of solder for copper and lack of affinity for the mask. At this scale, surface tension will completely overwhelm gravity, causing the bead to have a curved surface. The solder mask opening defines the outside dimensions of the bead.

The height of the bead is controlled by two factors. First, by volume, a typical solder paste is roughly 50% flux, which will vaporize during reflow. Thus roughly ½ the volume of paste will be deposited as solder. The solder stencil aperture is sized to assure that enough solder is deposited to later "bead up" via surface tension to a height that exceeds the surrounding mask. An example stack up of trace outline, solder mask and stencil holes is shown in Figure 3.

The solder mask hole is an obround hole (rectangular with rounded ends) of width W and length L center to center as shown. The width should be equal to or less than the width of the trace. The length should run in the same direction as the trace. Choice of width and length is given in the next section. The area of the obround hole, which exposes copper, is $WL + \pi (W/2)2$.

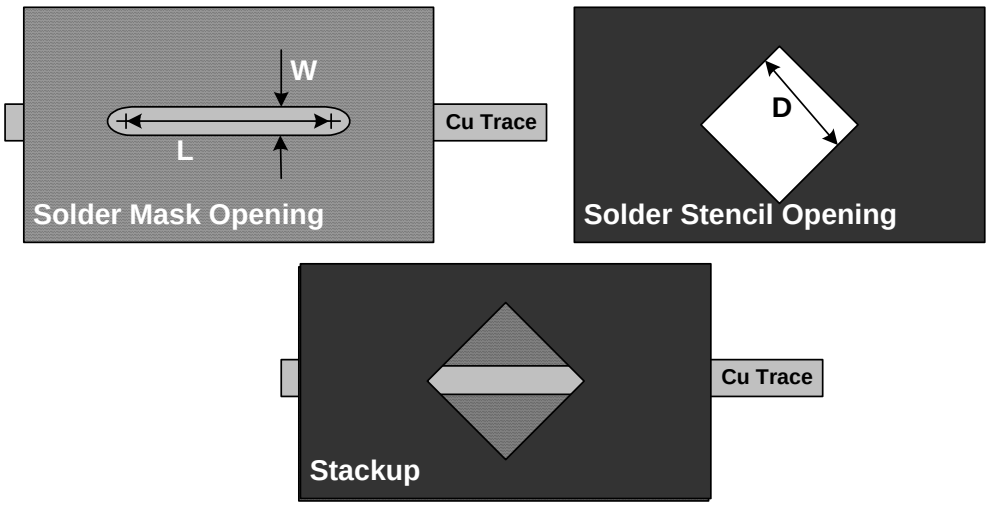

Figure 3 - Board, Solder Mask and Solder Stencil Layer Stack Up for a Bead Probe

The solder stencil hole is a square (side length D) rotated 45 degrees to the trace and centered on the bead location. This hole is larger in area, D2, than the mask hole. The rotation maximizes the area of copper that will receive solder paste, while the square is a preferred geometry for reliable stenciling. Some paste will be applied to the solder mask, but this paste will flow onto the copper when melting. The thickness T of the stencil will also determine the amount of solder paste that is applied. The paste volume applied to the board will be TD2, which after vaporizing the flux will yield TD2/2 volume of solder.

Given W, L, D and T, we can calculate the approximate height H of the resulting bead as follows. Divide the solder volume by the exposed copper area, or:

$$H \approx (TD^2/2) / (WL + \pi(W/2)^2)$$

If we are given W, H, D and T, then we can calculate the approximate length of the bead as:

$$L \approx ((T*D^2/2) / (H*W)) - \pi W/4$$

Theory of Operation

ICT bed-of-nails probing works by using sharp pointed probes to hit targets on a board. Consider a spear-shaped probe contacting a solder-covered target. The spring-force of the probe will force the sharp point into the solder for some distance. The spring force and the yield strength of solder govern this distance. Yield strength for solder (leaded and lead-free) is about 5000 pounds per square inch.

As the spear point first touches the solder and any oxide or contaminants on its surface, the area of the point is not large enough to support the spring force, causing the solder to yield. The point of the probe begins to enter the solder, displacing any oxide or contaminants. As the probe tip continues to enter the solder, it has an increasing cross-sectional contact area. At some time this area will be large enough to support the spring force, and the probe no longer displaces solder so the probe does not travel any further into the solder.

Bead probes also show displacement of solder when contacted by a flat-faced probe. They get a flattened head as shown in Figure 4. This flattening displaces oxide and contaminants and provides good electrical conductivity.

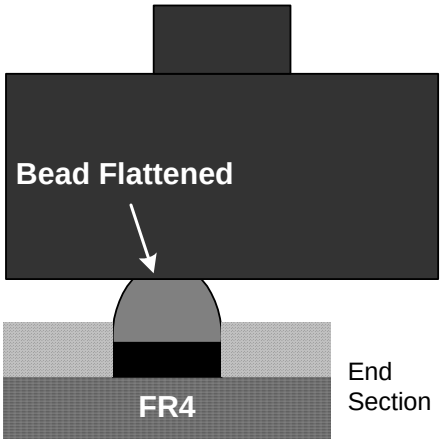

Figure 4 - A Bead Probe Flattens when Contacted

Beads are (approximate) hemi-ellipsoidal structures. When a hard, flat surface is pressed onto them, the initial contact is a point with infinite pressure, so the solder must move. As the surface yields, an area begins to form that is basically an ellipse with a semi-major axis A that runs along the length of the bead, and a semi-minor axis B that runs along the width. The area of the ellipse is πAB. The area continues to increase until it is able to support the spring force. Using the yield strength of solder expressed in ounces per square mil (0.08), we see the areas needed to support a force in the Table 1.

The semi-minor axis of a bead is often constrained to the width of the trace it sits upon. If a bead is too small, the surface area needed to support the spring force might be larger than the bead itself, implying that the bead would be catastrophically crushed out over the solder mask. If the bead is overly large, then the surface yield area may not displace enough solder to move oxides. The semi-minor axis should not exceed 50% of W ($W > 2B$) as shown in Figure 5 as this would imply bead crushing.

Table 1 - Area Need to Support Give Probe Spring Force

Probe spring force (oz)	Area to support force (mil^2)
2	25
4	50
8	100

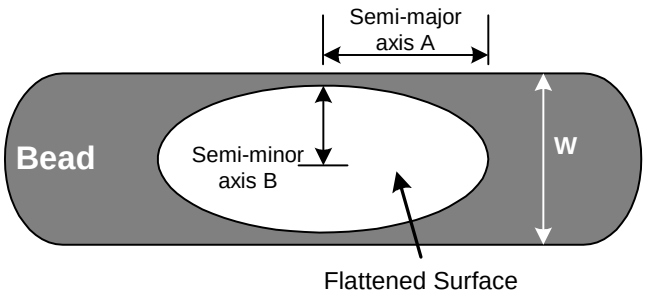

Figure 5 - Top View of a Flattened Bead

Table 2 shows semi-major axis lengths needed to support spring forces for some bead widths and forces. For low spring forces, beads must be very small or there will not be much surface yield on the bead. For all beads, the semi-major axis must be smaller than ½ length of the bead, as was true for the semi-minor axis versus width. Again, using the 50% factor, each bead length should be greater than 2 times the semi-major axis length (L >2A).

Table 2 - Semi-major Axis Lengths needed to Support Spring Forces for Bead Widths

Spring Force (oz)	Bead Width (mils)	Semi-minor axis B (mils)	Semi-major axis A (mils)
2	3	1.5	5.3
	4	2	4
	5	2.5	3.2
4	4	2	8
	6	3	5.3
	8	4	4
8	4	2	16
	6	3	10.6
	8	4	8

Bead widths less than 4 mils will be more difficult to build reliably, since the solder mask registration on a correspondingly narrow trace will become a factor. Also, the width to height ratio will become a factor, since the bead must be tall enough to clear the solder mask by several mils. The solder mask itself supports the sides of a bead, but building tall skinny beads may not be reliable.

Bead Probe Fabrication Experiments

A board containing several types of bead probes was constructed to see how several possible designs would work. Several dozen beads were photographed, and then sectioned and photographed under a microscope where accurate measurements were made. Both virgin beads and probed beads were measured.

Figure 6 shows a newly minted bead from the top, mounted on one of a pair of differential traces with 4 mil line and 6 mil space. The elliptical area surrounding the bead is flux residue (no-clean process).

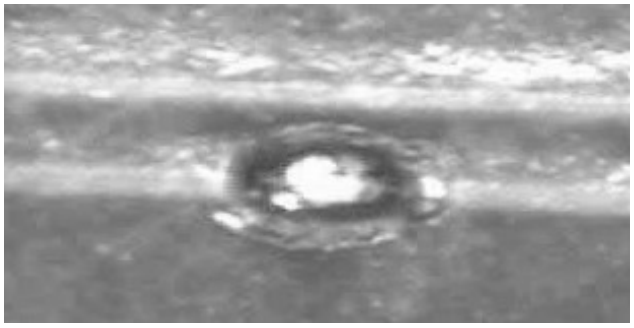

Figure 6 - Photo of a Virgin Bead from the Top, on One Trace of a Differential Pair

Figure 7 shows a section of a bead. At this point the bead was 2.9 mils tall. Other sections of the same bead had heights ranging from 2.3 to 3.7 mils. The width stayed fairly constant. Notice the etching and plating effects (CuNiAu plating) have created a trace with over-etched walls and a mushroom cap.

Figure 8 shows a bead that has been probed ten times with an 8-ounce probe. It looked the same after only one probing. The flattened area has a characteristic shine of clean solder. The area is not very elliptic as theory predicts, but the area is commensurate with theory.

Figure 9 shows a section of a bead that has been probed. The top surface shows the flattening caused by yielding solder.

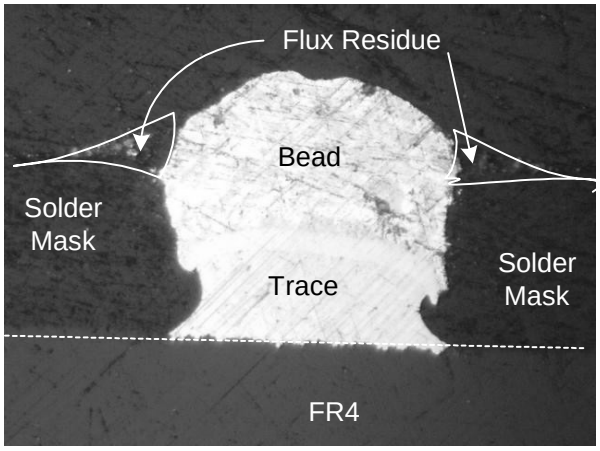

Figure 7 - A Bead, 2.9 mils Tall, and 5.3 mils Wide

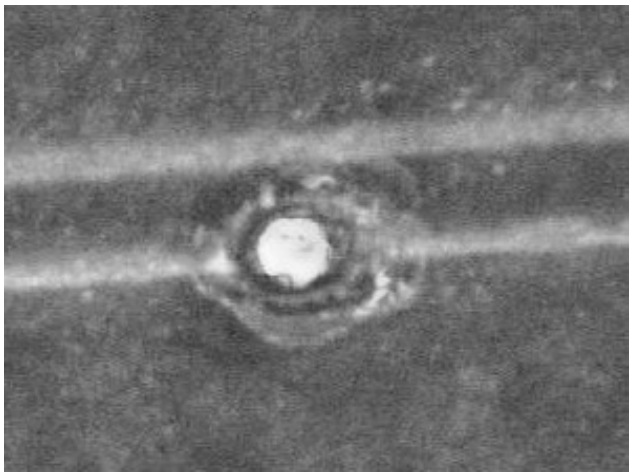

Figure 8 - Topside Photo of a Probed Bead - Note Flattened Surface

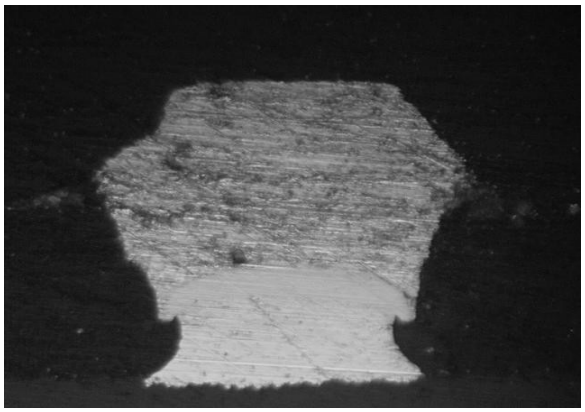

Figure 9 - Cross Section of a Flattened Bead

Probing Performance
A set of 41 beads of varying styles was checked for DC contact impedance using very accurate 4-wire measurements. Each bead's contact resistance was measured ten times in succession. The mean resistance of all the beads was 11.89 milliohms with a sigma of 1.02 milliohms. This compares very well with standard probe contact resistance. There was very little change in the measurements from first to last measurement. These beads had been manufactured in a no-clean process a month earlier so there had been time for some oxidation to occur. However, this was not a controlled part of this experiment.

A question did arise about the subsequent oxidation of a flattened bead. For example, if a board is tested and found faulty, it will go to a repair process. It is reasonable to expect that the repair process might allow time for a new oxide layer to build up. To see if this was the case, the tested board was "soaked" in 95% humidity at 40 degrees C for 48 hours. (The solder was leaded.) The beads were tested again and found to now have 20.60 milliohms of mean contact resistance with 5.25 milliohms sigma.

This rise in contact impedance is a concern. There are several ways to deal with it. One would be to reflow the board before re-testing (which may have been a result of the repair). Reflowing will restore the original shape of each bead. Second would be to chemically remove the oxide, but this seems impractical. Last is to use "twist probes" that twist (say) 45 degrees while being depressed in their sockets. This causes the flat-face probe to wipe the surface of the bead. At this writing, this last idea is being studied.

Finally, a crude life-test was conducted on the beads. Each was probed and re-measured 500 times. A contact was rated marginal if it ever exceeded 100 milliohms. The earliest a probe became marginal was after 38 cycles with a mean of 280 cycles. One type of bead was particularly small and fragile, especially with respect to 8-ounce probe force. When data for this type of bead was removed, the earliest and mean numbers jumped up to 145 and 332 respectively.

High Frequency Characteristics
What is the performance impact of a bead probe at elevated transmission frequencies? Complete details can be found in Parker's paper.[1] In summary, it was found that a good model of a bead is that of a lumped capacitance of about 10 femtofarads on an otherwise ideal transmission line. This value of capacitance is quite small and most designs would consider it negligible. Indeed, a single via along a trace path is often modeled as a 100 fF capacitance, ten times the discontinuity as a single bead probe of about 5x20 mils.

Conclusions from Bead Probe Review
Bead probes are a new ICT probing technique that has negligible effects on the high-speed electrical characteristics of a PCB design. Bead probes can be fabricated using well-understood PCB manufacturing techniques. ICT fixtures can be built with current mechanical tolerances to reliably contact the beads using off-the-shelf or easily adapted probes. Probe resistance and contact reliability are similar to traditional spear probes contacting solder-coated testpads. Testpad layout can be done without affecting the trace layout, significantly simplifying design cycles and improving ICT coverage.

Applying Bead Probes to a Real-Life Product
We were able to add bead probes to a recent PCB design and see if the theoretical benefits of bead probes translate into real-world savings. The board was typical of many of today's PCB designs. While this product did not have gigabit data busses that precluded any testpads, it was an extremely dense design, with limited opportunities for traditional ICT probing locations. Given the tight time-to-market pressures and an outsourced manufacturing strategy, there was great concern that lost ICT access would result in reduced ICT coverage and all its concomitant side effects: slower product ramp, higher warranty costs, more scrap, costly alternate test techniques.

The results are set forth below and focus on three areas—PCB CAD layout, manufacturing issues, ICT testpoint selection.

Bead Probe CAD Issues
Bead probes are built as CAD library elements, like a surface or blind via, to be placed on the top or bottom side of the board. Unlike SMT geometries, which come in all shapes and sizes, historically vias have always been round. Therefore, unlike placing an SMT geometry, there has never been a need to rotate a via when placing it into the CAD data. As a consequence, most popular CAD tools cannot rotate a placed via.

Since the SMT pad portion of a bead probe is abound, it must be rotated to match the direction of the trace onto which the bead probe is placed. This minimizes the parasitic effect on signal bandwidth, capacitance and transmission line impedance. Therefore, we found it necessary to build a separate bead probe via for each direction that the top or bottom side traces can flow. In our case we built both vertical and horizontal bead probe vias. We can also envision a need for 45 degree, and 135 degree angled bead probes to match angled traces, however we found these weren't necessary for our design.

Separate bead probe vias were designed to be placed on 0.005" wide traces, and for traces wider than 0.005", because the solder_mask opening width is different for these two different applications. As it turns out, we did not use any of the wide-trace bead probes in our design.

Also, while building your bead probe via geometries, it is helpful to add targeting circles showing the combination of the diameter of the flat-head probe which will be used, plus, the expected targeting inaccuracy of the probe's pointing vector. The combination of these two numbers represents a circle around which the probe head could 'wander' during probing. We used circles of diameter 0.050" and 0.080" to represent, respectively, the cumulative area that a 0.035" or 0.055" diameter flat-head probe could wander. These circles, then, are used by the PCB layout engineer, to visually ensure that there are no same-sided part bodies or leads within the circle – otherwise the flat-head probes could hit the much higher parts or lead frames long before they could contact the low-profile bead probes. Future improvements in CAD testpoint analyzer tools should be able to automate the checking for this step.

In our application, all of the bead probes were placed on traces on the bottom side of the board. However, if bead probes are required on top of the PCB also, we recommend a separate set of top-sided bead probes, to simplify the via layer mapping rules required to add a blind via to a PCB layout.

Our PCB design was implemented using Mentor Graphics' Boardstation version EN2002. In this CAD tool, you must design the bead probe via geometries using the TERMINAL_BURIED_VIA_DEFINITION property. Also, in the Setup Via Rules menu, you must ensure that the via is designated as what Mentor calls a 'Buried' via, whose mapping goes to the top or bottom layer of the board, as required. Be careful - the hard-to-read underscore ("_") character which Mentor uses to represent the layer mapping for a buried via, is hard to notice if your physical layer names are long.

The last step to building the bead probe vias is to add the diamond-shaped solder stencil opening, so each bead probe will receive exactly the right amount of solder during the solder paste operation, and can then be properly re-flowed in the SMT oven.
Specifying the right solder stencil openings is complicated by the fact that most contract manufacturers (CMs) of printed circuit assemblies (PCAs) prefer to modify and exactly control the actual amount of solder paste deposited to each SMT pin, to maximize solder joint yield – thus they could end up changing the size of your bead probe stencil openings.

Previously, we had specified in our solder stencil Gerber data, how big we thought the solder stencil openings should be, as extracted from our company's CAD parts library. However the CM instead requested that we discard our library's solder stencil opening information, and instead generate solder stencil Gerber data which showed the full outline of each SMT pad – which then allows them to later edit the data, and apply their own proprietary volumetric solder paste reduction algorithms, to reduce the actual stencil openings to a size that matches their process yield. Since the small obround shape of the SMT pad layer of the bead probe vias was completely different from the large diamond-shaped solder stencil openings required for our bead probes, this approach would not work for bead probes.

Subsequently we attempted to work around this problem by adding 'user-defined' layers to the bead probe vias (to reflect the diamond-shaped solder stencil openings) then adding those user-defined layers to the solder stencil Gerber data. Note that our calculation of the size of the diamond-shaped solder stencil openings is dependent on our assumptions on the thickness of the solder stencil. We validated with our CM that a 0.005" thick stencil is acceptable, then specified that thickness in our process requirements document.

Note that our application of bead probe was for improved probing density, not for improved RF performance. Since this was our first attempt to use bead probe, regular test vias were used for about 90% of the nodes. Only when we could not fit in a regular test via, did we add a bead probe. This meant that several of our bead probes violated the large keepout circle to nearest components or lead frames. In the end, the central section of the PCB contained 3600 nets (the board contains 6000 nets total), and of the 3600 nets, 360 were test-pointed with bead probes. Figure 10 shows an image of the PCA. It is 20.5"x16.8", containing 6000 components and 6000 nets. Only the central block of circuits, indicated by the red rectangle, required bead probes. All other areas could be 100% testpointed using traditional test vias.

Figure 11 shows an image of a 'typical' bead probe. Note the obround signal layer, the obround soldermask keepout, the diamond-shaped solder stencil opening, and the two reference circles to show flat-head probe location. The grid is spaced 0.002".

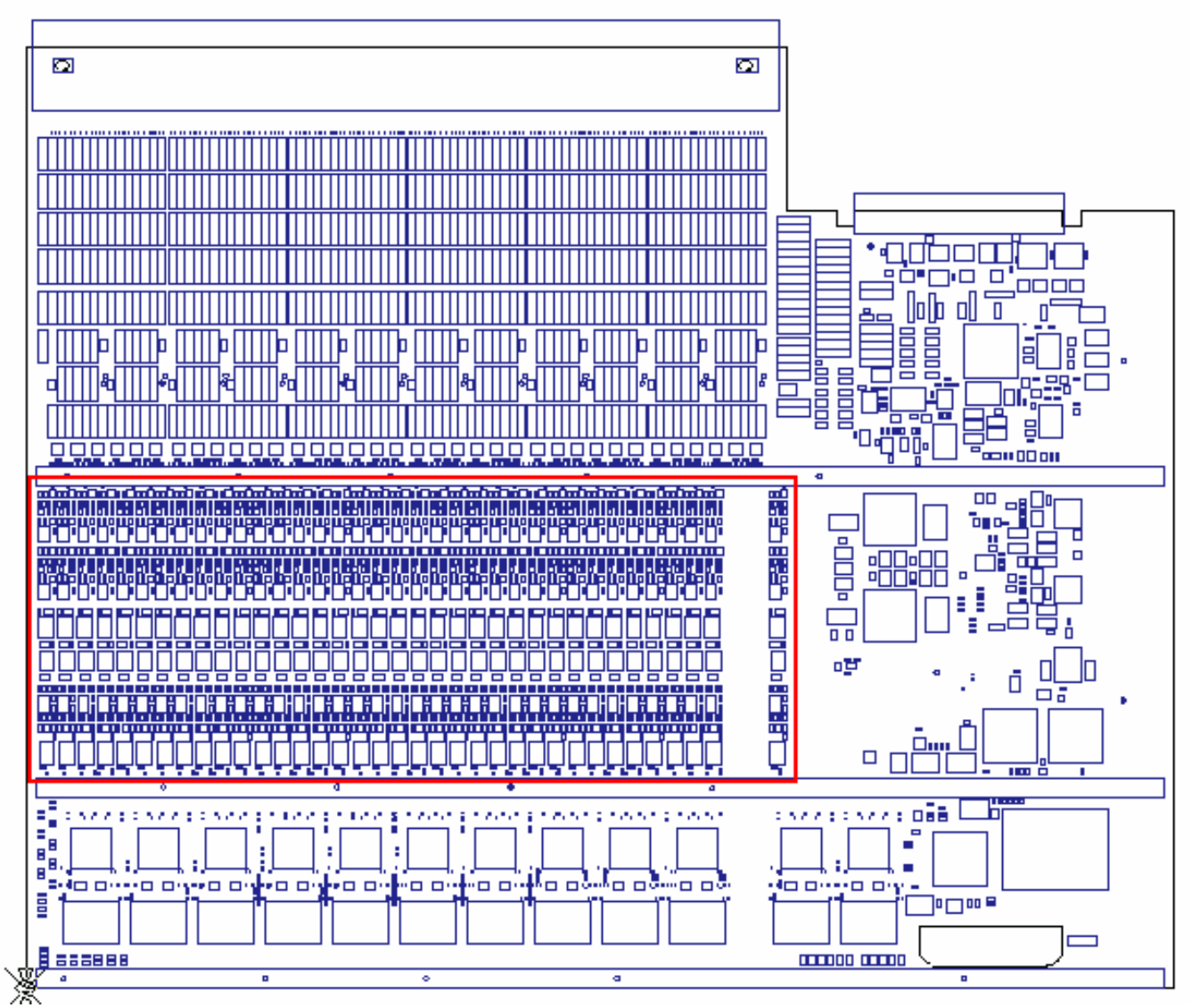

Figure 10 – PCA with Bead Probes

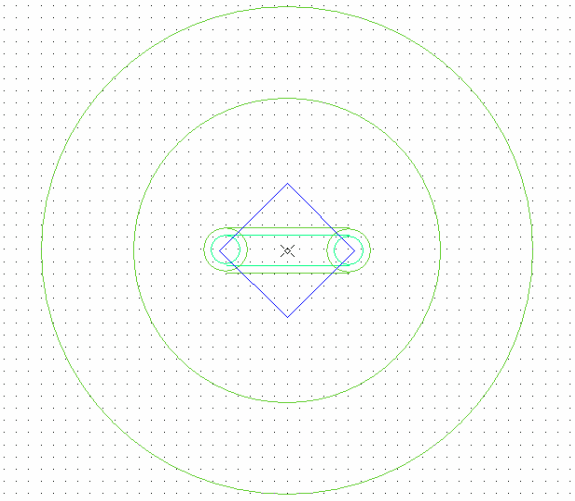

Figure 11 – Typical Bead Probes

Figure 12 shows a typical image of two bead probes added to 0.005” traces on the bottom side of the PCB:

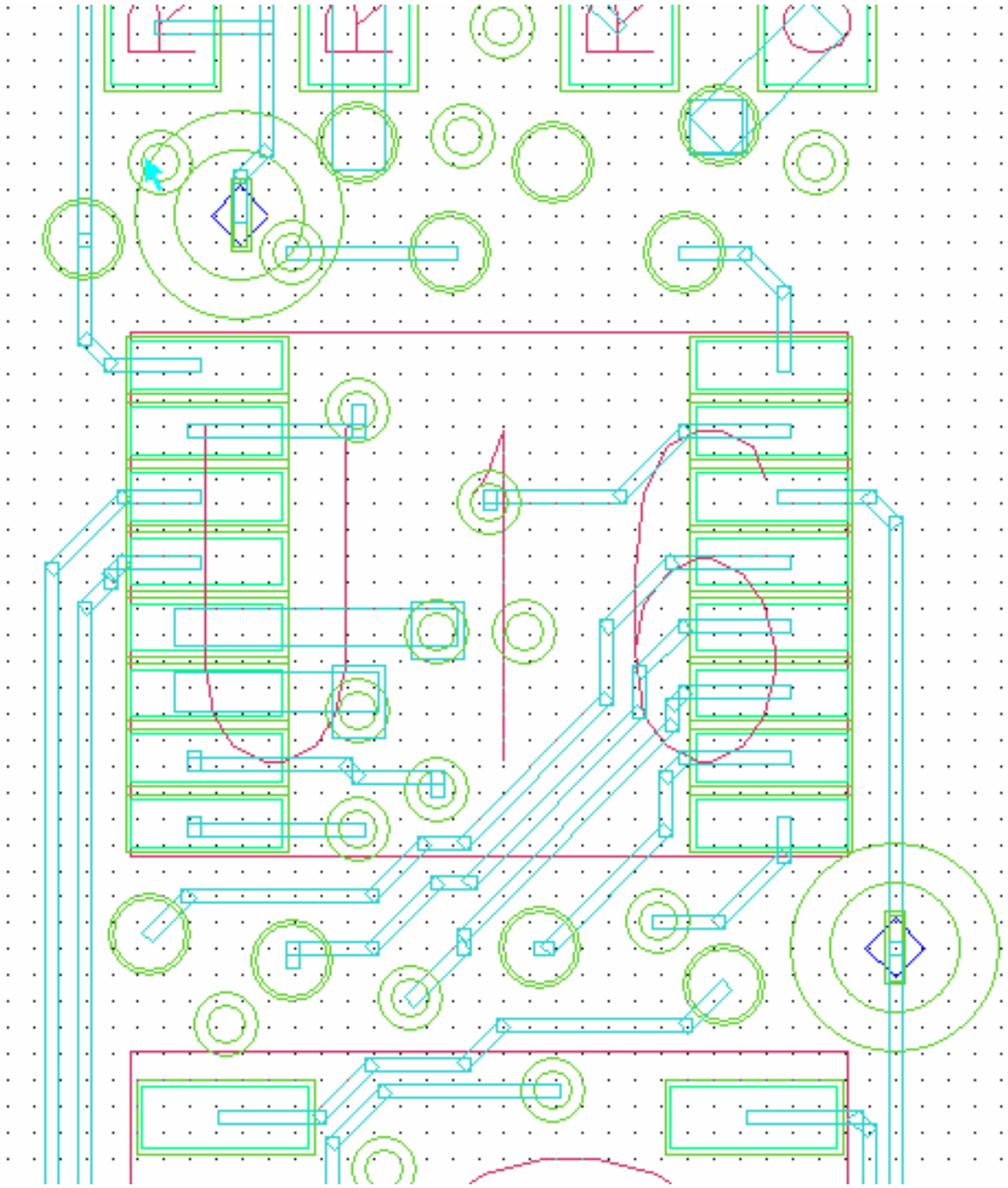

Figure 12 – Two bead probes

The Mentor Graphics ASCII geometry files for our bead probe vias are included in the Appendix.

Bead Probe Manufacturing Issues

We did not notice that the diamond-shaped solder stencil openings for the bead probes, were missing from the solder stencil Gerber data that we delivered to our CM. After having built prototypes, we learned the hard way that Mentor’s BoardStation does not allow user-defined layers to be mapped into Gerber data, for blind vias. As a result, none of the bead probes on those prototypes received any solder during the stencil operation. Without the solder on the bead probes, the bead probes were not probe-able.

As a work-around for the next prototype build, we moved the diamond-shaped solder stencil openings to the unused GLUE_MASK_2 layer (which does map correctly for blind vias), added the GLUE_MASK_2 layer to the artwork order, for generating the solder stencil data, and generated our Gerber data correctly. That is – all of the SMT parts had solder stencil

openings in the Gerber data which were exactly equal to their SMT pad sizes, and all of the bead probes had solder stencil openings that were diamond-shaped openings of the correct size. To reinforce the importance of not changing the size of these diamond-shaped openings, comments were added to the process requirements document, which travels to the CM along with the Gerber data, instructing them to not change the size of the diamonds.

As bad luck would have it, when the second round of prototypes arrived, they too were missing solder from all of the bead probes. In this case we had generated the Gerber data correctly, and the CM had correctly refrained from editing the size of the bead probe solder stencil openings. However the stencil vendor, while studying the solder stencil Gerber data, determined the diamond-shaped openings must be erroneous fiducial openings, and manually deleted them from the stencil data without mentioning it.

ICT Testpad Selection

At this point we have 40 prototypes with un-soldered bead probes, and have started the construction of our ICT fixture. As it turns out, our ICT fixture and test developer happened to have selected only 74 of the 360 bead probes to receive an ICT test probe.

In parallel with developing the ICT fixture, we are having one of the prototypes reworked so that solder is added to the bead probes manually. We are greatly concerned about the repeatability of this process, and the ability to get bead probes with solder neither too tall nor too short. It appears that the most repeatable way to do this, is to add the solder paste to the bead probe using a syringe, then reflow the solder using a low-velocity hot air pen. (High-velocity hot air pens can send the reflowed solder skittering across the PCB, possibly creating solder shorts.)

At this point it is inconclusive whether the hand-reworked prototype will have sufficient solder on the bead probes, for the purpose of ICT test development to use the prototype as a known good board. Given our conservative adoption of this new probing technology, it would only represent a coverage loss of 1.2% (74 bead probe points lost / 6000 total nets) if we could not probe any of the bead probes.

Conclusions

Real-world applications of bead probes are just beginning. In the example above, another round of prototypes are currently being assembled. These should have the missing stencil openings corrected. By the time of the presentation of this paper, the statistical analysis of the efficacy of the bead probes should be available and presented.

Notably, bead probes can be used interchangeably with any existing ICT test technique. Recall that contact resistance is similar to traditional ICT probes at less than 20 milliohms. Therefore, bead probes should be able to be used for:

- Accurate unpowered analog tests requiring low path resistance on sources, inputs, and guards.
- Digital tests for today's low voltage logic families since low path resistance minimizes IR drops when backdriving.
- Delivering current to the DUT without measurable I^2R heating.

In the future, bead probes high-speed electrical transparency and ease with which they can be incorporated on high speed busses means that new ICT techniques need to be developed to obtain coverage for these previously inaccessible nets.

References

1. "A New Probing Technique for High-Speed/High-Density Printed Circuit Boards", K. P. Parker, *Proceedings, International Test Conference*, pp 365-374, Charlotte NC, Oct 2004
2. "Designing SMT Boards for In-Circuit Testability", M. Bullock, *Proceedings, International Test Conference*, pp 606-613, Washington DC, Sept 1987

Appendix

Mentor Graphics ascii geometry files for our four bottom-side bead probes:

```
// file : /users/drv_rcv_4chan/design_geom/bp_horiz_bot
// date : Sunday November 28, 2004; 11:48:26
//
$$lock_windows(@on);
$$create_via("bp_horiz_bot");
$$page(0.0, 0.0, 0.03, @inches, 0.0, 0.0, [0.0,0.0,'VI$bp_horiz_bot'] );
$$point_mode(@vertex);
$$attribute( "TERMINAL_BURIED_VIA_DEFINITION", "");
$$circle( "DAM_2", 0.0, 0.0, 0.05, 0.0);
$$circle( "DAM_2", 0.0, 0.0, 0.08, 0.0);
$$template_line_style( @Solid );
$$path( "PAD_2", 0.005, , [0.01, 0.0, -0.01, 0.0] );
$$path( "SOLDER_MASK_2", 0.0075, , [0.01, 0.0, -0.01, 0.0] );
$$polygon( "GLUE_MASK_2", , [0.0, 0.011, 0.011, 0.0, 0.0, -0.011, -0.011, 0.0] );

// file : /users/drv_rcv_4chan/design_geom/bp_horiz_bot_wide
// date : Sunday November 28, 2004; 11:48:26
//
$$lock_windows(@on);
$$create_via("bp_horiz_bot_wide");
$$page(0.0, 0.0, 0.03, @inches, 0.0, 0.0, [0.0,0.0,'VI$bp_horiz_bot_wide'] );
$$point_mode(@vertex);
$$attribute( "TERMINAL_BURIED_VIA_DEFINITION", "");
$$circle( "DAM_2", 0.0, 0.0, 0.05, 0.0);
$$circle( "DAM_2", 0.0, 0.0, 0.08, 0.0);
$$template_line_style( @Solid );
$$path( "PAD_2", 0.005, , [0.01125, 0.0, -0.01125, 0.0] );
$$path( "SOLDER_MASK_2", 0.005, , [0.01125, 0.0, -0.01125, 0.0] );
$$polygon( "GLUE_MASK_2", , [0.011, 0.0, 0.0, -0.011, -0.011, 0.0, 0.0, 0.011] );

// file : /users/drv_rcv_4chan/design_geom/bp_vert_bot
// date : Sunday November 28, 2004; 11:48:26
//
$$lock_windows(@on);
$$create_via("bp_vert_bot");
$$page(0.0, 0.0, 0.03, @inches, 0.0, 0.0, [0.0,0.0,'VI$bp_vert_bot'] );
$$point_mode(@vertex);
$$attribute( "TERMINAL_BURIED_VIA_DEFINITION", "");
$$circle( "DAM_2", 0.0, 0.0, 0.05, 0.0);
$$circle( "DAM_2", 0.0, 0.0, 0.08, 0.0);
$$template_line_style( @Solid );
$$path( "PAD_2", 0.005, , [0.0, 0.01, 0.0, -0.01] );
$$path( "SOLDER_MASK_2", 0.0075, , [0.0, 0.01, 0.0, -0.01] );
$$polygon( "GLUE_MASK_2", , [0.0, 0.011, 0.011, 0.0, 0.0, -0.011, -0.011, 0.0] );

// file : /users/drv_rcv_4chan/design_geom/bp_vert_bot_wide
// date : Sunday November 28, 2004; 11:48:26
$$lock_windows(@on);
$$create_via("bp_vert_bot_wide");
$$page(0.0, 0.0, 0.03, @inches, 0.0, 0.0, [0.0,0.0,'VI$bp_vert_bot_wide'] );
$$point_mode(@vertex);
$$template_line_style( @Solid );
$$path( "PAD_2", 0.005, , [0.0, 0.01125, 0.0, -0.01125] );
$$attribute( "TERMINAL_BURIED_VIA_DEFINITION", "");
$$circle( "DAM_2", 0.0, 0.0, 0.05, 0.0);
$$circle( "DAM_2", 0.0, 0.0, 0.08, 0.0);
$$path( "SOLDER_MASK_2", 0.005, , [0.0, 0.01125, 0.0, -0.01125] );
$$polygon( "GLUE_MASK_2", , [0.0, 0.011, 0.011, 0.0, 0.0, -0.011, -0.011, 0.0] );
```