Presented in the ECWC 10 Conference at IPC Printed
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Designers Summit 05

Lead Free Flip Chip and Chip Scale Package Inspection: New Challenges Will Require New Inspection Technologies

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Introduction

Lead free implementation will present new challenges for PCB manufacturers from a design, soldering process, and QC standpoint. The higher reflow process temperatures will cause greater thermal stress to the PCB substrate as well as to the components. The smaller soldering process window, which lies between the higher lead free alloy melting point and the maximum allowable component temperature, will make the soldering task more difficult. Specific challenges, however, must be considered in order to guarantee required DPM levels and a minimum of in-field PCB failures. In particular, the very small solder joints found on Flip Chips (FCs) and Chip Scale Packages (CSPs) will see a great deal more thermal stress during the lead free soldering process, which can result in fatal defects. This paper will discuss the existing problem of topside ball delamination for the area array packages FCs and CSPs by highlighting passages from recent research publications. The research shown presents important failure analysis data relating to FC and CSP reliability in both a tin-lead and a lead free soldering process. Finally, an introduction of a new optical inspection technology designed to detect such defects in a non-destructive manner will be made.

The internal designs of FCs and CSPs vary greatly from manufacturer to manufacturer. Two internal designs can be seen in Figures 1 and 2 below.

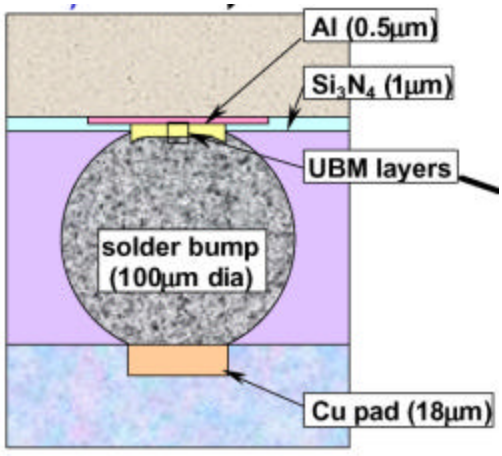

Figure 1 – Flip Chip

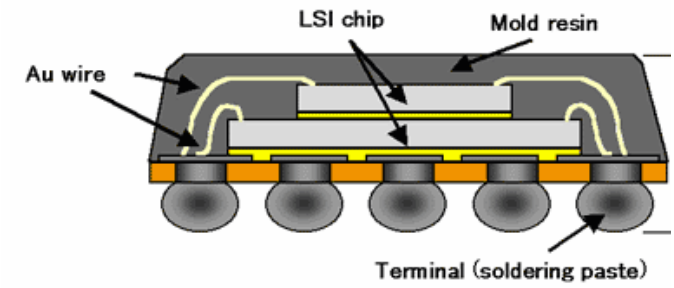

Figure 2 – Chip Scale Package

In any case, the extremely small component side joints of an FC or CSP are at greater risk of failing under mechanical stress. Professor Toshio Nakamura and Gary Yu Gu have conducted extensive research aimed at understanding the failure mechanism by identifying likely fracture modes and potential delamination sites in flip chip packages. Their research entitled **"Mechanical Behaviours of Flip-Chip Packaging"** clearly shows that the upper solder connection is at greater risk of delamination as seen in Figures 3 and 4 below.

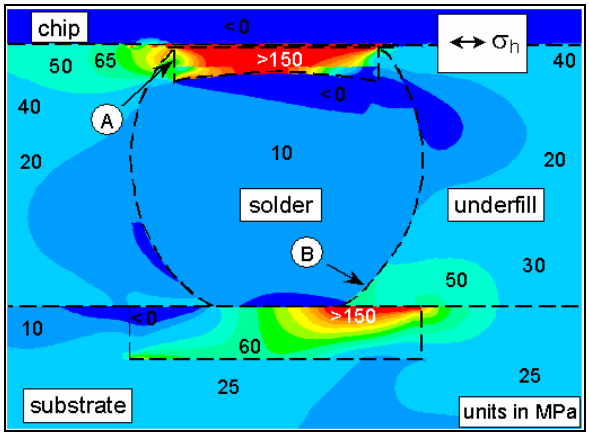

Figure 3 – Cell Analysis – Possible Failure Interface 1

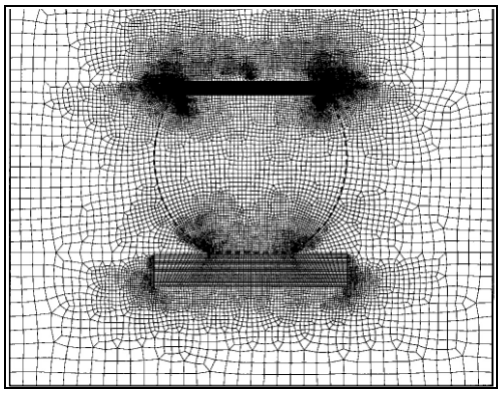

Figure 4 – Cell Analysis – Possible Failure Interface 2
Red colour indicates maximum stress area. Dark colour indicates maximum stress area.

In the publication, **"Mechanical Reliability of Underfilled CSP Assemblies"** by Murtuza Rampurawala, Michael Meilunas, and Arun Gowda & K. Srihari, Ph.D., the authors call attention to the problem of top side ball delamination of CSP joints:

The authors note that, "Cross sectional analysis of failed assemblies found cracks within the solder joint along the component side of the assembly. Figure 5 shows an image of a non-underfilled sample of Package H that failed in torsional testing. **The crack initiated from the interface of the solder mask and the pad of the component**. Figure 6 shows a cross-section of Package D, underfilled using UF1, which failed after 1825 torsion cycles."

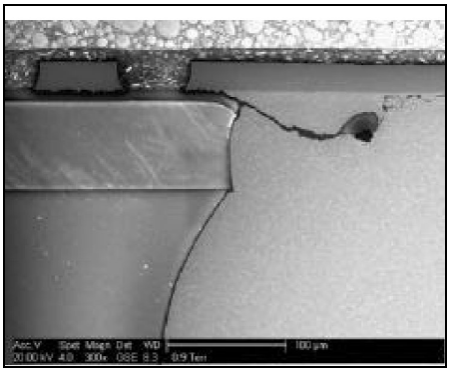

Figure 5 – Failed Non-underfilled Assembly of Package H

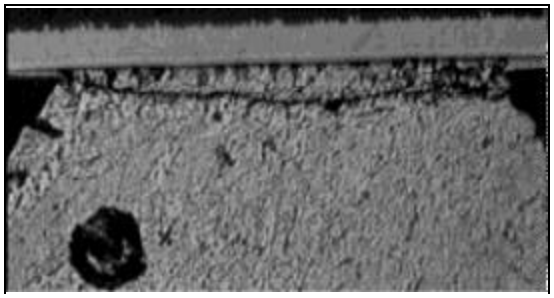

Figure 6 –Cross-sectional Image of Failed Package D Assembly (UF1)

Underfill is used for FCs and some CSPs in order to mechanically strengthen the joint after soldering. If delamination occurs before the underfill process and is not detected, this will cause an early in-field failure. Many area array packages to include CSPs, use an interposer which compensates for the internal tension in a solder joint which is created by CTE (Coefficient of Thermal Expansion) mismatch during the heating and cooling process. The general problem with CTE mismatch is illustrated in Figure 7 below. Due to the fact that the CTE from the PCB substrate and the component body (e.g. 18 ppm/°C for FR4 and 2,8 ppm/°C for the Si chip. See ref. 2.) are not the same, there is a relative movement differential between the expanding materials which increases at higher process temperatures. During cooling, there is a relative movement differential between the contracting materials which can cause a shearing when the solder ball solidifies.

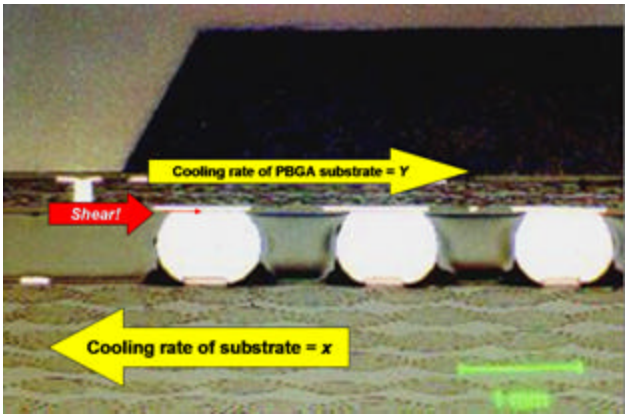

Figure 7 - Cross Section of BGA Revealing Shearing Zone

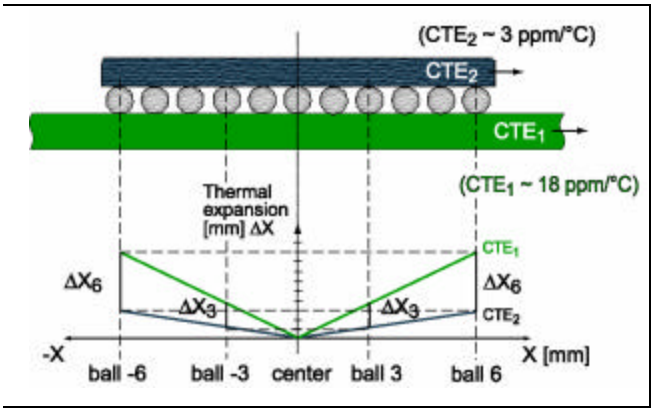

Figure 8 - Corner Balls are at Greater Risk Caused by CTE Mismatch during Cooling Delamination caused by CTE Mismatch

Figure 8 addresses the fact that this movement is greater at the corners of the component. Considering the component from the center outwards, the relative movement at the center ball is "0". As we move towards the corners of the package, the relative movement differential increases as the distance from the center point increases. The differential is greater at Ball 6 (ΔX_6), for example, than at Ball 3 (ΔX_3). During cooling the materials contract and the relative movement between the PCB and the component is impeded by the solidification of the solder. As all materials will assume their original position at room temperature, a residual sheer stress will remain in the solder joint. This stress is substantially larger at the corners of the component and can result in micro crack formation. For this reason, it is essential that PCB design engineers choose the right material combinations with respect to their CTE mismatch.

In their research entitled, **"3D Interfacial Delamination Near Solder Bumps in Flip-Chip Package,"** the authors Yu Gu and Toshio Nakamura underscore this issue of increased stress at the corners of the package. Figure 9 below reveals that there is increasing shear strain from the center to the edge, and that out-of-plane shear strain is larger near the edges of the component.

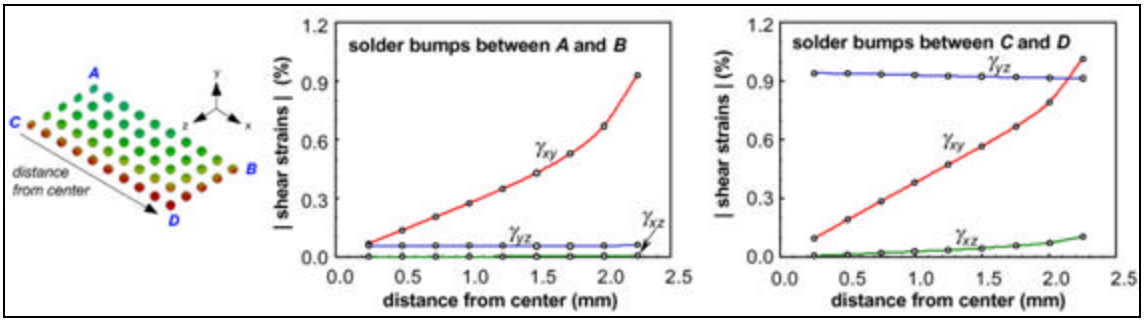

Figure 9 - Increased Shear Strain at Corner Balls

This analysis of the problems of increased corner ball stress as it relates to area array packages, especially in a lead free process is clearly supported in the publication entitled, "**HDPUG's Failure Analysis of High-Density Packages' Lead-Free Solder Joints**".

As stated in the article: "It can be seen that due to the higher lead free reflow temperatures, the package is warped severely, leading to the anomalous-shape solder joints near the corner and fatter than normal shape solder joints near the middle. The failure locations of the solder joints of the package are near the corners of the outer, inner, and the thermal ball arrays. **This is due to the global thermal expansion mismatch between the package (silicon chip, molding compound, and BT (bismaleimide triazene) substrate and the PCB, and the local thermal expansion mismatch between the silicon chip, the BT substrate, and the molding compound." Figures 21 and 25 from that reference (see below) illustrate the issue.**

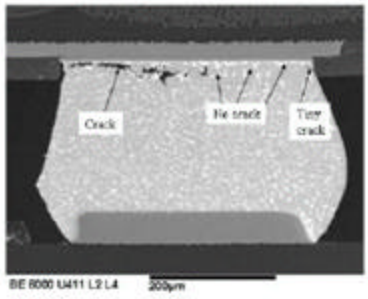

Figure 21 - SnPb Solder Balled 208PBGA with SnAgCu Solder Paste on NiAu PCB (Not Fracture Yet)

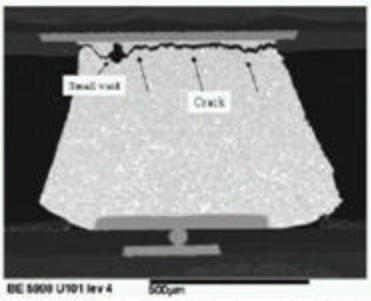

Figure 25 - Failed SnPb Solder Balled 388PBGA with SnAgCu Solder Paste on OSP PCB (At the Corner of an Outer Row of Solder Joints)

How does Lead Free increase the Risk of Solder Joint Failure?

The basic problems associated with FC and CSP solder joints as discussed above are amplified in a lead free process due to three essential factors: 1. the process temperatures for lead free is higher, 2. the temperature that a lead free solder joint solidifies is much higher and closer to the peak reflow temperature than with SnPb, and 3. the effects of CTE mismatch are amplified at higher temperatures. Figure 10 below identifies the problems in more detail.

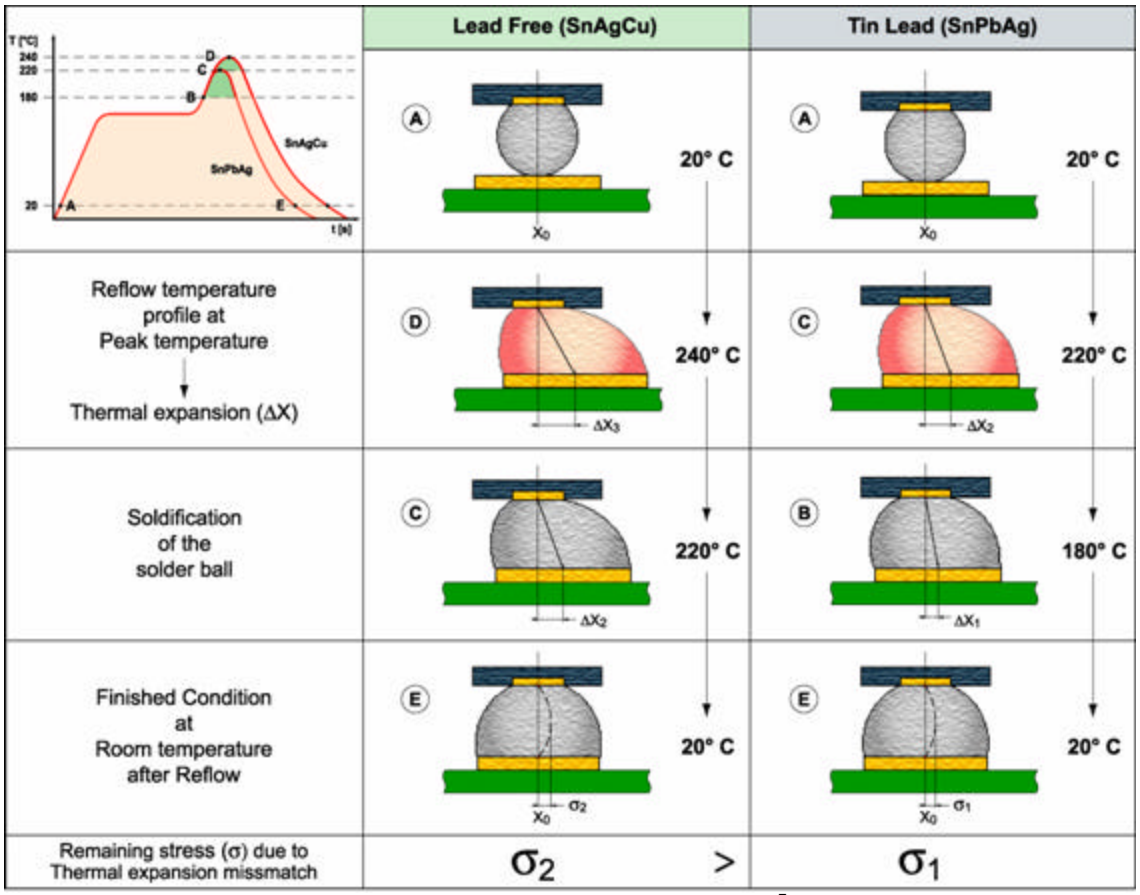

Figure 10 – Problems of CTE Mismatch [7]

The start up condition in both processes is the same at room temperature (A). As the assembly heats up in a reflow process, the relative expansion differential (ΔX_3) in a lead free process is greater at the higher peak temperature (D), than the relative expansion (ΔX_2) in a tin-lead process at its peak temperature (C). At position (C) in the temperature profile, the lead free alloy solidifies at position ΔX_2, whereas the tin-lead alloy is at its peak temperature. Therefore, during cooling, the contraction of the materials in the tin-lead process, takes place longer in a fluid or flexible state, and can move back to position (ΔX_1) at the ball solidification point (B). When all materials move back to their original positions (X_0) at room temperature (E), the remaining stress ($\sigma 2$) in the lead free solder joint is greater than ($\sigma 1$) in the tin-lead solder joint. It should be understood that the remaining stress (σ) can result in a shearing or delamination even during the first production reflow cycle. Proper inspection techniques should allow for the discovery and correction of such defects before they become costly in-field failures.

In the paper, **"Reliability of Lead-Free Solder Connections for Area-Array Packages"** by Ahmer Syed, Amkor Technology, Inc, the author clearly underscores the top side delamination problem as it relates to the lead free process: "The failures reported above were analyzed with dye and pry and cross-sectioning techniques. **Overall, it was found that solder joint failure for all of these Pb free alloys occur at the package side of the joint** as is the case for Sn/Pb alloy." A representative x-section of joints with Sn/Pb and Sn/Ag/Cu alloys is shown in Figure 11.

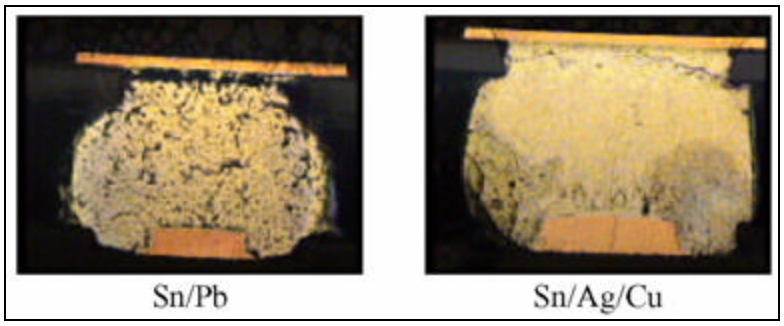

Figure 11 - Cracked Solder Joints for Sn/Pb and Sn/Ag/Cu Alloys due to Temperature Cycling

In a more recent publication**, "Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints"**, Mr. Ahmer Syed further underscored this problem: "**In all cases reported here, the solder joints failed at package interface. Figure 2 shows a typical cross-section of failed joint showing crack very close to intermetallic on package side." Figure 2 from that reference is reproduced below as Figure 12.**

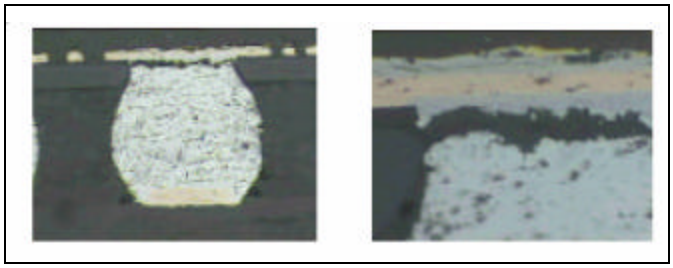

Figure 12 - Typical failed SnAgCu Solder Joint Cross-Section

In summary, given the CTE mismatch problems, and considering the fact that corner joints of an area array package have greater stress, it is clear that the lead free process for FCs and CSPs will realize a much greater danger for top side ball delamination. The excerpts from the research highlighted in the articles noted above clearly underscores the problems associated with component side delamination on a variety of FC and CSP devices. Greater care must be taken, therefore, during both the PCB design and production phases in order to minimize this problem. Most importantly, however, first article inspection procedures must be implemented in order to discover these fatal errors before they end up as costly in-field failures.

Inspection Equipment must allow for the Non-Destructive Discovery of Such Defects

Area array packages in general, and FC and CSP packages in particular, have presented great challenges for inspection equipment. The problem lies simply in the fact that the solder connections are both extremely small and are hidden under the package. The cross sectioning of such devices is a timely and costly undertaking, but can offer the necessary failure analysis information in order to understand and correct process or material problems. This destructive method, however, cannot be used on all PCBs. In the past 10 years, as area array packages have been taking over as a major SMD of choice, manufacturers have been using X ray technology for non-destructive inspection purposes both in and off line. X ray technology has proven its usefulness in the discovery of the typical problems such as voids, misalignments, opens and shorts. Additionally, this technology is continuing to increase its effectiveness, particularly from a magnification and resolution standpoint. Three factors, however, can make the use of this technology at times somewhat limiting;

1. proper interpretation of the image data
2. the ability to "see" particular defects, such as delamination in the form of micro cracks
3. the cost of high end equipment.

The specific problem as discussed in this article of top side ball delamination of lead free FC and CSP solder joints, can present difficulties for even the best 3D X ray equipment.

Since its introduction to the market in 1999, manual BGA optical inspection equipment has become a state of the art supplement to off line X ray systems. Until now, however, its limitation lied in the fact that the optical system could inspect only the bottom side joint of low profile packages such as micro BGAs, FCs and CSPs. In other words, the acute problem of top side ball delamination of FCs and CSPs, as discussed in this article, could not be properly inspected by existing BGA optical inspection systems. The recent introduction of a newly designed Flip Chip optical inspection system, now makes the visual inspection of the critical defect area possible, and is a cost effective alternative to destructive methods.

Low profile CSPs and FCs will require the improved inspection capabilities of a newly engineered Flip Chip optical head designed for visual inspection. The iris of the original BGA optical inspection system sits approximately 0.30 mm from the surface of the PCB. This provides a "look down image," as seen in Figure 13, of a Flip Chip whose standoff or gap height is only 0.05mm. The new Flip Chip optical head has now lowered the iris to approximately 0.015mm. This means that it is now possible to "look up," as seen in Figure 14, at even the top side of the Flip Chip joint in order to defect possible defects such as top side delamination. This critical topside fillet of FCs and CSPs was never before seen by any BGA optical inspection equipment on the market.

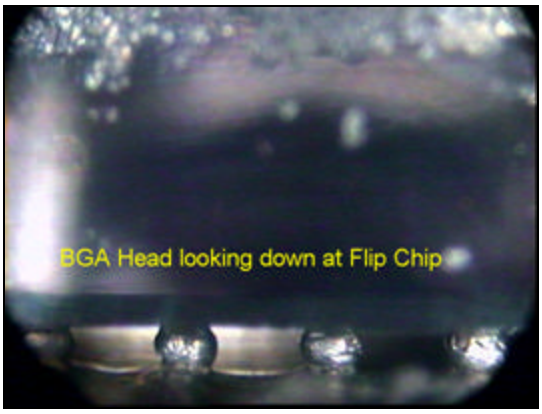

Figure 13 - Standard BGA Optics Look Down at Bottom Fillet

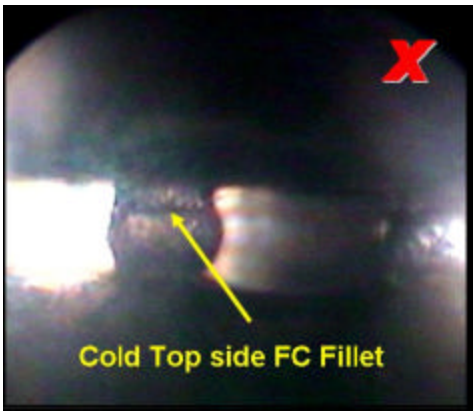

Figure 14 - New FC Optics Look Up at Top Side Fillet

Figures 15, 16 and 17 reveal the importance of this optical innovation by discovering precisely the problem outlined in this paper of topside fillet delamination of a low profile micro BGA.

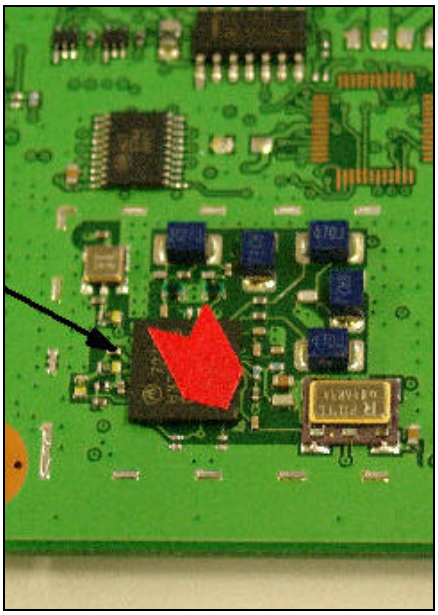

Figure 15 – Micro BGA

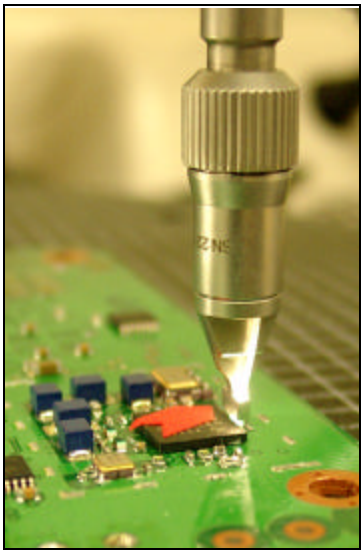

Figure 16 – New FC Optical Head

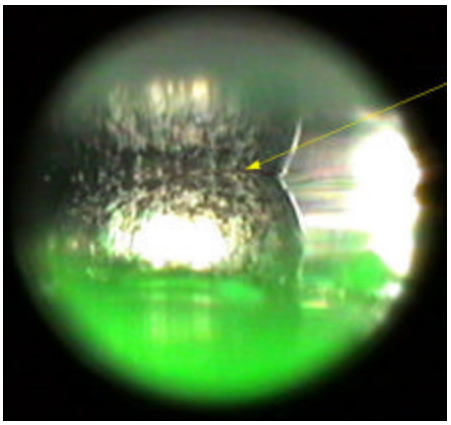

Figure 17 – Corner Ball of BGA Delaminated

Based on the extremely low iris, the new Flip Chip optic (Figure 16) even allows for the inspection of interior top side fillet problems in the middle of the component, as seen in Figures 18 and 19, which were taken from the same micro BGA (Figure 15).

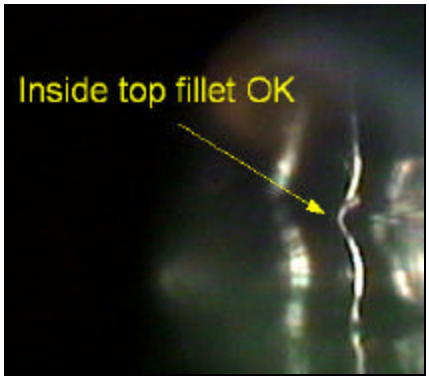

Figure 18 – Interior top Side Fillet OK

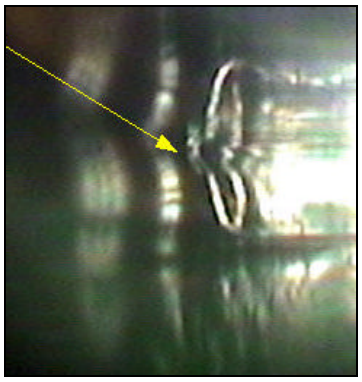

Figure 19 – Interior Top Side Fillet Deformed

The Flip Chip optical inspection system has successfully been used to discover critical defects in a lead free CSP production. The top side fillets of a low profile lead free CSP seen below reveals that the middle ball in Figure 20 has a proper top side fillet, whereas the left side corner ball in Figure 21 shows obvious delamination.

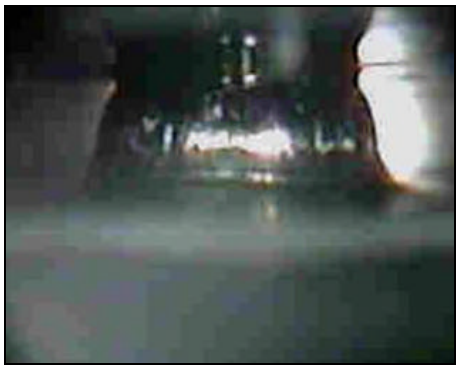

Figure 20 – Interior Top Side Fillet OK

Figure 21 – Interior Top side Fillet Delaminated

As clearly mentioned above, X ray inspection is state of the art and is a necessary technology for the non-destructive inspection of PCBs. The particular defect of top side delamination, however, is very difficult or impossible to detect with X ray technology, as can be seen in the images below. Figure 22 was taken with the new Flip Chip optic, whereas Figure 23 was taken with a state of the art X ray machine.

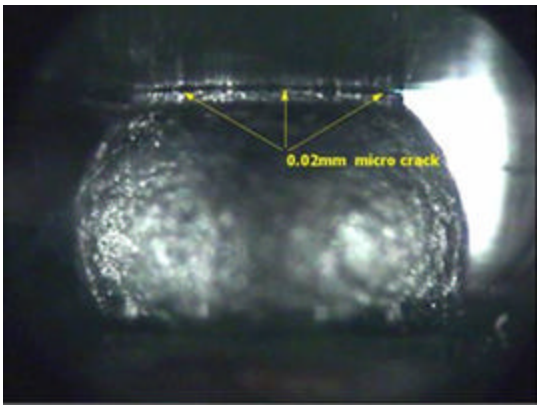

Figure 22 – Top Side Delamination Visible

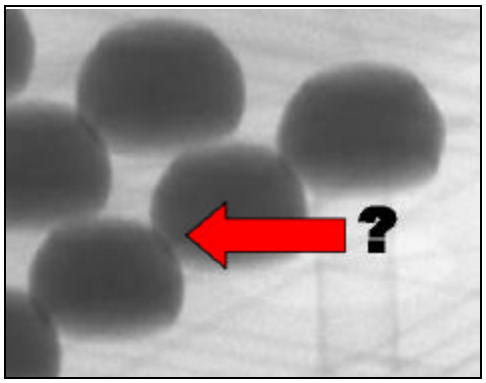

Figure 23 – X-ray Image of Same Defect difficult to Detect

It is clear from these images, that the X ray system alone was not capable of discovering this top side delamination, which resulted in a 0.02mm micro crack on the lead free micro BGA shown above. The use of such an optical inspection system that can compliment X ray, especially in a lead free environment, should be considered as a sensible requirement.

Conclusion

This paper has highlighted a very specific defect of component side ball delamination of area array packages, in particular FCs and CSPs, by examining and summarizing current research available on this critical subject. It has become clear that the lead free soldering process will create new process challenges for these components. Simply put, the existing problems of component side delamination will be exacerbated in a lead free process. With this knowledge, therefore, it is essential to implement proper inspection and test procedures in order to guarantee a quality lead free FC and CSP soldering process. Failure to discover such fatal process defects, as highlighted above, will result in in-field failures, and will generate unnecessary warranty and repair costs. PCB manufacturers implementing lead free and using low profile area array packages such as FCs and CSPs should consider using new optical inspection technologies designed to detect these very specific defects in a non-destructive manner as a supplement to their current equipment. The implementation of thorough First Article Inspection procedures with newly designed inspection equipment is a cost effective alternative to the high costs of destructive methods, or the even higher costs of non-discovery of fatal defects. Properly informed and properly equipped, these challenges for FC and CSP production should be seen as a new opportunity to increase process quality, and increase product reliability in the lead free future.

References

1. “Mechanical Behaviors of Flip-Chip Packaging” by Professor Toshio Nakamura and Gary Yu Gu
2. “3D Interfacial Delamination Near Solder Bumps in Flip-Chip Package” by Yu Gu and Toshio Nakamura
3. “MECHANICAL RELIABILITY OF UNDERFILLED CSP ASSEMBLIES” by Murtuza Rampurawala, Michael Meilunas, and Arun Gowda & K. Srihari, Ph.D.
4. “HDPUG's Failure Analysis of High-Density Packages’ Lead-Free Solder Joints”, by John Lau, Agilent Technologies, Dongkai Shangguan, Flextronics, Todd Castello, Flextronics, Rob Horsley, Celestica, Joe Smetana, Alcatel, Nick Hoo, Tin Technology, Walter Dauksher, Agilent Technologies, Dave Love, Sun Microsystems, Irv Menis, IBM, and Bob Sullivan, HDPUG
5. “Reliability of Lead-Free Solder Connections for Area-Array Packages” by Ahm er Syed, Amkor Technology, Inc
6. “Accumulated Creep Strain and Energy Density Based Thermal Fatigue Life Prediction Models for SnAgCu Solder Joints”, Ahmer Syed, Amkor Technology, Inc
7. Figure 10: source: ERSA GmbH

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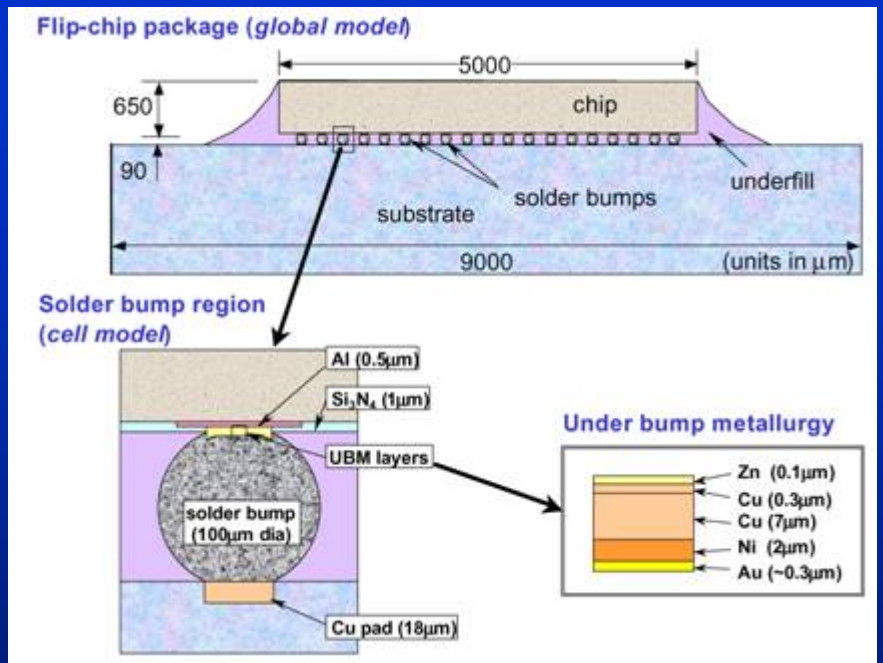
New Challenges Will Require New Inspection Technologies

By Mark Cannon
President and Chief Operating Officer
ERSA GmbH

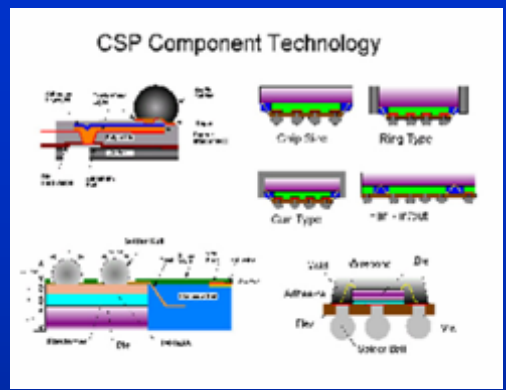
APEX 2005

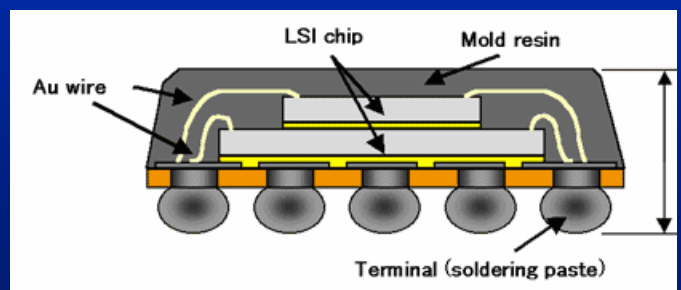
Flip Chip & CSP Package Designs….

Although component designs vary between manufacturers,



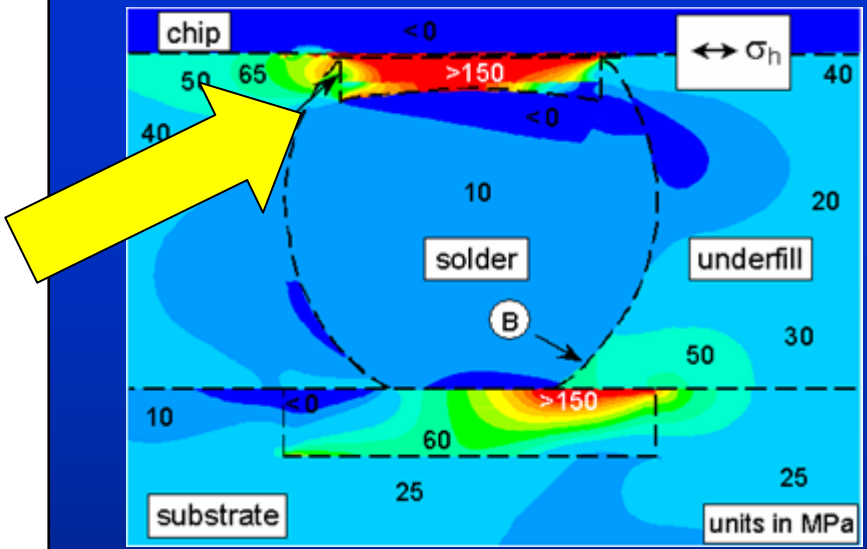
Source: 3D Interfacial Delamination Near Solder Bumps in Flip-Chip Package, by Yu Gu and Toshio Nakamura

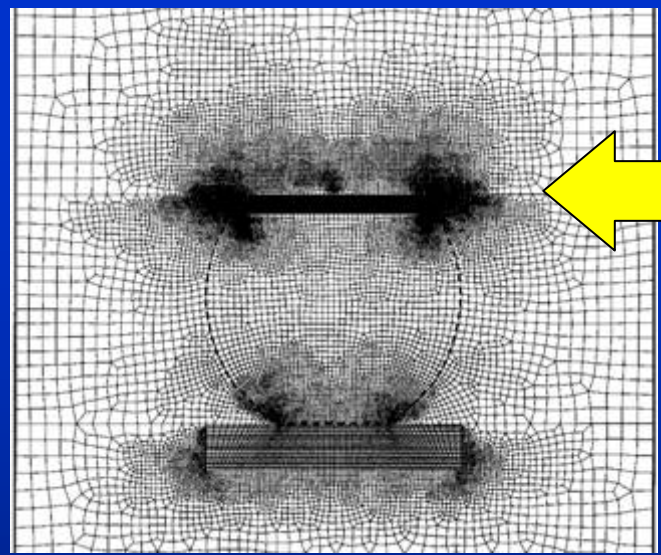




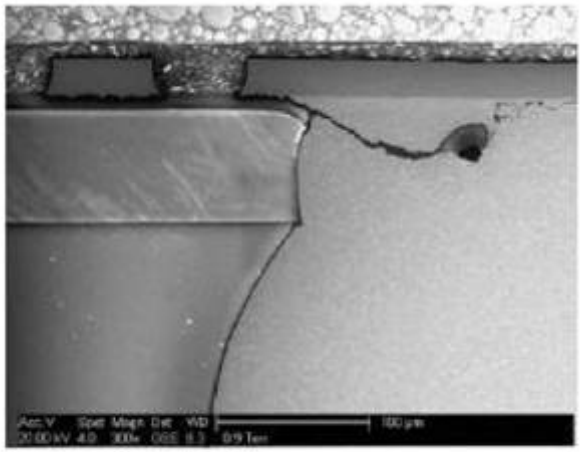
one fact remains; the size of the soldered connection is extremely small and is mechanically a weak point!

“Mechanical Behavior of Flip Chip Packaging” by Professor Toshio Nakamura and Gary Yu Gu

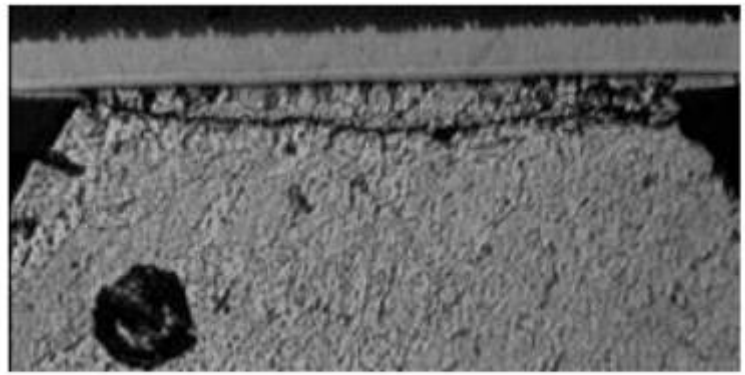




Professor Toshio Nakamura and Gary Yu Gu have conducted extensive research aimed at understanding the failure mechanism by identifying likely fracture modes and potential delamination sites in flip chip packages. Their research clearly shows that the upper solder connection is at greater risk of delamination as seen in the possible failure interface of the cell analysis figures above.



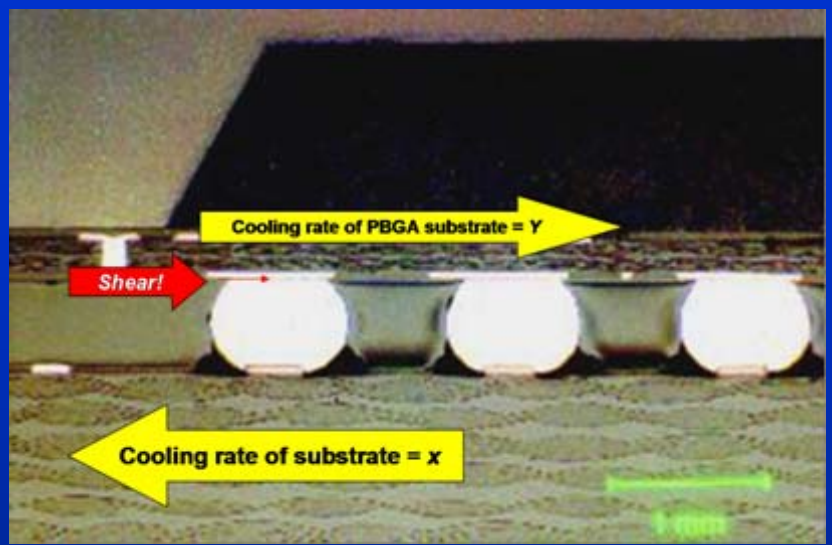
Failed Non-underfilled Assembly of Package H



Cross-sectional Image of Failed Package D Assembly (UF1)

Crosssectional analysis of failed assemblies found cracks within the solder joint along the component side of the assembly. Figure 5 shows an image of a non-underfilled sample of Package H that failed in torsional testing. The crack initiated from the interface of the solder mask and the pad of the component. Figure 6 shows a cross-section of Package D, underfilled using UF1, which failed after 1825 torsion cycles.

Coefficient of Thermal Expansion (CTE) Mismatch (1)

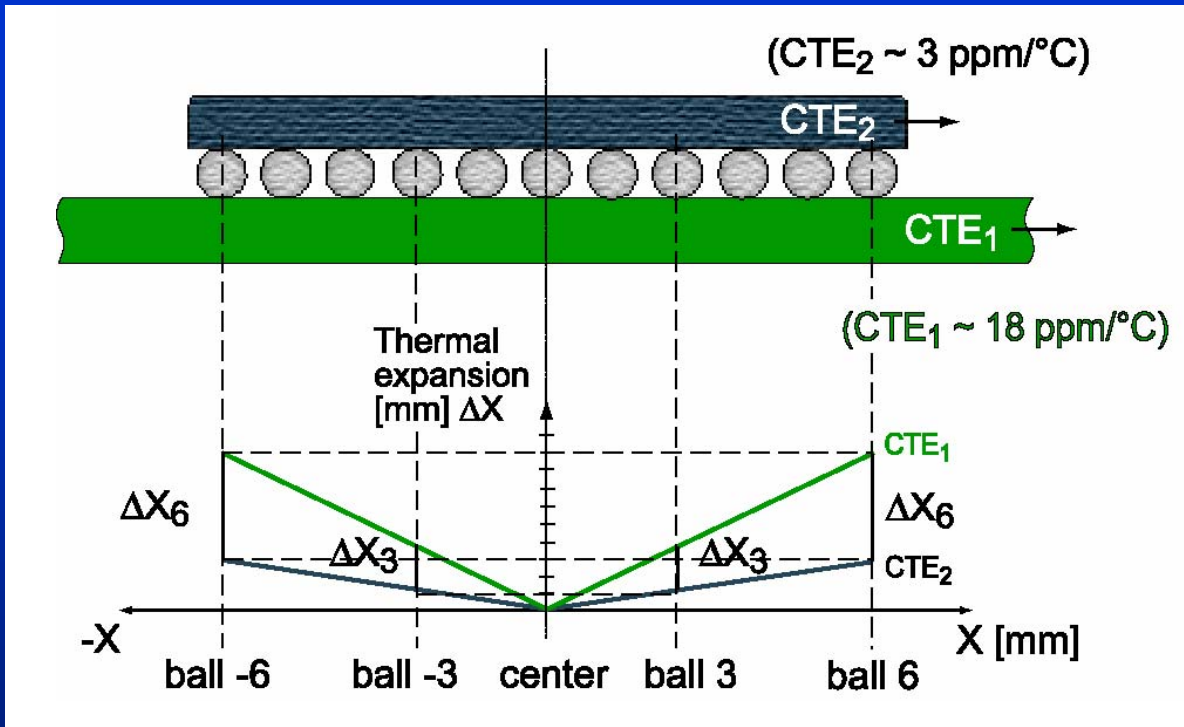


Materials	CTE (ppm/°C)	E (GPa)
chip (Si)	2.8	131
passivation (Si_3N_4)	2.9	325
bond pad (Al)	23.2	70
UBM layer 1 (Cu)	16	117
UBM layer 2 (Ni)	12.7	200
solder bump (63Sn/37Pb)	21	30
underfill (FP2546)	33	8.5
substrate (FR4)	18	22

Source: 3D Interfacial Delamination Near Solder Bumps in Flip-Chip Package, by Yu Gu and Toshio Nakamura

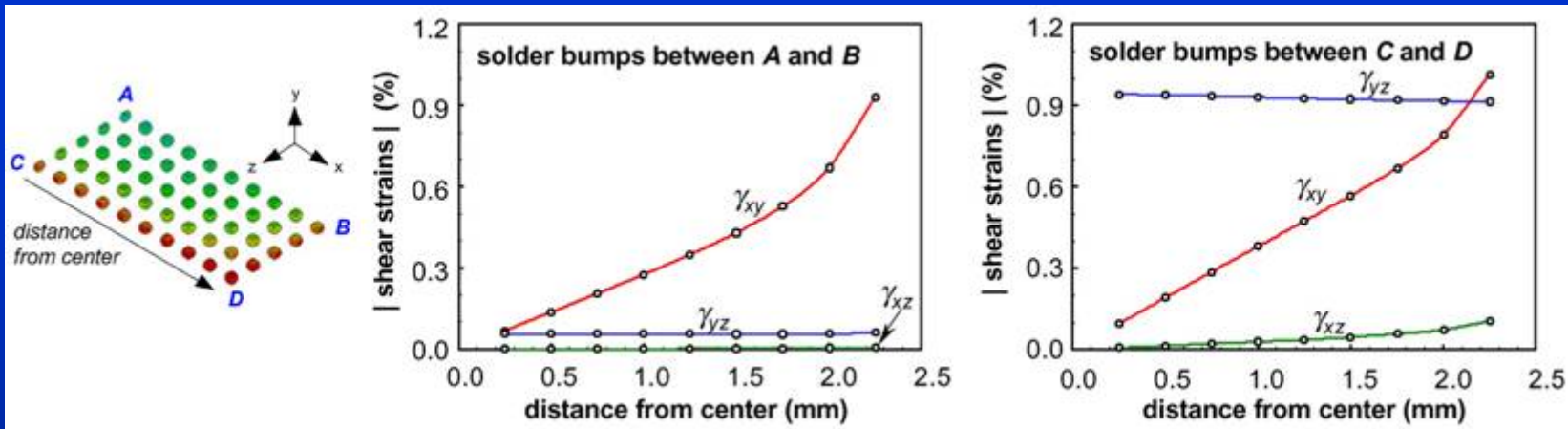
CTE from the PCB substrate (x) and the component body (y) are not the same, there is a relative movement differential between the expanding materials which increases at higher process temperatures. During cooling, there is a relative movement differential between the contracting materials which can cause a shearing.

Coefficient of Thermal Expansion (CTE) Mismatch (2)



As we move towards the corners of the package, the relative movement differential increases as the distance from the center point increases. This stress is substantially larger at the corners of the component and can result in increased micro crack formation at the corner joints.

Shear Strain at corners of Flip Chip



Source: 3D Interfacial Delamination Near Solder Bumps in Flip-Chip Package, by Yu Gu and Professor Toshio Nakamura

The figure above reveals that there is increasing shear strain from the center to the edge, and that out-of-plane shear strain is larger near the edges of the component.

Lead Free Reflow First Article Inspection

How does Lead Free change my inspection process?

How does lead free increase the risk of joint failure?

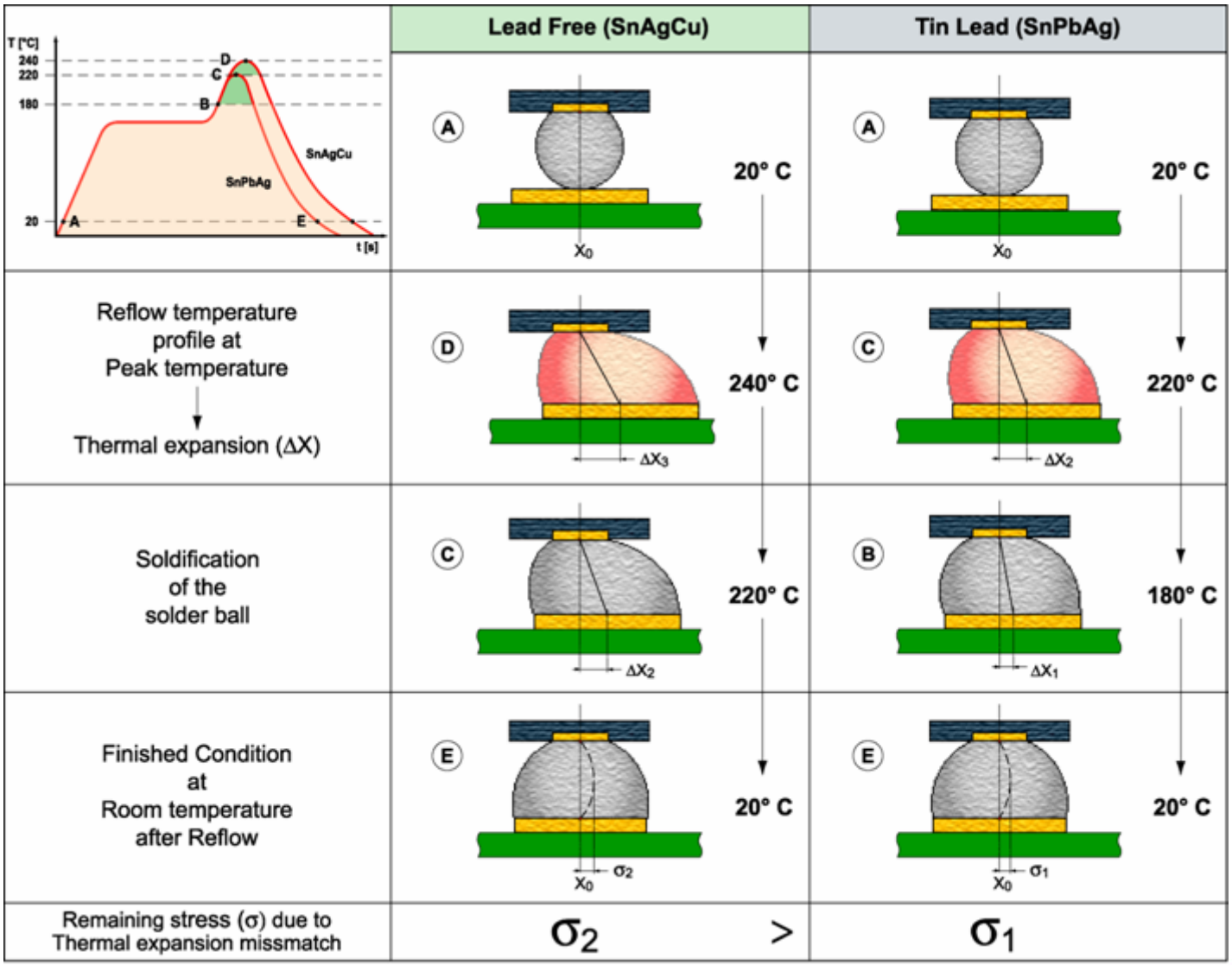
The basic problems associated with FC and CSP solder joints are amplified in a lead free process due to three essential factors:

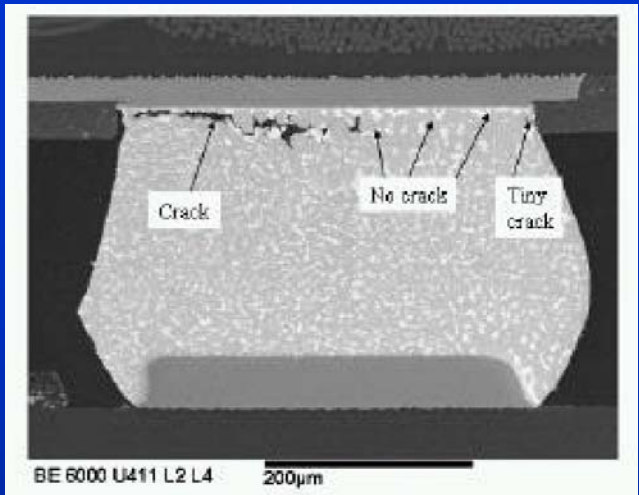
1. the process temperatures for lead free is higher,

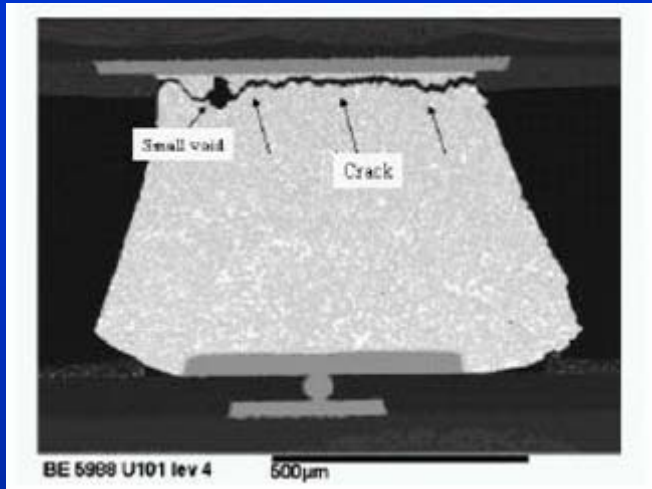
2. the temperature that a lead free solder joint solidifies is much higher and closer to the peak reflow temperature than with SnPb,

3. the effects of CTE mismatch are amplified at higher temperatures.

How does lead free increase the risk of solder joint failure?







“It can be seen that due to the higher leadfree reflow temperatures, the package is warped severely, leading to the anomalous-shape solder joints near the corner and fatter than normal shape solder joints near the middle. The failure locations of the solder joints of the package are near the corners of the outer, inner, and the thermal ball arrays. This is due to the global thermal expansion mismatch between the package (silicon chip, molding compound, and BT substrate and the PCB, and the local thermal expansion mismatch between the silicon chip, the BT substrate, and the molding compound.”

Sn/Pb

Sn/Ag/Cu

Figure 9 - Cracked Solder Joints for Sn/Pb and Sn/Ag/Cu Alloys due to Temperature Cycling

“The failures reported above were analyzed with dye and pry and cross-sectioning techniques. Overall, it was found that solder joint failure for all of these Pb free alloys occur at the package side of the joint as is the case for Sn/Pb alloy. A representative x-section of joints with Sn/Pb and Sn/Ag/Cu alloys is shown in Figure 9.”

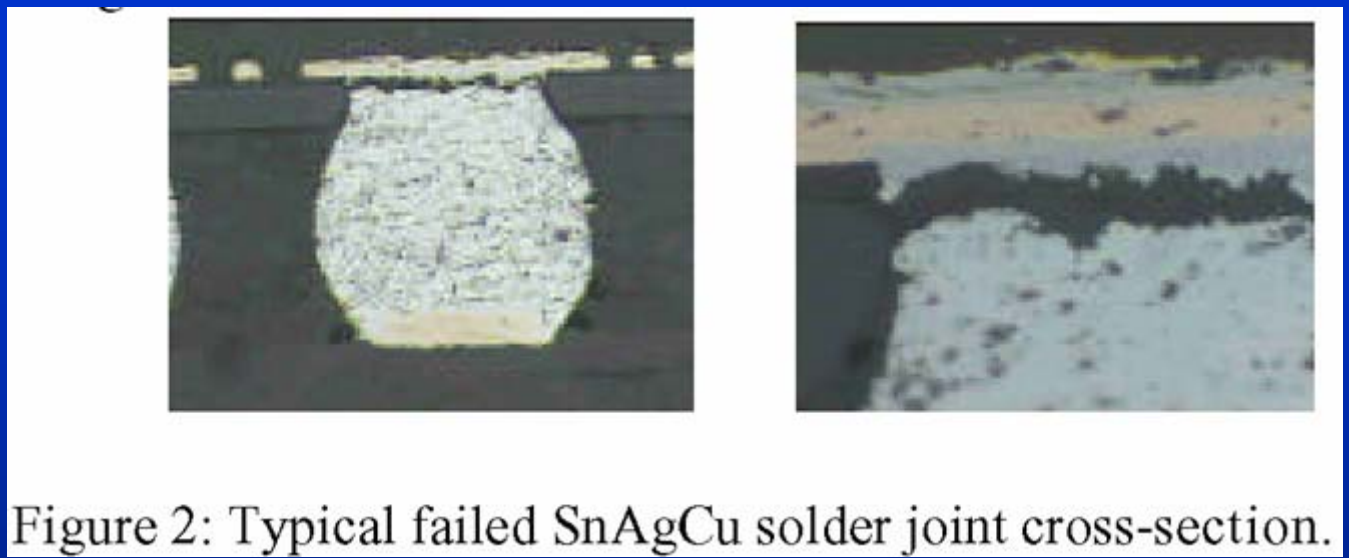


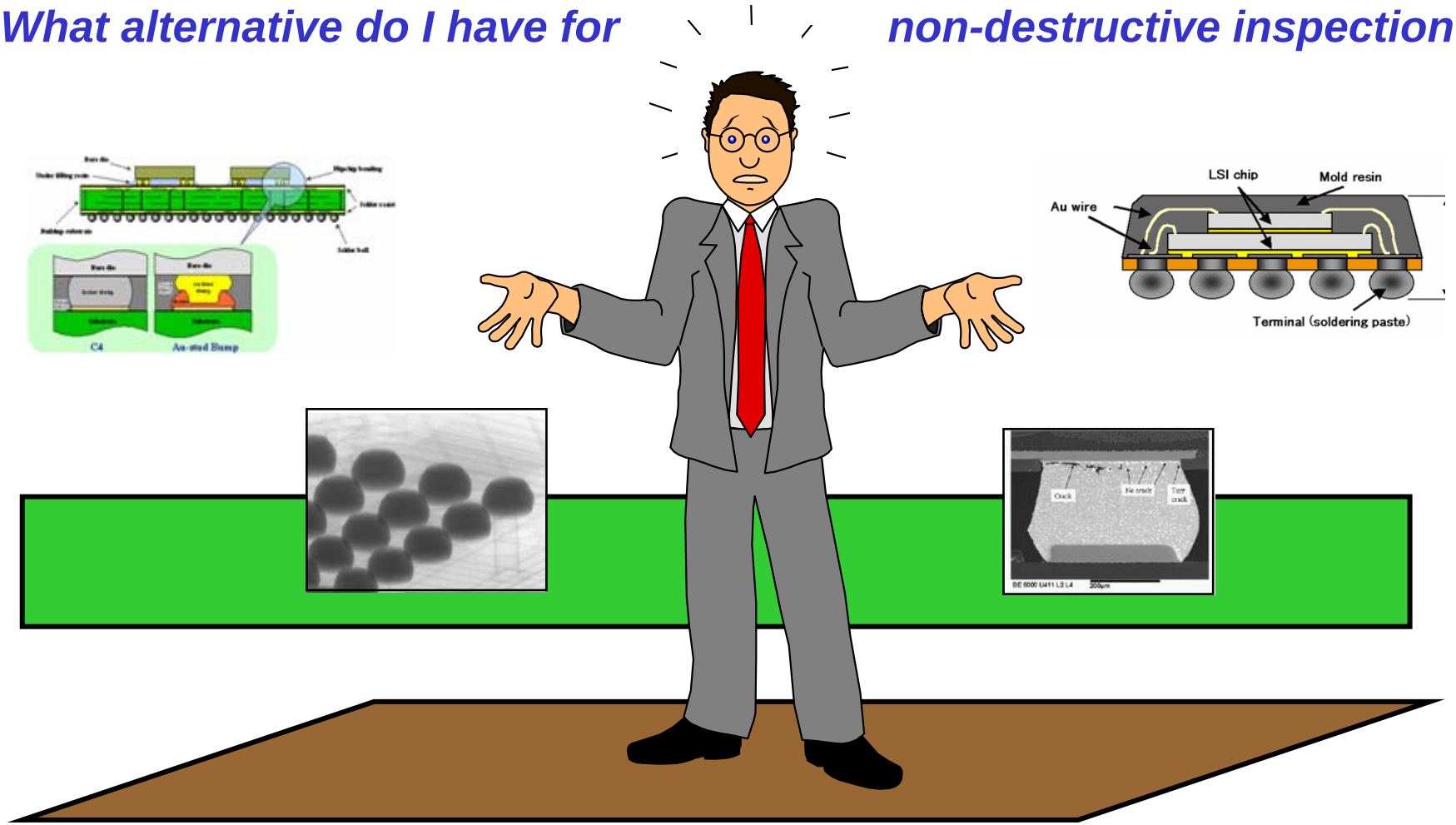
Figure 2: Typical failed SnAgCu solder joint cross-section.

"In all cases reported here, the solder joints failed at package interface. Figure 2 shows a typical cross-section of failed joint showing crack very close to intermetallic on package side."

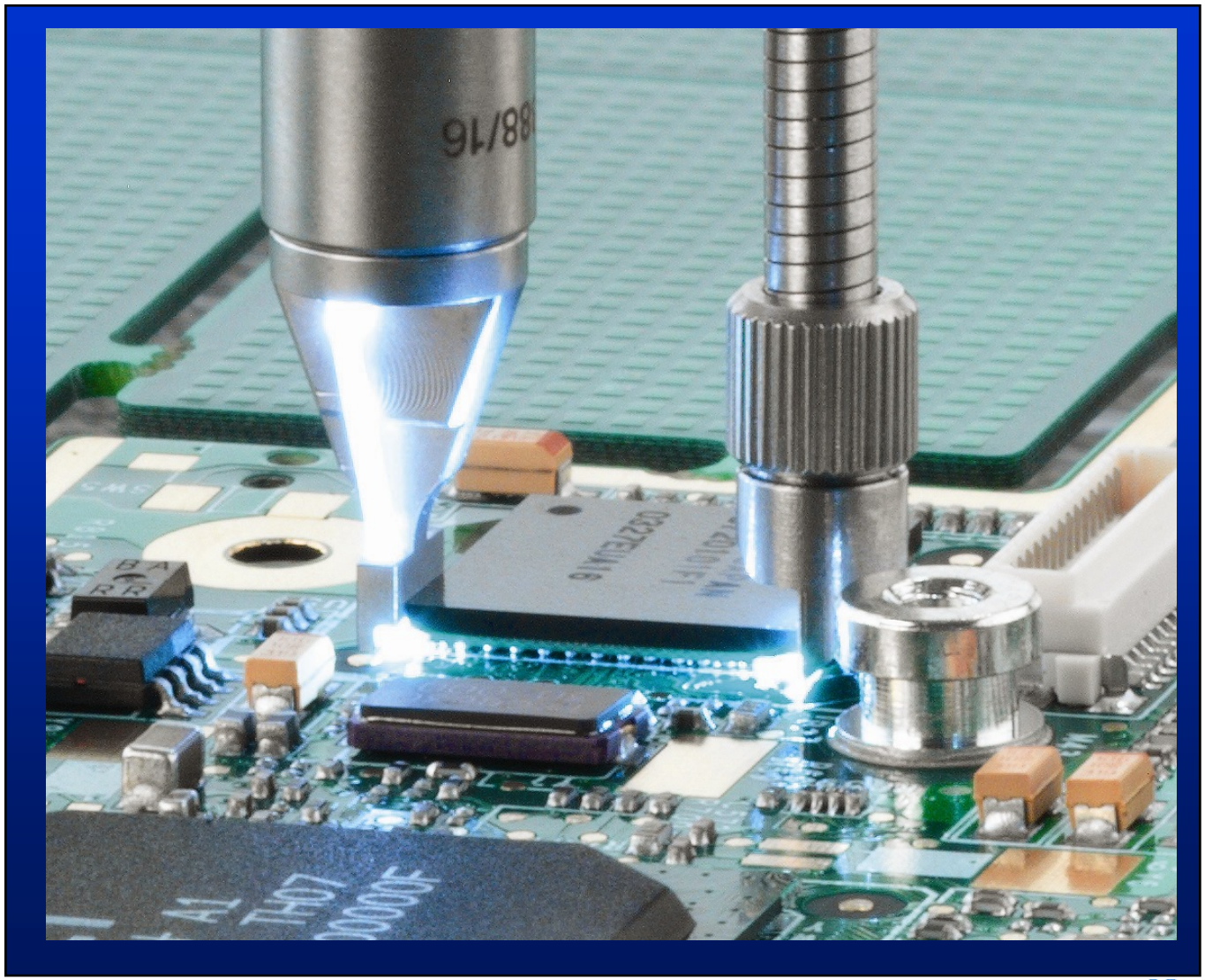
by Mr. Ahmer Syed, Amkor Technology, Inc

Test, Inspection, and FA of lead free FCs and CSPs

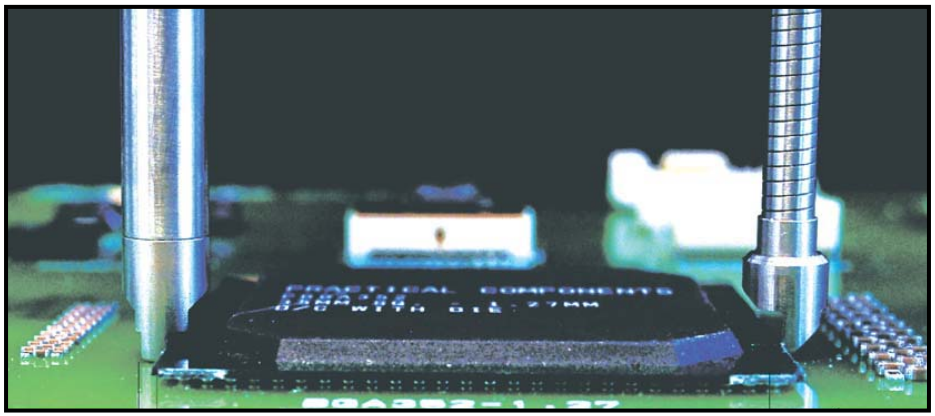
What alternative do I have for non-destructive inspection?

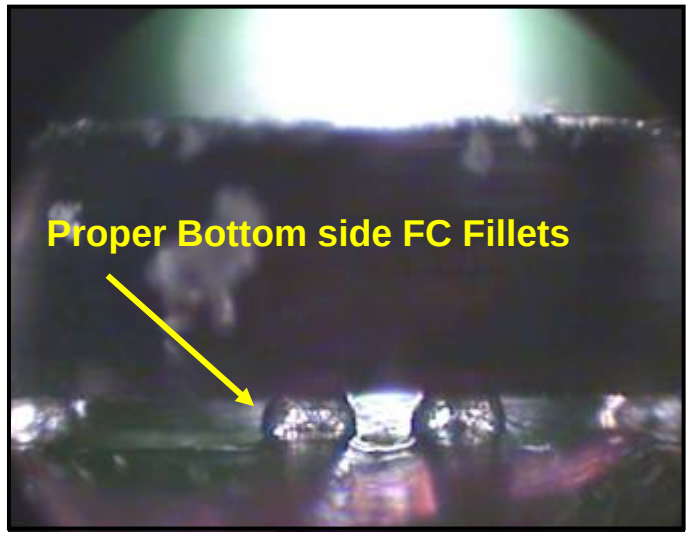


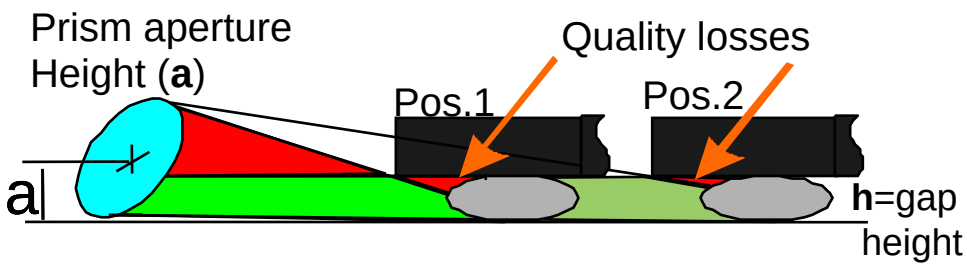
New Visual Inspection Technology for low profile FCs and CSPs

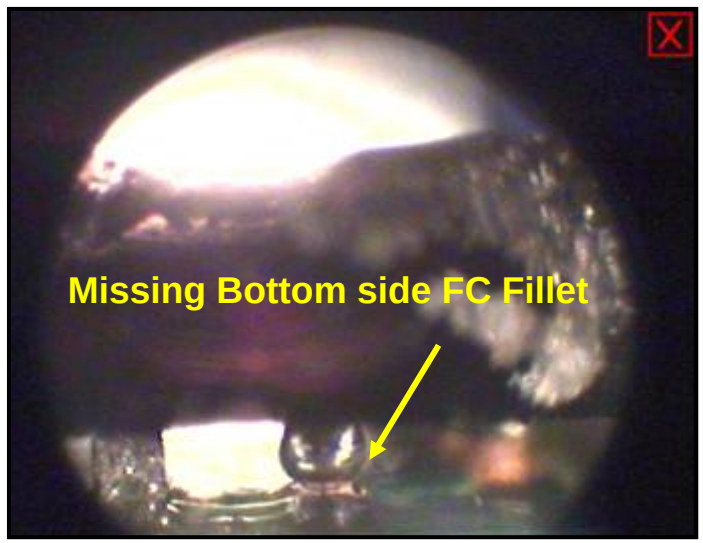


Original Optical Flip Chip Inspection: Looks down at bottom joint







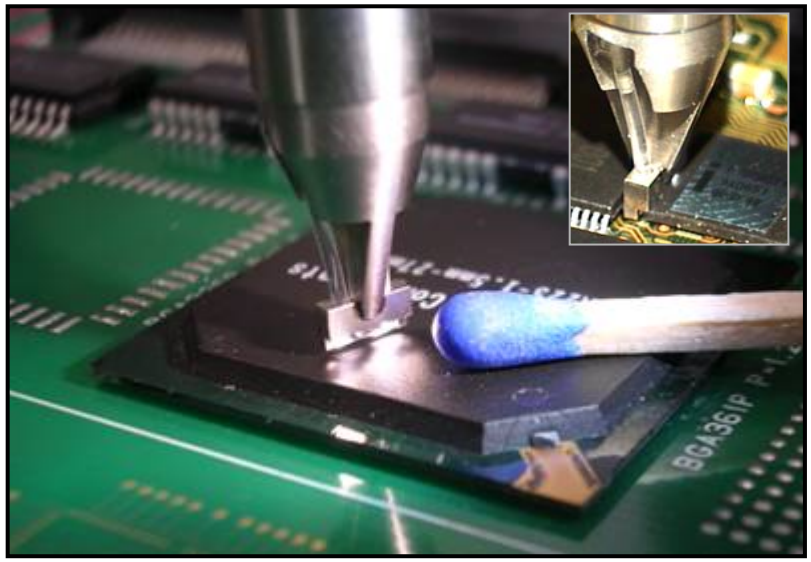


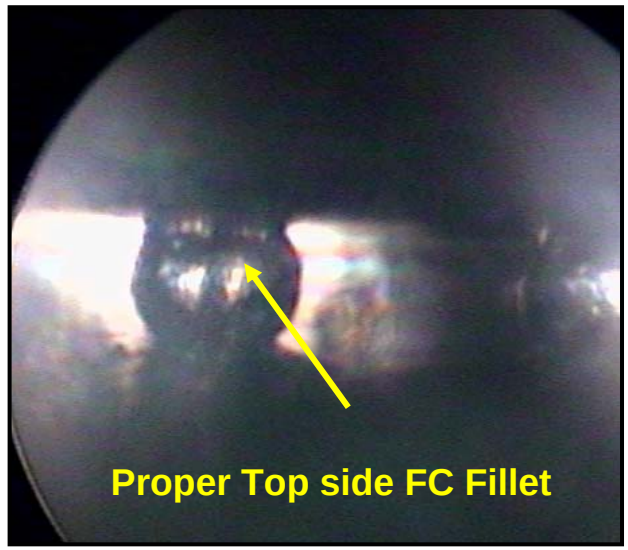
Optical Head 1: a = 0.300 mm
Flip Chip: h= 0.050 mm

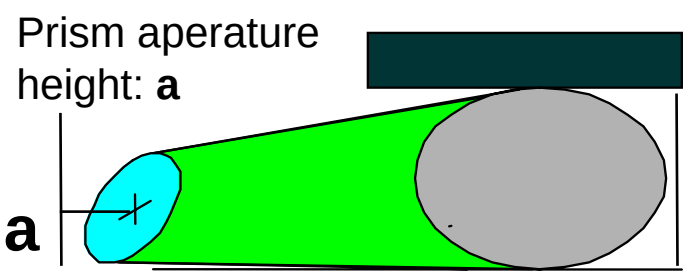
ERSA GmbH Pictures: ERSA

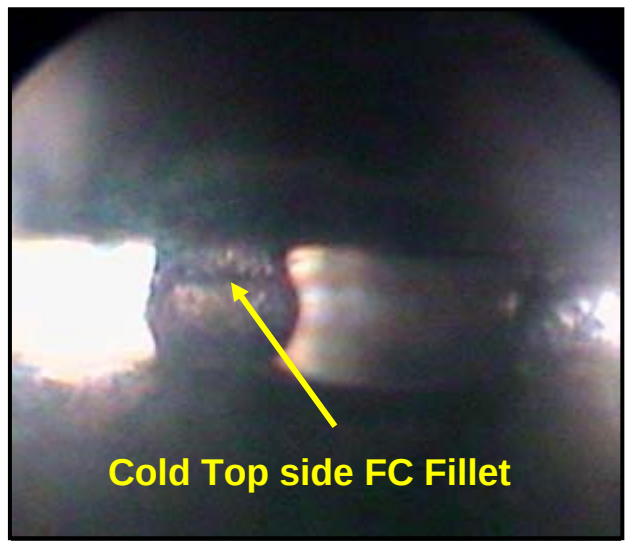
A Kurtz Company

New Flip Chip Inspection Head: Looks up at top joint!







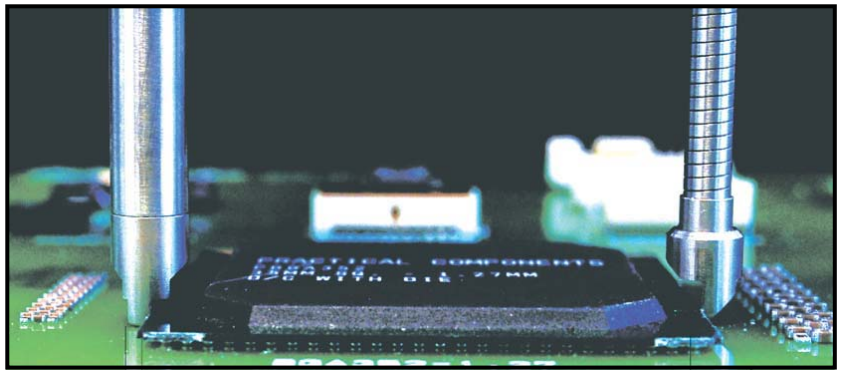


Optical Head 2: a = 0.012 mm
Flip Chip: h= 0.050 mm

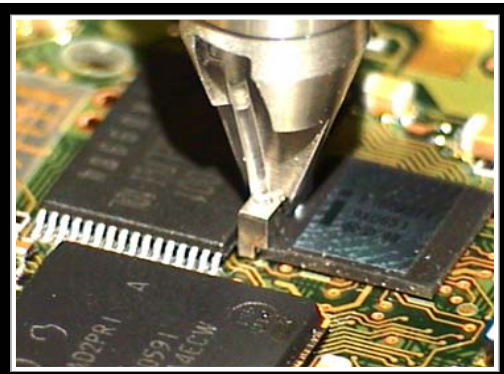
ERSA GmbH

Pictures: ERSA

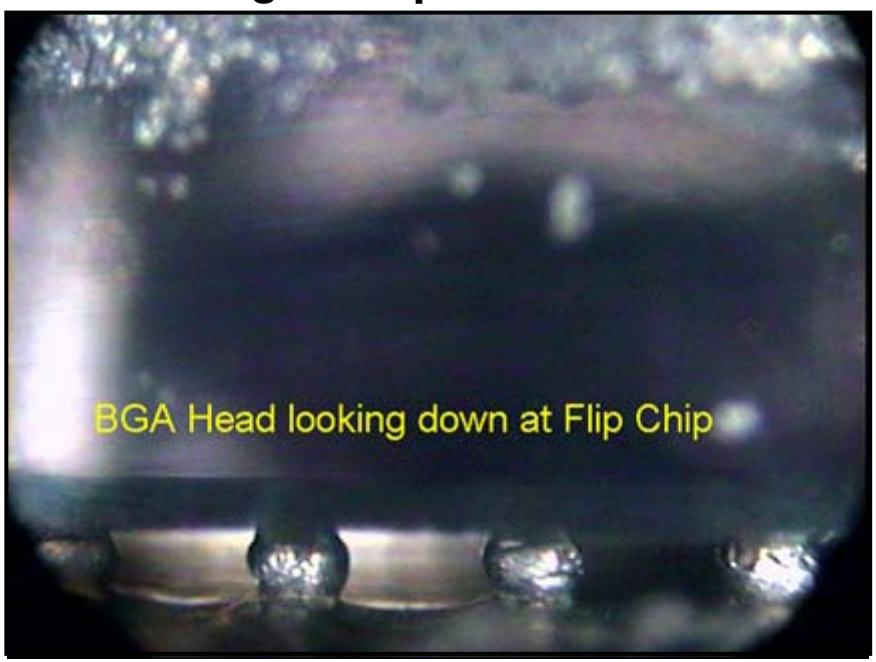
Flip Chip Inspection: Original vs. New Optical System

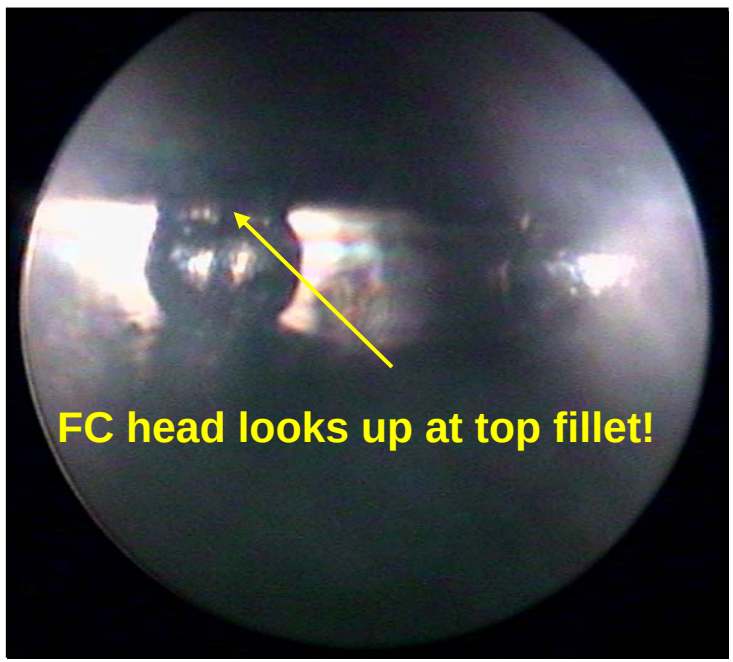


Original Optical Head

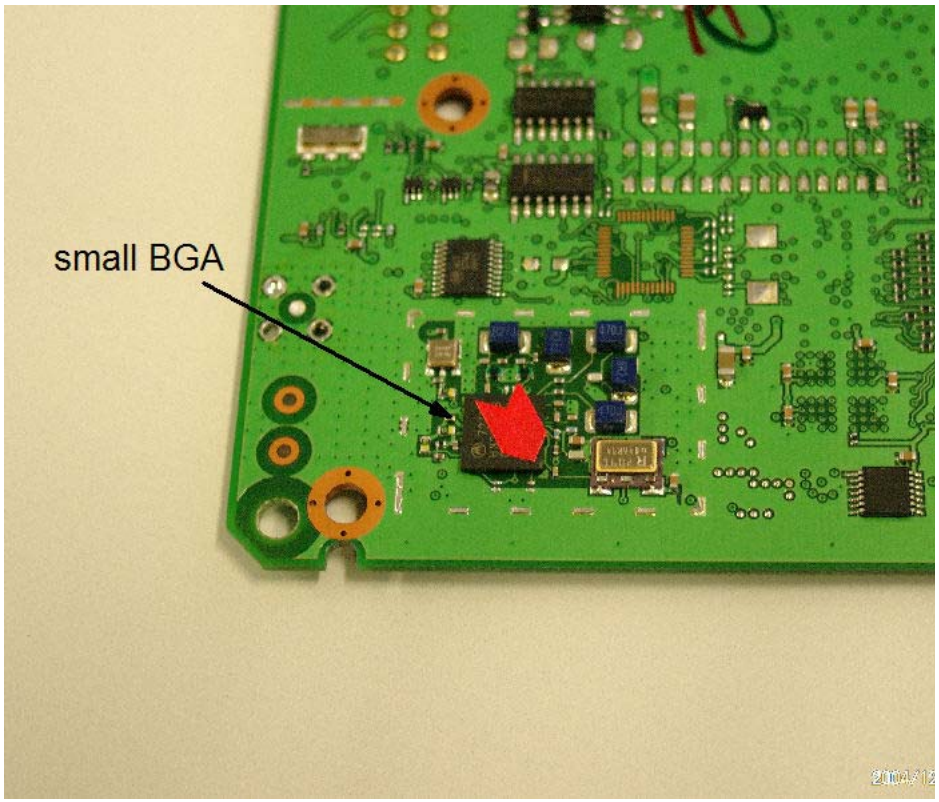


New Flip Chip Head

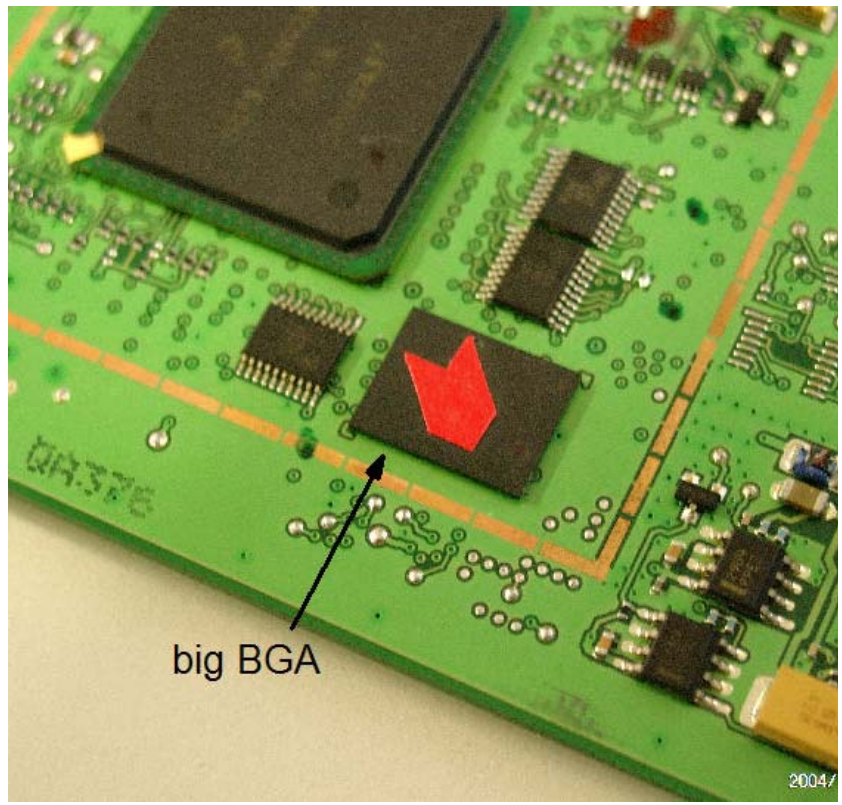




Low Profile micro BGA (lead free): a real example



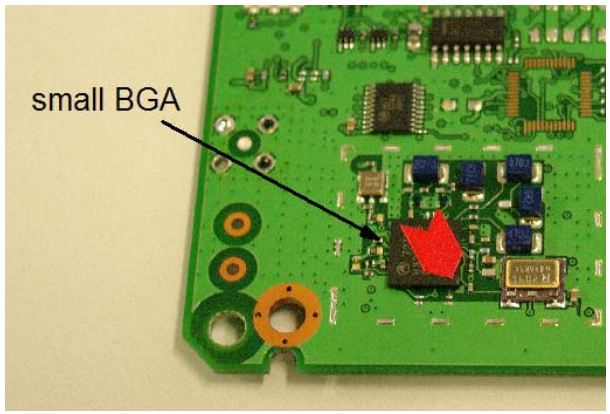
PCB top side: small micro BGA



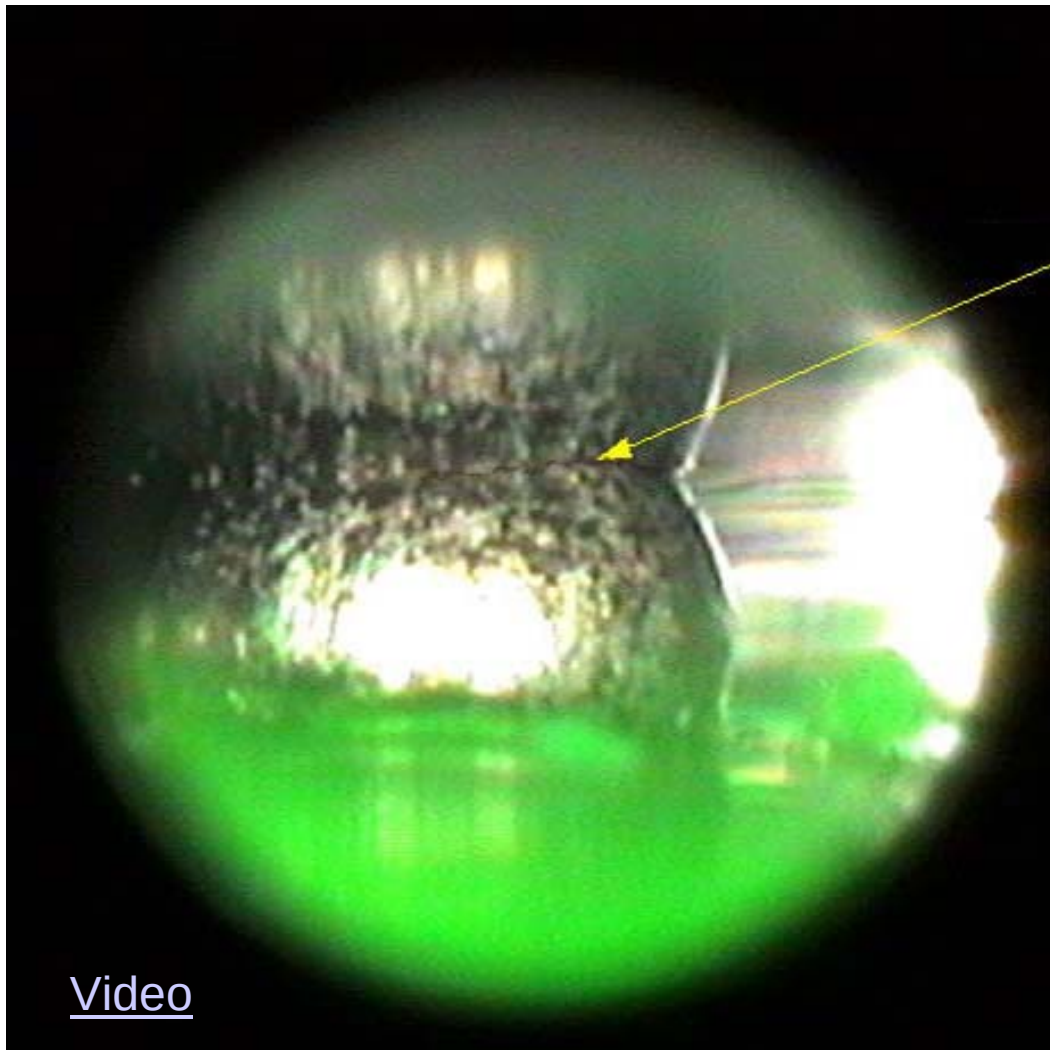
PCB bottom side: large micro BGA

ERSA GmbH Picture: ERSA

Low Profile micro BGA (lead free): a real example (1)

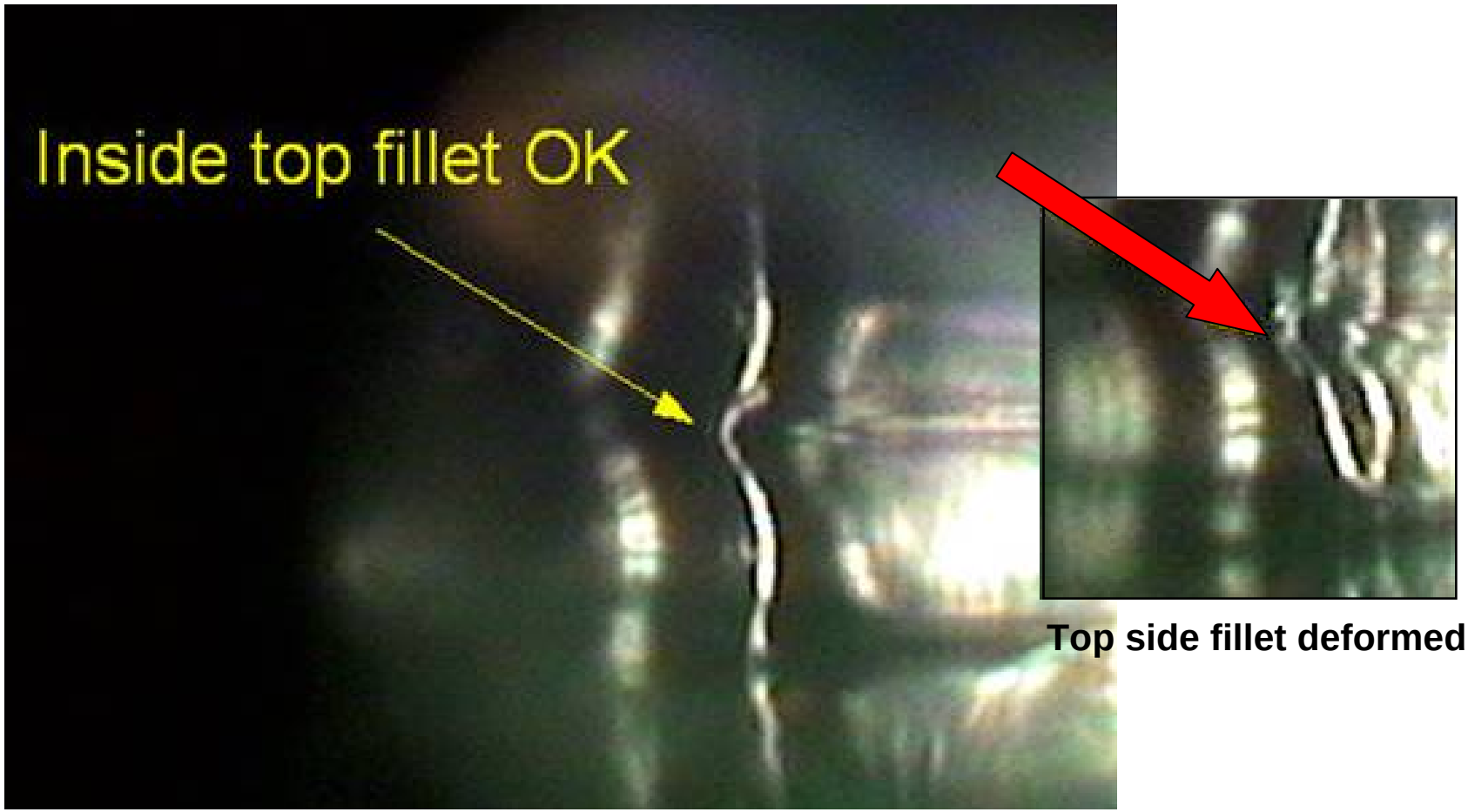


PCB top side: small micro BGA



ERSA GmbH Picture: ERSA

Low Profile micro BGA (lead free): a real example (2)

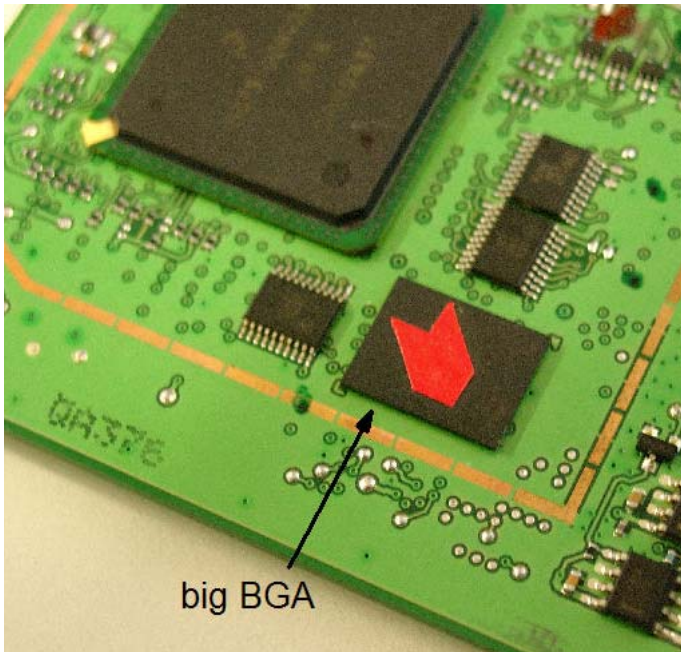


Top side fillet deformed

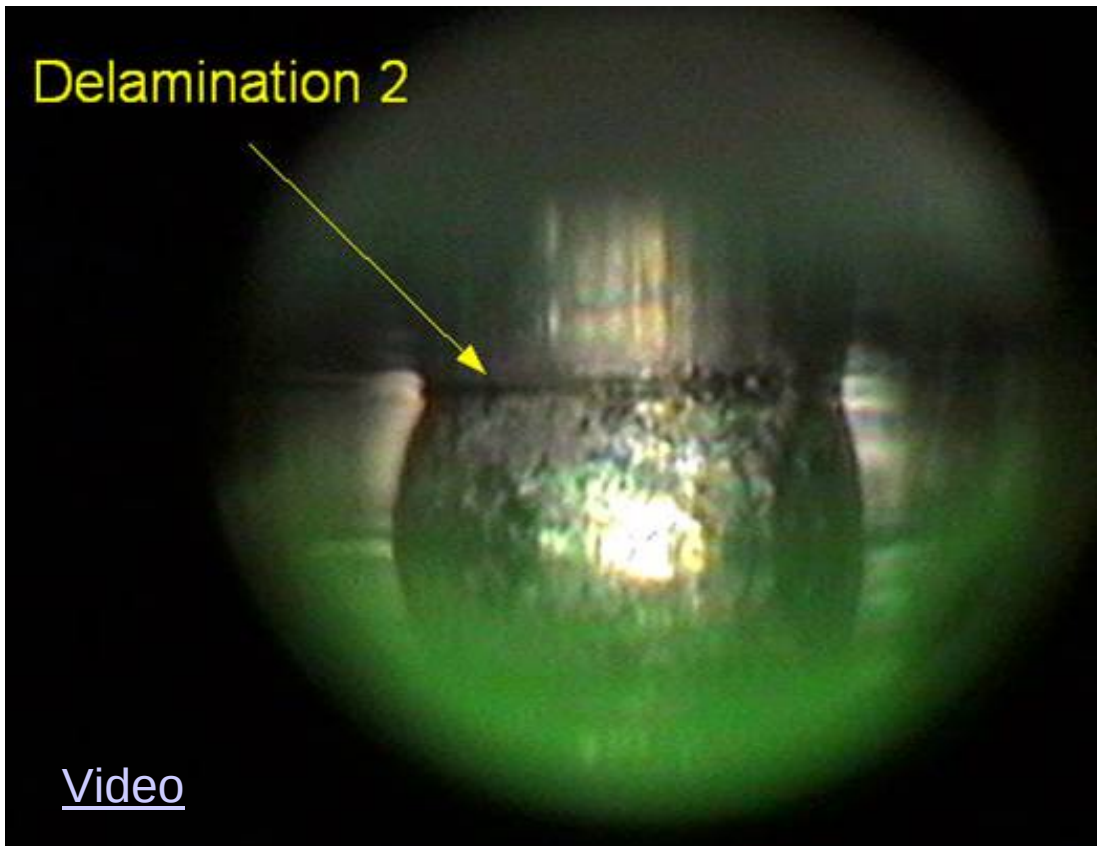
Interior top side fillet inspection is possible with new Flip Chip optical head.

ERSA GmbH Picture: ERSA

Low Profile micro BGA (lead free): a real example (3)

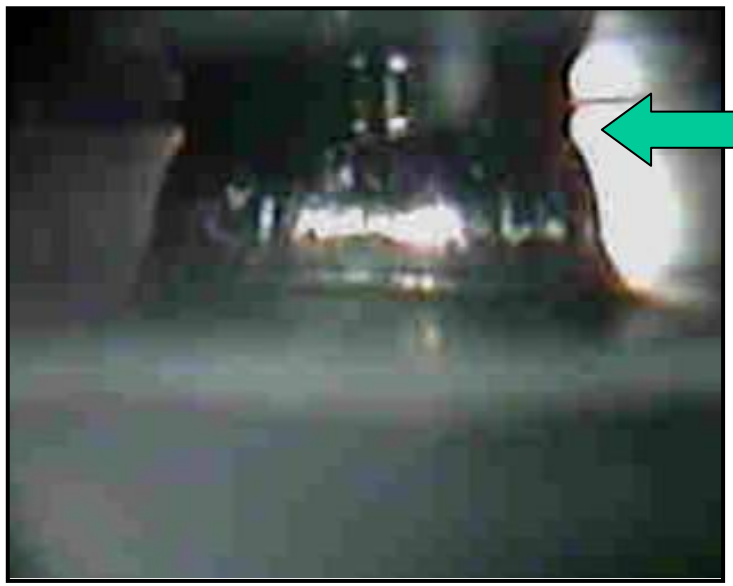


PCB bottom side: large micro BGA



ERSA GmbH Picture: ERSA

Low Profile CSP (0.80mm) Top Side Fillet Inspection



Middle ball of CSP

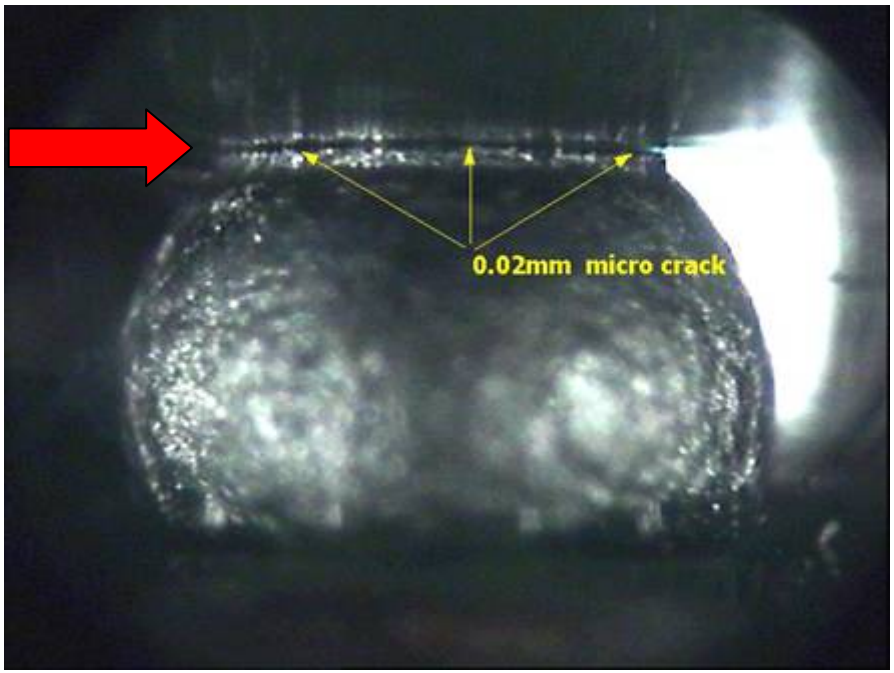
Left corner ball of CSP

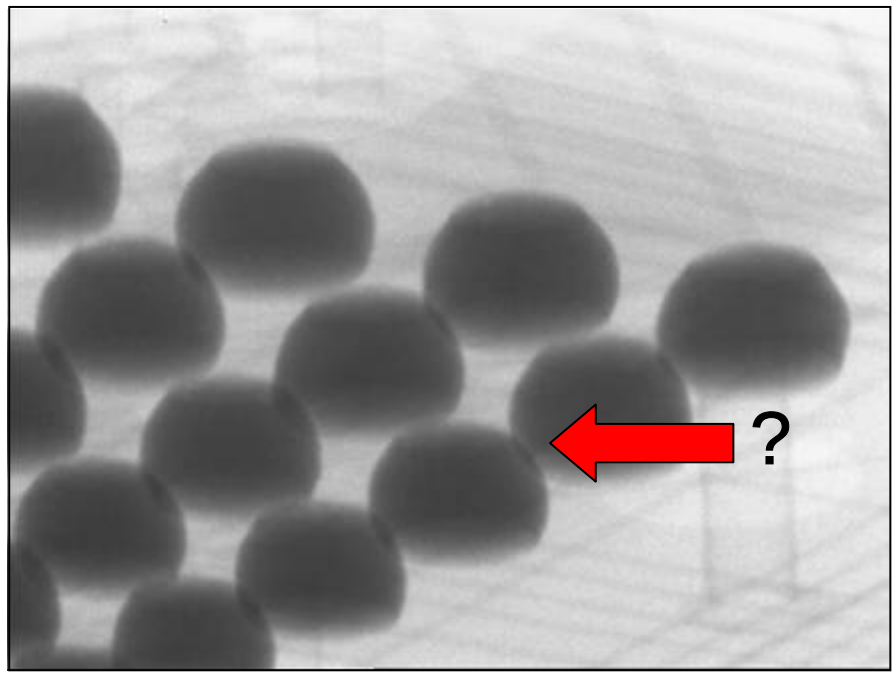
Top side fillet inspection of low profile lead free CSPs is a requirement!

ERSA GmbH Picture: ERSA

BGA Delamination: *Micro crack difficult to detect with X-ray!*

!





Non detection will result in PCB failure!

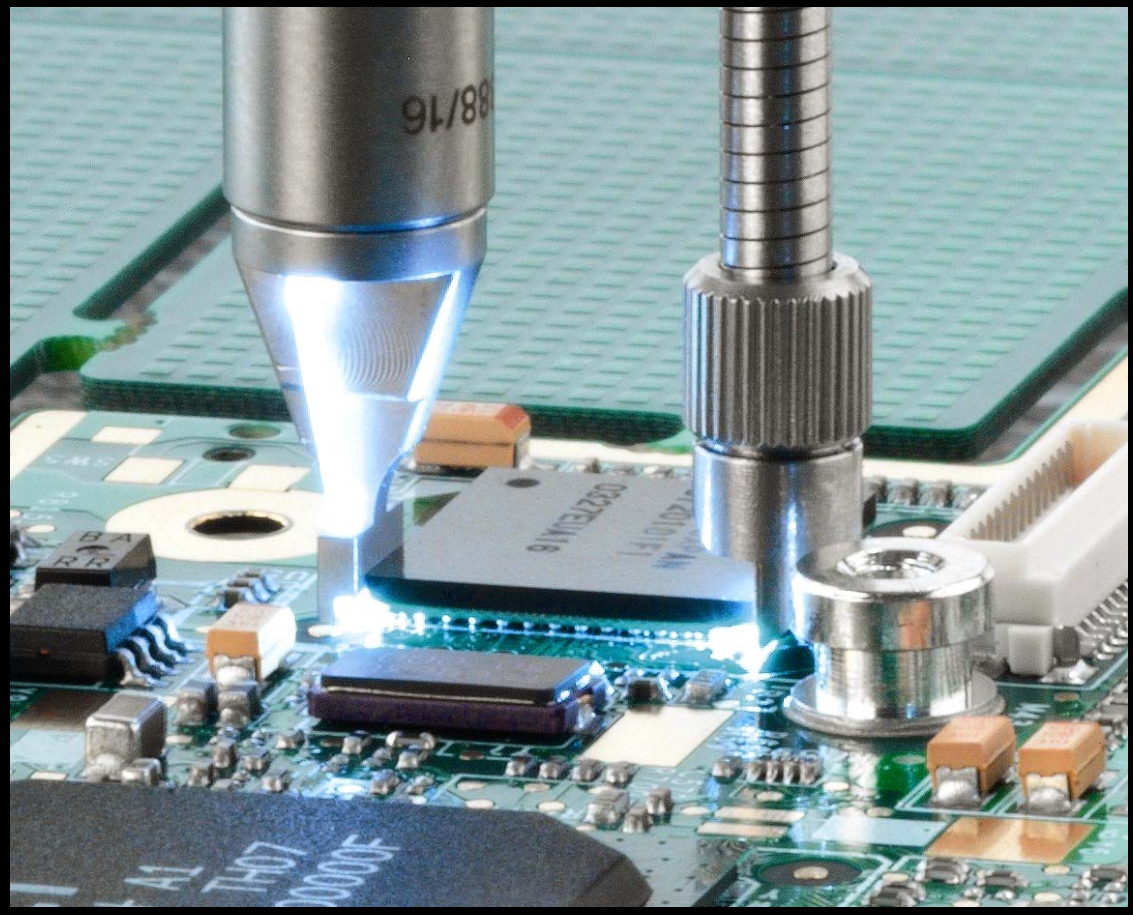
How should I set up my inspection and QC program ?

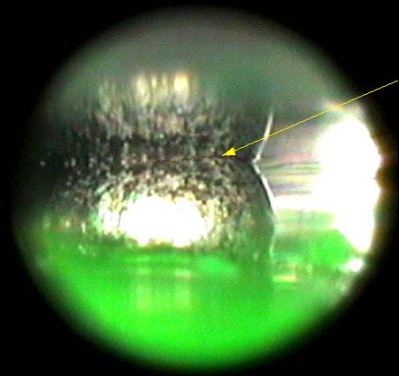
Lead Free FC and CSP Soldering:

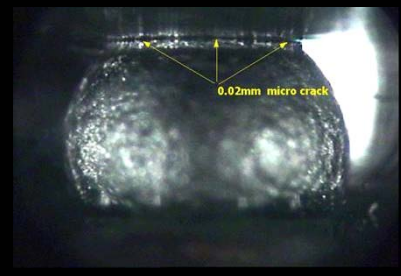
The risk for component side ball delamination will increase in a lead free process.

New inspection technology designed to perform non-destructive inspection of FCs and CSPs should be implemented!

To See is to Survive!







Only by being capable of seeing all potential problems in your process, will you be able to correct those problems, assuring reliability, and saving money lost by premature failures!