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Optimizing Production Cost with Electronic Manufacturing Simulation

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Abstract
Factory simulation has been used extensively to optimize and reduce costs across many manufacturing disciplines. Unfortunately, general purpose factory simulators do not effectively model the special needs of electronic assembly. For example, the wide variations in rework time on different boards can create a significant bottleneck for the boards with low first pass yield. This bottleneck delays product shipment, and results in higher costs and lower customer satisfaction. Since time differences due to variations in first pass yield are not effectively modeled by general discrete event based manufacturing simulators, this problem will not be caught if that is the only simulator used.

This paper presents a comprehensive approach to manufacturing simulation that includes detailed analysis of the boards to be built coupled with a general manufacturing simulator to accurately predict the time, cost, and throughput for board assembly.

Manufacturing Simulators

Manufacturing simulators and virtual prototyping have been used extensively to predict and control the manufacturing process. In the automotive industry, a complete virtual prototype is created early in the design process to insure that assembly activities are efficient and have high yield. Unfortunately, in the electronics industry, the use of comprehensive manufacturing simulators is not as prevalent compared to other industries. The list below highlights some of the key reasons that simulation is not more widely used:

- *Different board types require significantly different times to assemble* – Unlike a dedicated automotive factory that is producing the same product, a typical board assembly factory builds many different boards on a daily basis. The attributes of those boards significantly affect the assembly cost and time, and those costs and times are difficult to predict.
- *Board yield is difficult to predict* – The board yield will significantly affect the total cost and rework time necessary for that board. Lower yielding boards mean more boards fail during ICT (In Circuit Test), and therefore require diagnosis and rework. However, it is difficult to predict the yield of a specific board type without carefully analyzing the characteristics of the board itself and the components that go on the board. Key yield drivers include board type, package type, soldering used (e.g. lead free), board mounting choices, IO pitch, etc. Using an average board yield across the whole factory is inadequate because of the wide variation in board yield.
- *An electronics manufacturing model requires two different types of analysis* – For an accurate factory simulation, you must first understand all the activities and times required to build a specific type of board. As outlined above, this involves analyzing the detailed characteristics of the board and components against the capabilities of the factory to determine the total factory resources required to build that board. This will tell you the total cost, yield, and throughput of a board under ideal circumstances. Ideal circumstances means that all the factory resources are available when needed and there are no delays associated with missing resources. However, actual factories have finite resources and there will be contention for critical resources when many different boards are in production simultaneously. This means a second simulation is necessary. This second simulation involves modeling the limited factory resources and servicing the requests for those resources when the resources become available. Boards may be delayed between activities leading to longer and costlier production.

Simulating the Electronic Board Assembly

As noted in the previous section, two different types of simulation are required. Before the full factory simulation model can be used, each board type to be built at the factory must be analyzed to determine how much it will cost, how much time will be required, and which factory resources will be needed to build that board. Then, given those inputs, a model of the total factory is run and the resources can be allocated and prioritized according to the production plan for the factory. The diagram in Figure 1 shows the architecture of a complete factory simulation model using the two simulators described above.

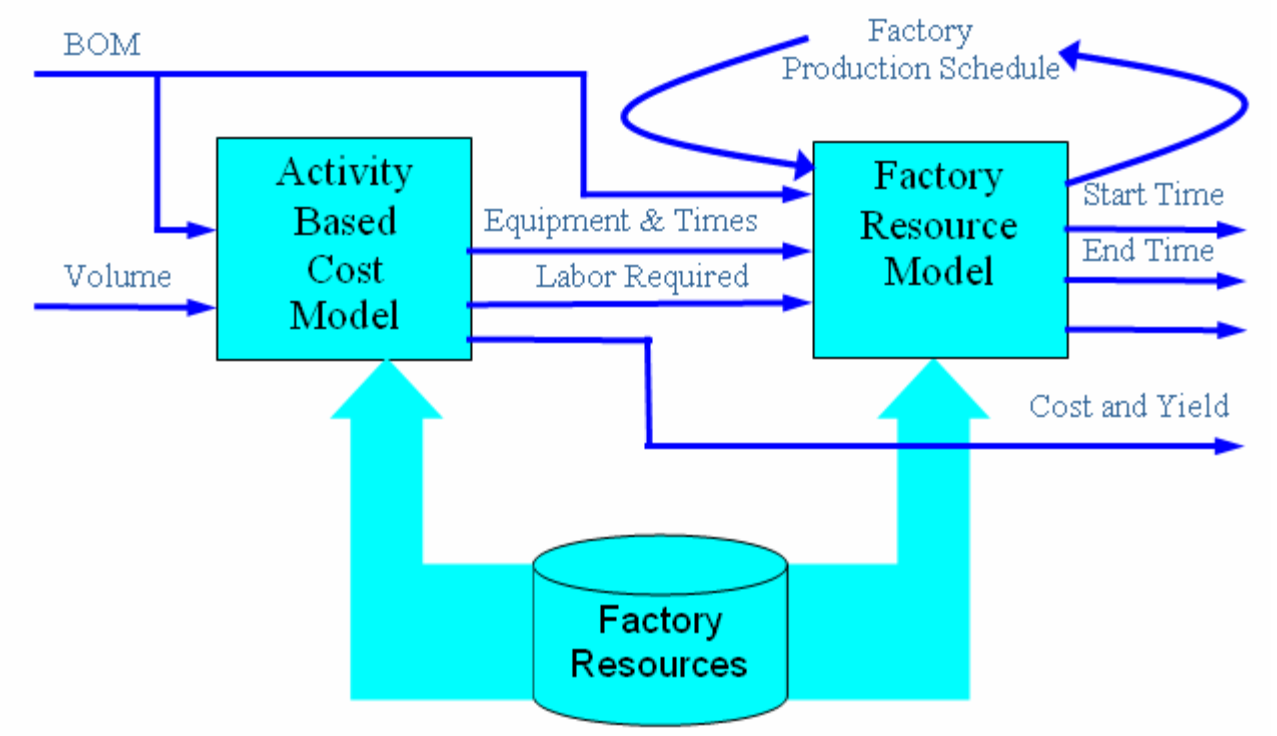

Figure 1 – Full Factory Simulation Architecture

Activity Based Cost Model

The activity based cost model is necessary to compute the cost, yield, and factory resources necessary to build a specific board. Specific board characteristics including component type, component count, board type, placement side, mount type, pin count, pin pitch, etc. are processed against the capabilities of the factory including equipment type, labor rates, overhead rates, etc. to generate the following simulation outputs.

- *Required labor resources* – The amount of labor required drives both the board cost as well as the total time required to build the board. This is used to compute the total cost and becomes an input to the factory resource model.
- *Required equipment resources* – The amount of equipment resources drives both the board cost as well as the total time required to build the board. This is used to compute the total cost and becomes an input to the factory resource model.
- *Board yield* – Yield directly affects the cost of the board since low yield board are either reworked – which adds labor cost, or scrapped – which adds material cost. The yield is not a direct input to the resource model, since the labor required includes rework labor.
- *Board Cost* – This is the total cost of the board including all material, depreciation, labor used to create the finished product.

Factory Resource Model

The factory simulation model takes as inputs the required resources (equipment, labor, and material) for each board type and combines this with the factory production schedule to determine necessary resources, sequencing, and priorities to complete the production plan. A discrete event simulator is used to analyze the capacity, throughput, station wait times and queues that will occur in the factory during production. Each specific type of factory resource and its capacity forms the complete factory resource model. As simulation time passes, assembly activities request resources. When all the necessary resources are available (equipment, labor, and material), the request is serviced and the activity completes. However, if all the resources are not available, the activity must wait until they become available. For example, a factory will have a certain number of rework personnel available and boards needing rework will be delayed until someone is free to work on the board.

Simulating the combination of the production plan, the resource requirements for each board type, and the actual capabilities of the factory produces the total cost, yield and completion time for each board type being built. Note that the results of the factory resource simulation model depend on the characteristics of the specific board being built as well as all the other boards being built at the same time. If the factory is busy, the elapsed time required to build a board will be significantly longer than if the factory is not busy. The outputs of the factory resource model are all times.

- *Start time* – This is when a board begins production. It may be a scheduled time or it may be the time that the first activity in the process can begin.

- *Completion time* – This will be the actual time that the board (or actually lot of boards) finishes.
- *Elapsed time* – This will be the total time in production. As noted above, this number will vary on the same board type based on how close the factory is to capacity.

Value of Simulation

In the section above, we showed a methodology for doing a complete factory simulator. So, a relevant question is - Once we run the simulation and get results, what can we do with it? Our goal for doing this simulation is to optimize the production cost of the product and to accurately predict and manage time to market. The cost and yield results of the simulation provide the designer with specific feedback regarding the highest cost and lowest yielding manufacturing activities. He or she can then optimize the design and in many cases reduce or eliminate those activities. For example, if the only through hole components in the design are connectors and it is possible to use a pressfit connector, wave soldering can be completely eliminated. The factory resource model provides the production planning organization with the ability to insure that resources are balanced. A simulation showing 20% utilization of most of the resources with 80% utilization of others indicates a factory that is not well balanced according to the production mix being built. Balancing these resources reduces the total time in production and reduces cost since idle resources cost money.

To show this simulation in operation, one system was used to determine the time, cost, and factory resource requirement for each different design, and a second discrete event simulation product was used to simulate a factory with finite resources. A description of each of these follows.

***SavanSys* Activity Based Cost and Yield Model Overview**

Below is a brief description of the activity based cost and yield modeling technology. For additional information on the capabilities and availability of this technology, please contact the author.

This system is a cost, yield, and technology tradeoff tool. Data is extracted from the design tool environment to create a physical representation of the design. Activity based models of both board fabrication and assembly are created to model the manufacturing process using the step definitions presented earlier in this paper. This combination of design and manufacturing information is used to generate a “virtual prototype” of the board to accurately determine size, cost, time, and yield throughout the manufacturing process. The results of this model are extremely accurate because it considers the details of the target board applied to a specific manufacturing environment with precise capabilities.

The data considered by the tool for doing this analysis is listed below.

The Design Model

Because of the substantial number of packaging technologies, processes, and materials that are available, making optimum choices is not a trivial task. Alternative technologies and materials include:

- Substrates (printed circuit boards, ceramic, thin-film, etc.)
- Chip packaging
- Bonding techniques (wirebond, TAB, flip chip)
- Test techniques
- Manufacturing methods

The tool accepts physical information that describes multiple chips (or bare die) and their interconnection. The tool inputs and considers the following physical inputs.

Chips (bare die and packaged die):

- Dimensions (length, width, thickness)
- I/O type and count
- Cost and yield

Chip Packaging:

- Bonding (technology, materials, and design rules)
- Encapsulation (materials and design rules)
- Die attach (materials and design rules)
- Process flow information (chip preparation, testing, and burn-in)

Boards/Modules:

- Substrate (technology, materials, and design rules)

- Connectorization (technology, materials, and design rules)
- Process flow information (substrate fabrication)

The plot in Figure 2 shows the results of an analysis.

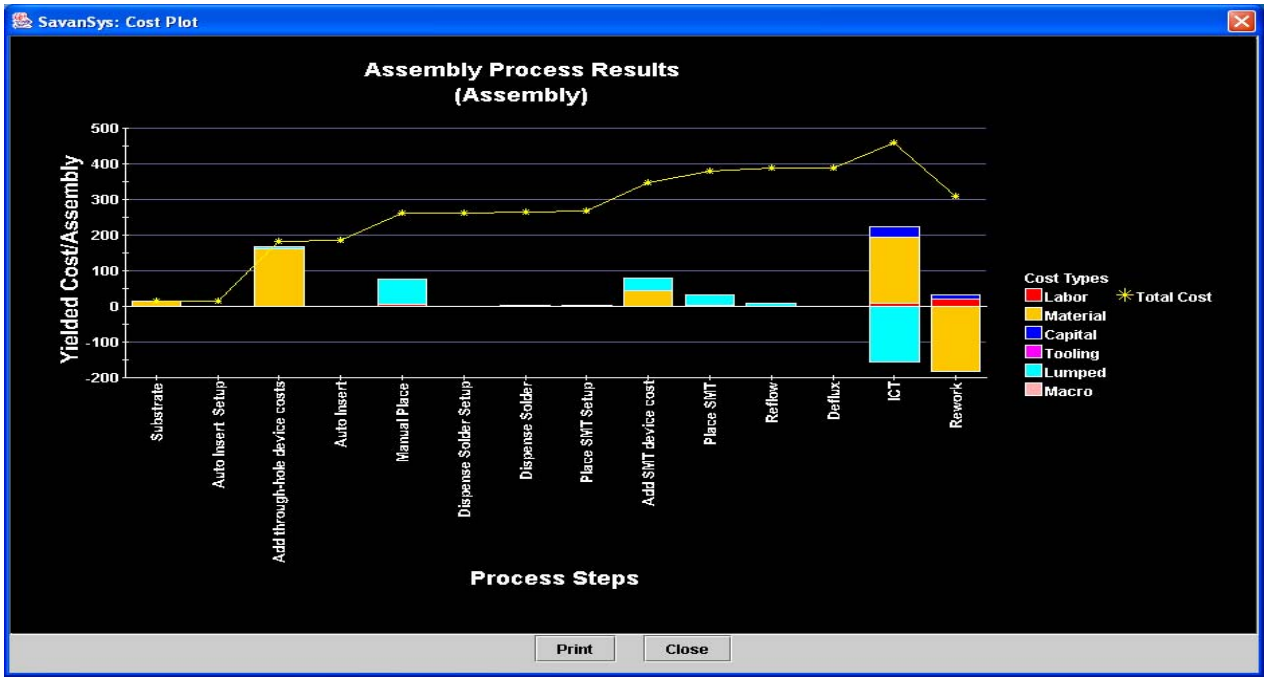

Figure 2 - Cost Plot

The Manufacturing Model

Cost models may include the following costs and yield. Given that the costs below are optional, models can be used to analyze total system costs and required resources or components of the system cost and resources.

- Component cost and yield (entered or computed)
- Component preparation (process may be defined)
- Single chip package cost and yield (entered or computed)
- Substrate fabrication cost and yield (entered, computed, or process flow)
- Surface mount and through-hole assembly cost and yield
- Bare die attach cost and yield (TAB, wirebond, flip chip)
- Tooling costs associated with assembly processes
- Test, repair, and rework costs, coverages, success rates, and yields.

The methodology for defining cost models is based on dividing the process into a series of activities and then defining the costs, times, and yields associated with each of those activities. Step types are one of the following:

- Substrate – This step calculates the cost and yield of the substrate using either a user defined calculation or running a substrate fabrication process flow.
- Component – This type of step adds the cost and yield of new components to a system.
- Assembly – This type of step is used to define the cost and yield of board assembly activities.
- Processing – This type of step is used to define the cost and yield of board fabrication activities.
- Test - This type of step defines testing activities. Defects introduced into the system by previous steps are detected by test steps, and the board/panel is either fixed through rework or scrapped.
- Rework – This type of step defines the repair or rework activities.

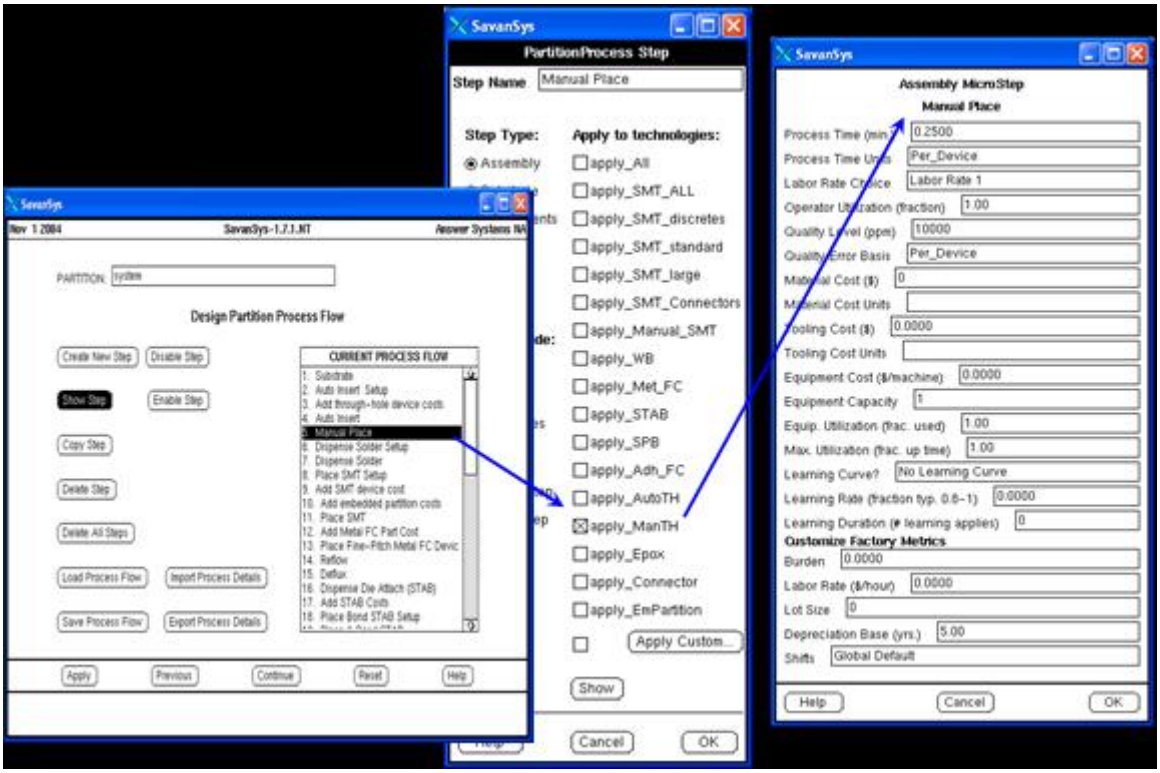

Figure 3 – Manual Place Step Details

Step definitions vary slightly based on the type of step, but all steps include the following basic information:

- Time – Used to calculate labor and equipment requirements.
- Operator utilization and rate – Combined with time to get cost and required labor.
- Equipment utilization and cost – Combined with time and depreciation schedule to determine allocated cost and how often that equipment is busy.
- Defects in parts per million or defects per square cm – Used to calculate and accumulate the system yield that will drive the required rework resources.
- Tooling costs – Divided over the lifetime quantity of boards.
- Material and amount used – References the material database to calculate material costs.

The screen shot in Figure 3 shows an example step definition for an assembly step.

***Foresight* Discrete Event Simulation Model Overview**

This system is a general purpose discrete event simulation package. Two main types of constructs make up the model:

- Activities – Activities are used to describe the functionality of the process being modeling. This functionality can be expressed as a combination of data flow diagrams, procedural code, and state transition diagrams. These activities communicate in a sequence which may change based on the data being processed. For example, in this board factory model, the rework activity will only take place on boards that fail test.
- Resources – The resource model is used to simulate the limited capacity of the actual factory. Each activity can only be completed if it has all the right resources available to complete the activity. For this factory model, those resources may be people, equipment, material, or factory floor space. For example, if there is a big delay at one station and there is no room to queue up additional boards for the next station, the activity before that station will be delayed even if it has equipment and people resources available.

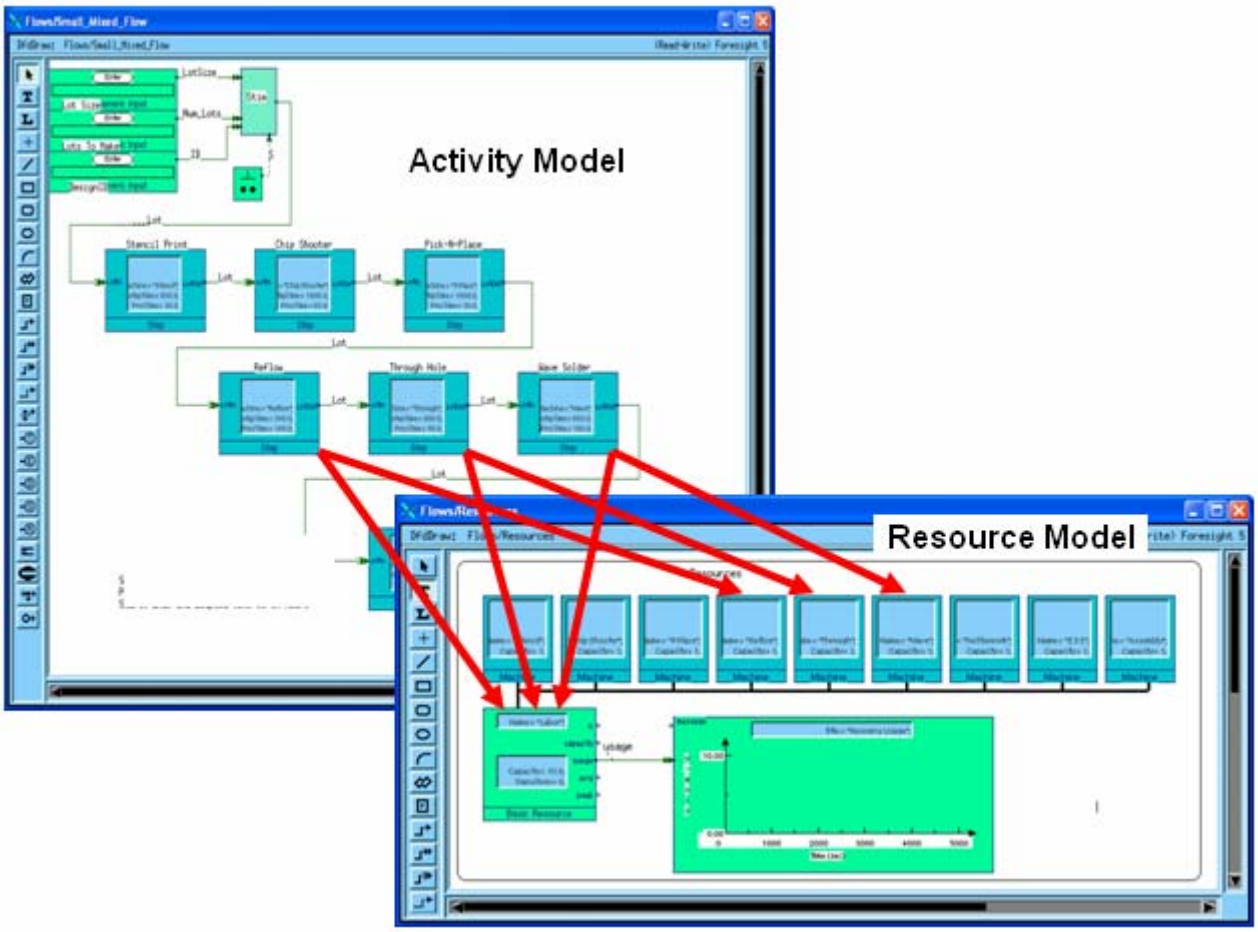

Figure 4 –Event Factory Model

The screen shot in Figure 4 shows a model of a board assembly factory. Each activity requests the appropriate amount of equipment and labor resources to complete that activity for that board. The next activity in sequence will not start until the previous activity is complete. The resource model grants the activity requests based on availability and priority. In the example above, one lot of boards will not be interrupted until that complete lot is processed. So, even if a high priority job comes through, it may get delayed if a large lot is being processed. The production planner can optimize the efficiency by managing the lot size and priorities.

Summary and Conclusions

This paper presents a new and comprehensive approach to the simulating the assembly manufacturing of electronic boards. The combination of an activity based simulation to determine the per board costs and times is combined with a factory resource simulation model to also the actual production time. By using this approach, designers and production planners can reduce costs and optimize the use of resources.