Presented in the ECWC 10 Conference at IPC Printed
Circuits Expo®, SMEMA Council APEX® and
Designers Summit 05

Semiconductor Technology ITRS Roadmap

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For four decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table 1 with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law. (i.e., the number of components per chip doubles every 24 months). The most significant trend for society is the decreasing cost-per-function, which has led to significant improvements of productivity and quality of life through proliferation of computers, electronic communication, and consumer electronics.

Table 1 - Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor clock rate, GHz**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last two decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. *The International Technology Roadmap for Semiconductors (ITRS)* has been an especially successful worldwide cooperation. It presents an industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, research organizations, and governments. The *ITRS* has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that truly need research breakthroughs.

The *ITRS* is the result of the continued worldwide consensus building process. The participation of semiconductor experts from Europe, Japan, Korea, Taiwan, and U.S.A. ensures that the *ITRS* continues to be the definitive source of guidance for semiconductor research as we strive to extend the historical advancement of semiconductor technology and the integrated circuit market. The diverse expertise and dedicated efforts that this international effort mobilized have brought the Roadmap to a new level of worldwide consensus about future semiconductor technology requirements.

Emerging Research Devices

The *2001 ITRS* document marked the additional investigation of the limits of traditional scaling, its extension by improving electrical performance with new or improved materials, and of the introduction and feasibility of new device architectures. This new section on Emerging Research Devices (ERD), in 2001 highly coordinated with Process Integration, Devices, and Structures (PIDS), has evolved considerably since then. This evolution is seen in the two primary goals for Emerging Research Devices.

The first and original goal is to stimulate invention and research leading to proof of concept and feasibility demonstration for one or more Roadmap-extending concepts. A new and important corollary goal this year is to provide a balanced view of many of the exciting new approaches to information processing, articulating their potential contributions balanced with a brief discussion of their limiting challenges. In addressing these goals, this section serves two purposes. First is to introduce advanced non-classical CMOS structures and memory technologies aimed at extending microelectronic technologies to the end of this Roadmap timeframe. Second is to introduce and critique (without endorsement) new technological concepts for logic and architectures aimed at extending information and signal processing beyond the end of the Roadmap timeframe.

The quickening pace of MOSFET scaling is accelerating the introduction of new technologies to extend CMOS beyond the 65 nm node. These technologies include both new materials and advanced MOSFET structures. The Front End Processes chapter discusses new materials required for the gate stack and the PIDS chapter identifies technology requirements for CMOS structures. In a complementary fashion, the new ERD chapter serves as the bridge between bulk and non-classical CMOS and the realm of microelectronics beyond the end of the Roadmap.

Technology Characteristics / Requirements Tables

These tables summarize key high-level technology requirements, which define the future "technology nodes" and generally establish some common reference points to maintain consistency . The high-level targets expressed in the ORTC tables are based in part on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies. Thus, the ORTC provide a "top-down business incentive" to balance the tendency for the ITWGs to become conservative in expressing their individual, detailed future requirements.

The ITRS technology node is defined as the minimum metal pitch used on any product, for example, either DRAM half pitch or Metal 1 (M1) half pitch in Logic/MPU. DRAMs continue to have the smallest metal half pitch; thus it continues to represent the technology node. Commercially used numbers for the technology generations typically differ from the ITRS technology node numbers. However, the most reliable technology standard in the semiconductor
industry is provided by the above definition, which is quite clear in that the patterning and processing (etching, etc.) capability of the technology is represented as the pitch of the minimum metal lines. Table 2 is a representative section of the larger ORTC.

Table 2 - Silicon Roadmap Table Structure—Key Lithography-related Characteristics by Product Type

Near-term Years

YEAR OF PRODUCTION	2003	2004	2005	2006	2007	2008	2009
Technology Node		hp90			hp65		
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50
MPU/ASIC M1 ½ Pitch (nm)	120	107	95	85	75	67	60
MPU/ASIC Poly Si ½ Pitch (nm)	107	90	80	70	65	57	50
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20

Long-term Years

YEAR OF PRODUCTION	2010	2012	2013	2015	2016	2018
Technology Node	hp45		hp32		hp22	
DRAM ½ Pitch (nm)	45	35	32	25	22	18
MPU/ASIC M1 ½ Pitch (nm)	54	42	38	30	27	21
MPU/ASIC Poly Si ½ Pitch (nm)	45	35	32	25	22	18
MPU Printed Gate Length (nm)	25	20	18	14	13	10
MPU Physical Gate Length (nm)	18	14	13	10	9	7

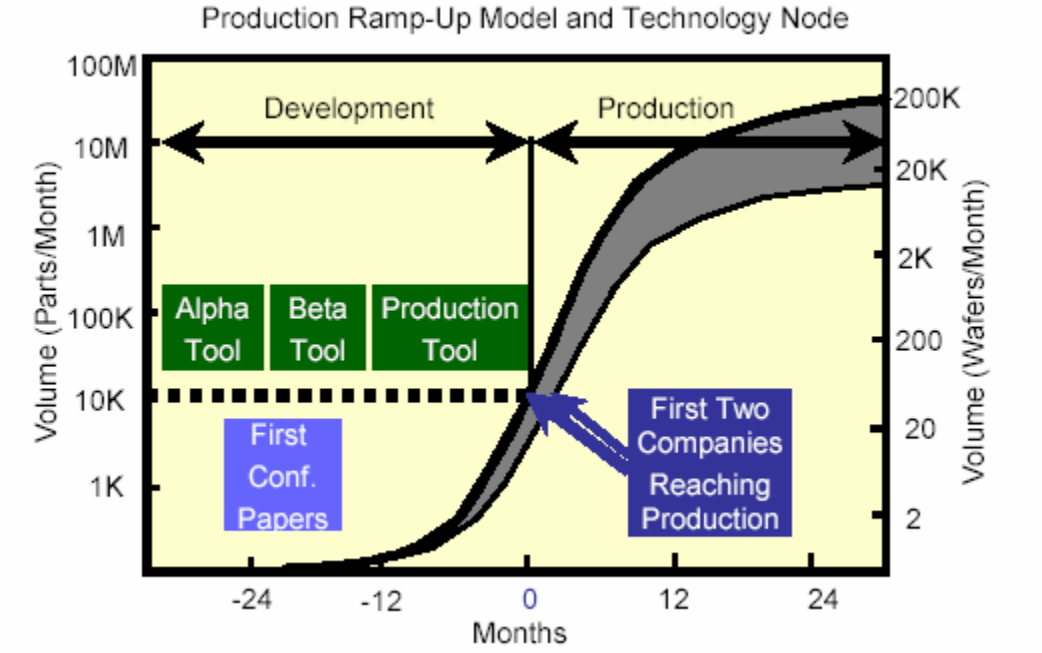

Figure 1 - A Typical Production "Ramp" Curve Volume

The technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "Time of Introduction" in the *ITRS* is the "Year of Production," which is defined in Figure 1.

The "Production" time refers to the time when the first company brings a technology to production and a second company follows within three months. Production means the completion of both process and product qualification. The product qualification means the approval by customers to ship products, which may take one to twelve months to complete after product qualification samples are received by the customer. Preceding the production, process qualifications and tool development need to be completed. Production tools are developed typically 12 to 24 months prior to production. This means that alpha and succeeding beta tools are developed preceding the production tool.

Also note that the Production "time zero (0)" in Figure 1 can be viewed as the time of the beginning of the ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (WSPM) capacity, the time to ramp from 20 wspm to full capacity can take nine to twelve months. This time would correspond to the same time for ramping device unit volume capacity from 6K units to 6M units per month if the chip size were 140 mm2 (430 gross die per 300 mm wafer × 20K wspm × 70% total yield from wafer starts to finished product = 6M units/month).

Technology Nodes

The concept of "technology nodes" used to be quite straightforward to understand as it has historically been linked to the introduction of new Dynamic Random Access Memory (DRAM) generations with a 4× increase in bits/chip between generations. For as long as this cycle strictly followed Moore's Law (three-year cycle for 4×), the technology nodes and DRAM generations were essentially synonymous. However, in recent years, a greater diversity of products serving as technology drivers, faster introduction/optimization of product-specific technology, and the general increase in business and technology complexity are all tending to de-couple the many technology parameters that have traditionally characterized "advance to the next technology node." For example, microprocessor unit (MPU) and ASIC or Logic products have recently driven the reduction of gate length at a faster pace than lithography half-pitch. While DRAM continues to drive the lithography half-pitch, MPU/ASIC drives the gate length. Even the choice of basic lithography technology has tended to become more product specific (such as "pushing the wavelength as fast as possible" versus "using phase-shift masks"). Following the practice of the *2001 ITRS*, the *ITRS* ORTC tables list the DRAM half-pitch, the MPU /ASIC half-pitch, and MPU gate length, as shown in Table 2. These technology parameters are defined in Figure 2, which now also includes the MPU/ASIC Metal 1 (M1) half-pitch line item.

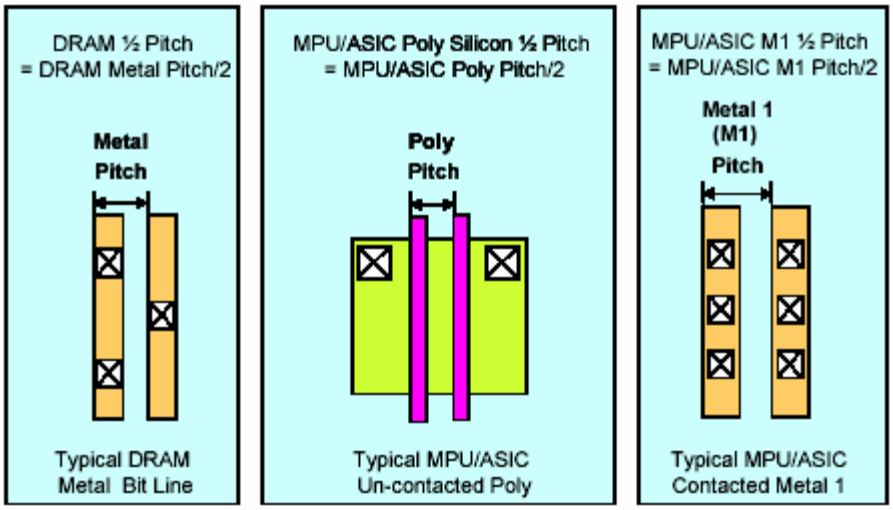

Figure 2 - Definition of Metal Half Pitch

Any of these five parameters (rows) in Table 2 may be chosen as the driver for a given technology requirements table of a given ITWG. Nevertheless, for a point of reference, the DRAM half-pitch is still used in the *latest ITRS* as the designation of the technology node (DRAM still requires the smallest half pitch among all products). For example, according to Table 2, 2004 will be the year of production of the 90 nm node. Again, the "node designation" is defined by DRAM half pitch, not by the transistor gate length or minimum feature size characteristic of that node.

Drivers for ITWG Technology Requirements

The particular lithography-related rows selected for Table 2 are special in that any one of them may be designated by an International Technology Working Group (ITWG) as a "driver" for any specific row in one of their technology requirements tables. For example, the physical gate length may be the appropriate driver for the gate CD control and the source/drain junction depth. The designation of drivers for technology requirements provides some traceable and supportable assumptions for constructing the ITWG's individual tables. It also provides useful links between the ORTC tables and the ITWG tables. Thus, as the Roadmap is updated in subsequent editions, these links will be used for creating a first-pass version of the new tables. For example, if the requirements in one of these driver rows of the ORTC tables were subsequently pulled-in by one year, it would be assumed that rows in the ITWG technology requirements tables would shift by default along with their designated ORTC driver row.

A new cross-roadmap effort was begun this year to integrate the System-level driver needs of the ITRS and the iNEMI Roadmaps. Figure 3 is a model of their efforts. As a result, information is being shared between the iNEMI Product Emulator Groups (PEGs) and the ITRS Design TWG. The ultimate goal of the cross-roadmap work is to integrate the key semiconductor-related requirements (identified in the iNEMI PEG market application needs tables) into the ITRS Design TWG System Drivers, which is also beginning to identify specific semiconductor end-product application needs and develop tables to describe the needs. The initial work this year has identified a relational framework for the iNEMI application markets and the ITRS System Driver System-in-Package (SIP) and System-on-Chip (SOC) Architectures, Chips, and on-chip functional Fabrics (see Table 3). In addition to the cross-roadmap driver framework, the ITRS Design TWG has begun work to examine the specific overlapping requirements which drive the needs of future semiconductor devices. These specific technical needs connections between the two Roadmaps will be developed more fully in the 2005 ITRS Renewal as the relationship between the iNEMI and ITRS PEG and Design TWG cross-roadmap teams continues to develop.

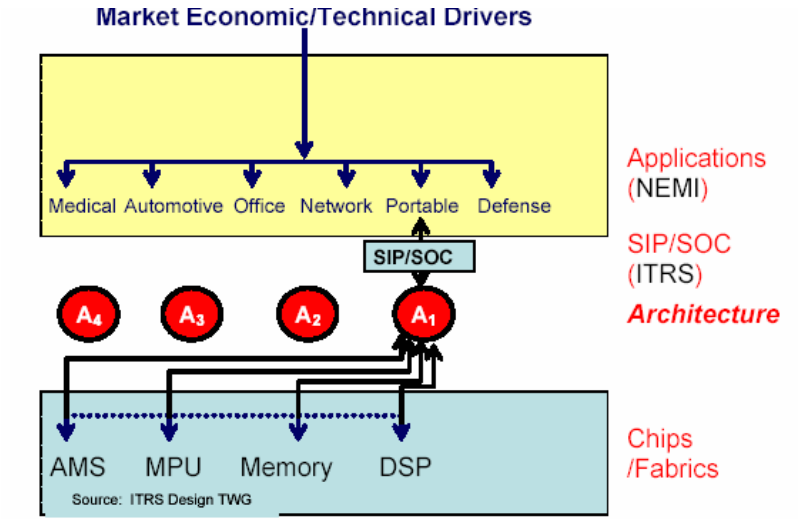

Figure3 - iNEMI / ITRS Drivers

Table 3 - Illustration of Potential References between iNEMI and ITRS Roadmaps

Parameter	iNEMI emulator chapters	ITRS Design chapters
Technology parameters	DRAM pitch MPU pitch Pkg I/O pitch	MPU driver, MPU pitch eRAM driver, DRAM pitch - SoC/SiP driver I/O
Thermal	Thermal design power Highest power chip Chips with power > 10W Module power Current (average)	Active SoC power Standby SoC power
Environmental conditions	Temperature ranges System voltage ranges	Chip temperature Chip voltage supply
Test	BIST	% of logic with BIST

Business Issues

The Semiconductor Industry Association (SIA) has recently released forecast data that indicates the 2004 semiconductor revenues are expected to exceed the 2000 peak level of $204B (dashed square), and the the Semiconductor Equipment and Materials Initiative (SEMI) has recently increased their forecast for 2004 Semiconductor Equipment Revenues to nearly $40B (dashed diamond). At those levels, the semiconductor and manufacturing equipment markets will be on track to 8-10% growth range scenarios, however the exact nature of future business cycle peaks and troughs around those scenario trends remains uncertain. One certainty that drives the semiconductor and equipment technology roadmaps is that we have set a historical expectation for the global consumers that our industries will continue to provide incredible product value by doubling functionality and speed approximately every 2 years. This concept has become known as “Moore’s Law,” based on observations of Gordon Moore of Intel Corporation, and is a key driver of the technology needs of the Silicon Roadmap as noted below.

A key measure of the pace of the semiconductor technology which enables the delivery of “Moore’s Law” capability is the interconnect half-pitch and the transistor gate-length. Both of these key attribute needs are analyzed in detail below. It is worth noting here in the Situation Analysis that starting in 1998, the leading-edge half-pitch has accelerated from a historic 70%/3 years reduction rate to a 70%/2 years reduction rate and that rate is expected to continue through 90nm in 2004. To a large extent the half-pitch acceleration enabled the semiconductor industry, and the electronics industry which it supports, to survive and thrive in the recent history of tightening product margins and slowing revenue growth.

The present ITRS and iNEMI Semiconductor Roadmaps anticipate a return to a 3-year pace of the half-pitch and gate-length, however it remains to be seen if the resulting slower levels of productivity and performance will be adequate to meet the economic and performance needs of the global consumer.