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VIGOR European Project
New Industrial Applications in 3-D Interconnection

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Abstract
The 3-D interconnection and packaging emerged from the last decade. Today, the 3-D interconnection technologies are becoming mature and their reliability assessed. 3-D technology constitutes the technical core of the VIGOR project which is integrated in the European Framework 5 Research & Technology. This European project is called VIGOR for Vertical InteGration for Opto and Radio (sub)systems. Thanks to the work performed by the consortium members the performance of the 3-D module will be significantly improved. Applications proposed include the stacking of a wireless module for automotive, integrating digital levels and a high-frequency level. The applications developed will integrate opto-electronics functions, i.e. containing optical, opto-electronic as well as electronic parts. To the best of our knowledge, no 3-D module supplier proposes today these types of applications. As a scientific expertise, thermo-mechanical together with finite element modelizations and simulations are very crucial. The purpose of this paper is to review with emphasis the different techniques of 3-D module manufacturing and to focus on the technological developments and the reliability tests performed up to the mid-term of the project.

Introduction
The continuous demand for more and more integration in electronic packaging leads to the relevant industries to push the limits of components and interconnection techniques and to develop innovative solutions. Three dimensional techniques, stacking several layers of circuitry, are a very interesting way to increase functionality while keeping the electrical connections short. The System On Chip (SOC) and System In Package (SIP) concepts are gaining interest because a complete tested function is proposed to end users rather than bricks to be assembled separately. System on Chip concept could be an attractive solution because it presents the ultimate integration level, using the very high density silicon processing techniques. However, SOCs are often more cost effective to combine several standard parts manufactured in high volume, and time to develop is higher than SIPs. For the most advanced complex ICs (SOCs), the available design and test software may not be adequate. Due to these reasons, the SIP concept is more and more attractive in comparison with the SOC one. It is considered as the fully integrated solution and/or the only cost-effective and technical solutions.

Since the last 10 years, the 3D packaging and interconnection have emerged and developed integrated packages. 2,5D-SIP techniques are appearing in standard BGAs, in the form of a "stacked die package". This technique is an interesting extension of the semiconductor packagers capabilities. However it is limited to very specific applications because the chips have to be designed together. Another possibility is the "few die package", using the same assembly level, and which can include other kinds of components, like passives. This in turn can become a 3D-SIP module if several levels are stacked. This is the objective of the project VIGOR to improve the best existing 3D concept and develop techniques making it versatile enough to allow for various functions integration including optical or wireless functions, in a robust, green and cost-effective way, manufacturable in volume.

Starting from the niches markets, the 3-D technology has reached a maturity. The particularities of the 3-D technology developed by 3D PLUS and recently integrated into a Framework 5 R&T project and called VIGOR for Vertical InteGration of Opto electronic and Radio (sub)systems. This project has started on April 2002 and will finish on April 2005. Thanks to

the work performed by the consortium, constituted by SOLECTRON for volume production part, FIAT (CRF) and BAE SYSTEMS end-users, the performance of the 3-D module will be significantly improved. The applications proposed by FIAT (CRF) will include the stacking of a wireless module for automotive, integrating digital levels and a high-frequency level. The applications developed by BAE SYSTEMS will integrate opto-electronics multimedia functions, i.e. containing optical and opto-electronic parts as well as electronics. From our knowledge, no 3-D module supplier proposes these types of applications. As scientific support, Bordeaux University – IXL Laboratory will carry out thermo-mechanical simulations which are very crucial, and environmental tests. This technique and industrial approach is quite ambitious as it couples automotive and avionics applications specialists with the number one world-wide for surface-mounting manufacturing and a small company, 3D PLUS. The VIGOR project is clearly oriented to the industrialisation of the process then collective process and cost savings are challenged. This project is composed by several tasks which are technical developments, reliability tests, modelization and simulation by finite element of thermo mechanical and thermal constraints, wireless and opto electronics applications. Each of the five partners are responsible of one task; for example 3D PLUS is in charge of technical developments task, and IXL laboratory is in charge of reliability analysis and modelization one. Since April 2002, the mid-term is reached and some significant progresses has been assessed in terms of technical developments and cost saving. The consortium has specified, designed and manufactured some test vehicles in order to evaluate new raw materials and to perform the 3D process; these developments are presented and discussed.

State of the art on 3D technology

Since a few years, new interconnections in 3-dimension technologies have appeared, most of them pulled by mobiles telephone markets. In order to position and compare them, we propose a new classification of all the 3-D interconnection technologies (see Figure 1). The 3-D interconnection, which was first developed to stack memories, is progressively applied to the stacking of heterogeneous components (active and passive components) in order to build Systems in Package. An important differentiation in the processes used for the interconnection is given and driven by the maximal temperature of the process:

- Cold process: the temperature is inferior to 150 °C
- Hot process: the temperature is higher than 150°C.

"Hot" process: This process is used by most of the companies which stack packaged dice (TSOP, µBGA, CSP). Some others use flip chip bare dice, mounted on a substrate; this necessitates high temperature reflows. Those who use a folded flex, mount flip chip or micro BGA by reflow and will be forced, because of the coming of leadless soldering to use alloys at a much higher temperature. It can observe that the interconnection technique which is based on a dipping in a soldering bath or on a furnace reflow soldering, will considerably penalise for these techniques, since the coming of leadless soldering significantly increase the melting temperatures (between 30 and 40°C). As a consequence, these techniques will be forced to use solder alloys with higher melting temperatures in order to avoid their reflow during the mounting of the cubes on the PCB by their customers, thus leading to having working peak temperatures inside the reflow furnace comprised between 280°C and 300°C; this will significantly weaken the components and sometimes even be unacceptable. These techniques should be modified to a new process to overcome this difficulty.

"Cold" process: Only three techniques can be found in this category. One company uses a process based on a conductive glue, and two others companies use a process based on a plating which can also be named « Bus Metal ». In this configuration, the components are not overheated during the process and by consequently the process is full compliant with lead free assembly. These two companies can stack any kind of components in order to build real Systems in Package.

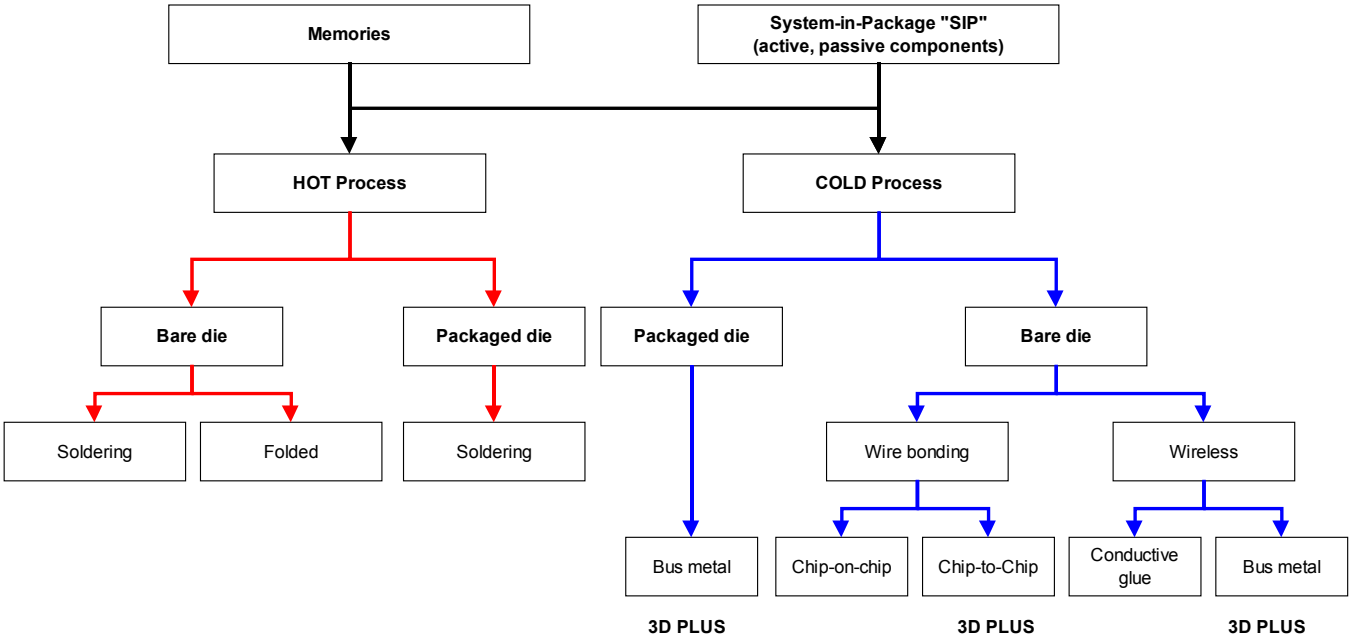


Figure 1 - Classification of 3D Interconnection Techniques

3-D process

The specific advantages of the 3D PLUS technology (hereafter referred to as 3D) are presented, compared to the competitive technologies. The main key challenges are:

- Cost of raw material as low as possible,
- Process compliance with dual stacking packaged dice and bare dice,
- Electrical tests of each level before stacking in order to get an excellent yield and use commercial dice,
- Keep a "Cold" process.

The 3D interconnection technique contains 6 main steps (as a comparison, there are 20 to 25 steps with some competitors).

1. Packaged dice / bare die on Tape so called Chip On Tape,
2. Stacking / moulding,
3. Cutting with dicing machines,
4. Nickel/Gold wet plating, this technology is around 50 years old and is perfectly mastered from the PCB technology,
5. Laser Direct Patterning,
6. Final electrical testing

The Chip On Tape is well known. It allows using printed circuit boards, with one layer to two levels, exceptionally with four levels, in the case of very quick signals. The pitch of the conductors required by the pads area of the packages is compliant with the pitch for interconnection (0.635 mm). This is not the case with the new folded packages which require flex with small pitches (around 50 microns); the electrical adaptation of such packages is difficult and the variations in the velocity of propagation lead to electrical integrity problems.

The moulding of the stacked components allows to protect them; many companies stack the components without moulding the 3D module. Another advantage of the moulding is that it prevents the penetration of soldering flux and all outside substances such as dust which, linked to humidity, can develop leakage current. Lead-less solder alloys lead to high reflow temperature and the flux is more and more difficult to remove at the level of the PCB. After mounting, when the PCB is cleaned, the flux could penetrate inside the non-moulded cube. The resin can induce residual constraints on the components after moulding; but the coefficient of thermal expansion is matching with printed circuit board and plastic components ones.
The plating allows to interconnect the different levels between them, by using the shortest path. These metallic bus have a very low electrical resistance and a very low inductance. This is what makes 3D different with regards to both the Chip-On-Chip techniques (length of wires could be up to 6 to 7 mm) and the folded packages.

The laser direct patterning constitutes a significant technical advantage in terms of cost, with an unique etching operation (beam speed: around 3 meters per second). It is possible to perform in one step what is generally done in 5 operations when a photo etching is used.

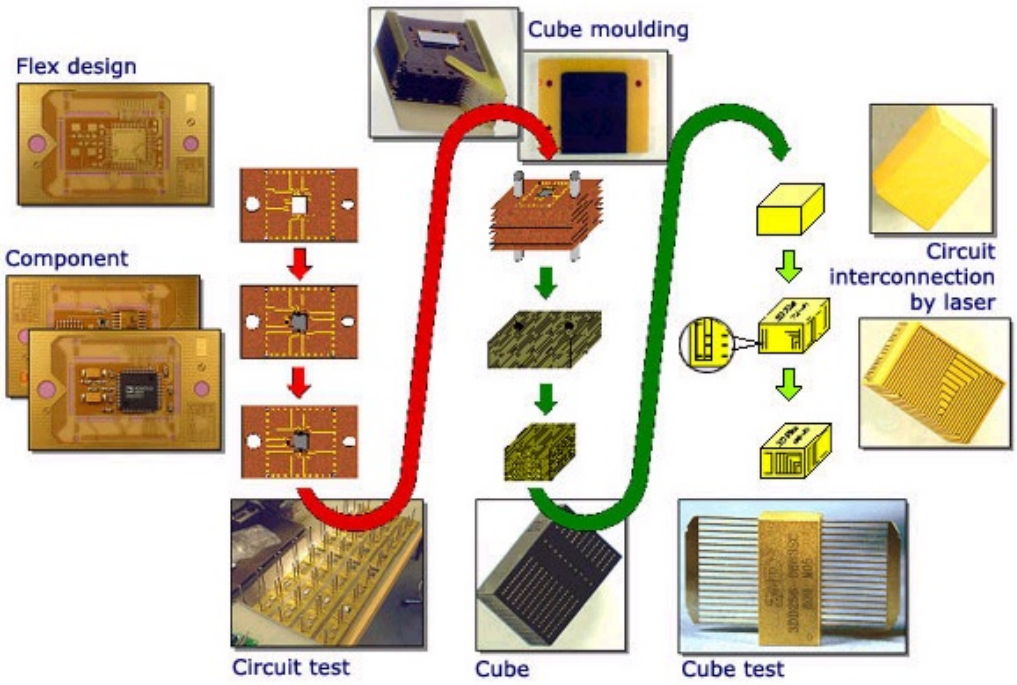


Figure 2 - Process Flow Chart

VIGOR project objectives

At the beginning of the proposal, some main objectives have been defined following our knowledge and technical roadmap on the high density package. The driving forces are clearly presented as the industrial developments in term of production and to demonstrate the compliance of this technique with new applications as opto electronic and wireless. Consequently, the main objectives are:

- To develop a robust and versatile, novel module technology combining the advantages of System In Package integration with vertical integration and allowing the use of any kind of active and passive components.
- To provide industrial capabilities for high integration of various functions, particularly opto-electronic and wireless, in a cost-effective module, manufacturable in volume.
- To develop 3D design for manufacturing and assembly (DFM and DFA) analysis
- To design and to manufacture demonstrators integrating opto-electronic or wireless functions.

The major task consists in improving the basic technology steps with the view to future volume manufacturing.

Technological developments

This part is dedicated to the industrialisation of the manufacturing process. The Figure 3 represents all the technical activities which have to be performed to get a process with a real potential for volume production.

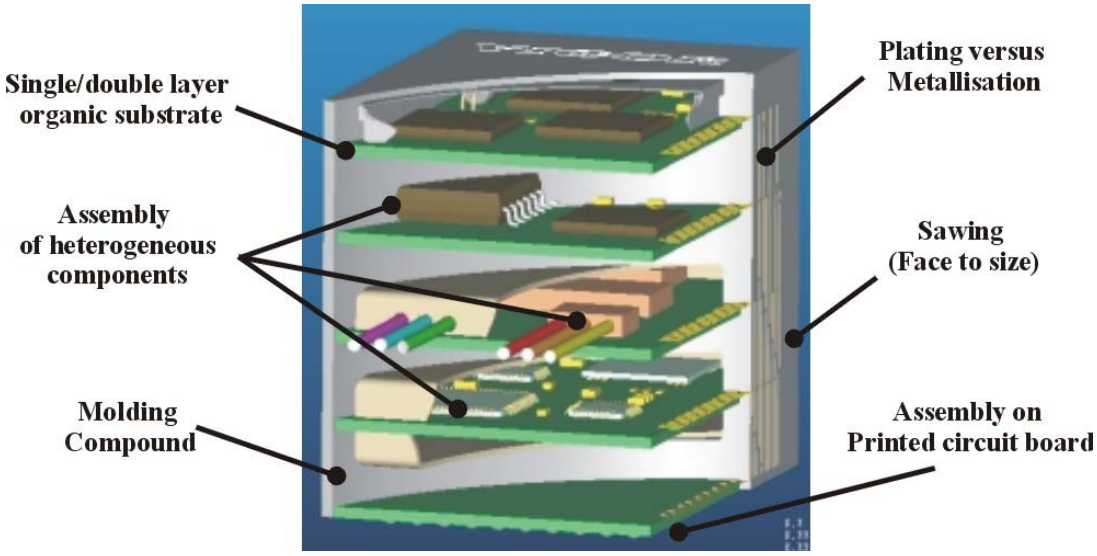


Figure 3 - Major Steps for Industrialisation

The three different key points can be pointed out from the current manufacturing process: PCB technology, moulding compound, and plating/metallization. The specific PCB technology consists in performing flying leads at the level of the cutting window. Today, two PCB manufacturers (in Europe) have been qualified. This situation is not suitable for in-line production (see Figure 4). Moreover, this reliable technique is relatively expensive. The strategy is to develop a new technique compliant with the current techniques and process, more cost effective and increasing the number of sub-contractors. The solution is to create a homogeneous path for the laser patterning thanks to an oblong hole technique. This technique is based on a mechanical or laser drilling between two consecutive copper tracks (see Figure 5). That permits getting the same configuration as flying lead excepted below the copper track; but it should be not a concern for the reliability. The advantage is the cost savings which is estimated around 10 times lower than flying lead technique. Moreover, there is a larger sub-contractors for the printed circuit board manufacturing. The first results are full of promise and some Generic Test Vehicles have been built with this technique for a complete evaluation.

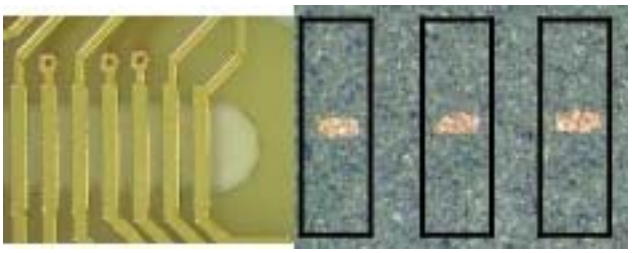


Figure 4 – Flying Lead Techique

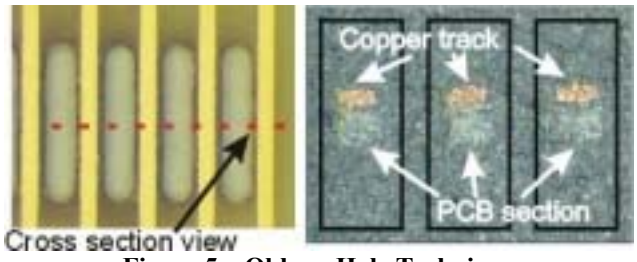


Figure 5 – Oblong Hole Technique

The electronic component (bare die or plastic package) encapsulation requires high performance moulding compound: high glass temperature (Tg), low coefficient of thermal expansion (CTE) and high chemical purity. At the moment, an epoxy resin has been qualified for space and aeronautic applications. This is an old chemical generation and high cost resin, is unacceptable for in-line production. New moulding compound sources must be evaluated, in particular low cost, new chemical systems exhibiting high Tg and for low curing temperature range. The plating process (electroless deposition of nickel followed by electrolytic deposition of nickel and gold) is subcontracted. It is a wet chemistry and needs a continuous control of the different chemical baths. This technical step is identified as a bottleneck for the cube industrialisation. The

evaluation of an industrial and collective plating process is necessary and the PVD plating deposition process seems to be very attractive. This process is planned to be developed internally. Basically, it requires a 6-8 hours lead time and 800 – 1000 modules can be treated per batch; it's fully compliant with the industrial target. The Figure 6 represents, in detail, all the parameters which are evaluated and tested during these developments. Some basic technical modules are designed and manufactured in order to evaluate the technical improvements. These modules will be tested to validate the electrical integrity of vertical interconnection and obviously the compatibility of all new materials.

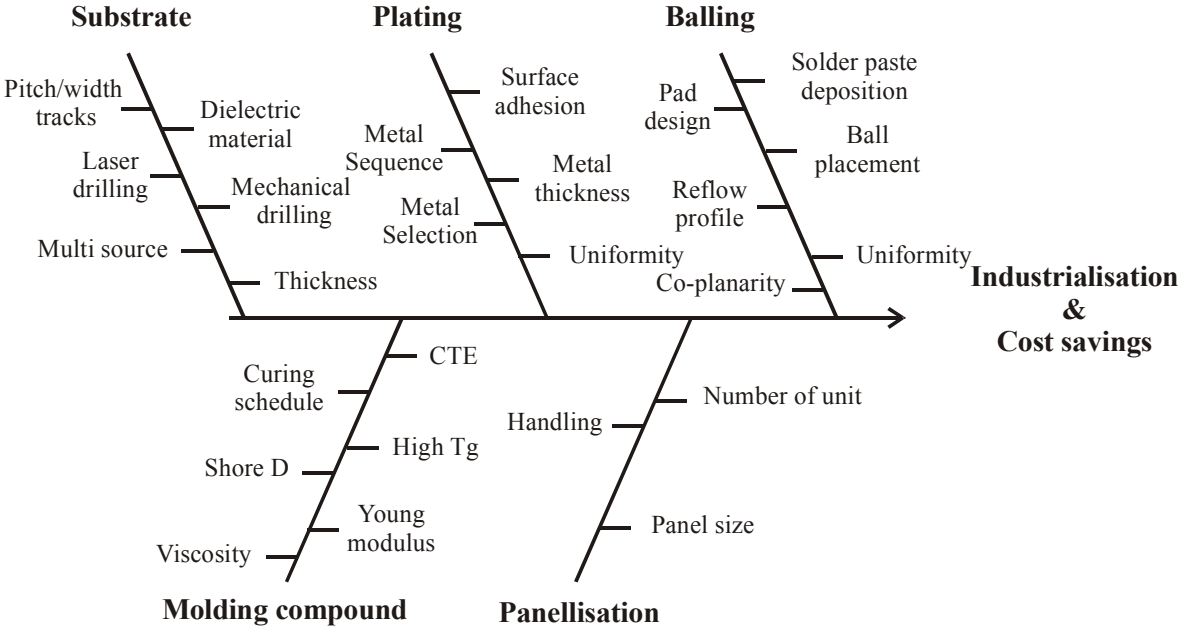


Figure 6 - Technological Development Parameters

Generic test vehicle description

The objectives of the Generic Test Vehicles (GTV) are to evaluate the new techniques and materials in order to industrialise the 3D process and to get a cost saving. On this way, the substrate is studied in terms of dielectric material and structure; the objective is to define a substrate without flying leads which are settled as a real bottleneck for manufacturing and cost. The moulding compound is studied to look for an improvement for thermo-mechanical performances, manufacturing cycle time and cost. The last step is the plating which has to be defined as a collective process in line. These three points constitute the base for the definition of the Test Vehicles. Concerning the end-users, the Test Vehicles have to permit a functional evaluation.

Two raw dielectric materials have been selected: the material S1 is based on epoxy with aramid fibre and the material S2 is based on BT epoxy (Anti-CAF) with glass fibre (see table 1). These materials are different in terms of adhesion between fibre and epoxy dielectric and mechanical behaviour. Three moulding compounds have been selected: the material M1 is the current and qualified compound. The material M2 is similar to the material M1 in terms of physical characteristics and but is cheaper. And the material M3 is characterised by a higher hardness and lower coefficient of thermal expansion (see Table 1).

Table 1 - Raw Material Properties

Parameters	S1	S2	M1	M2	M3
Coefficient of thermal expansion (x/y/z) ppm/°C	11/11/110	12/12/55	22	19	32
Young modulus G Pa	14.5	30	12	11.5	6
Poisson's coefficient	0.49	0.15	0.26	0.26	0.26

The GTV modules defined following the DOE matrix on the Table 2. The plating study has been removed from this first set because the PVD equipment is under up grading. The GTV modules are defined by 5 levels populated with passive components, daisy chain components and bare silicon dice (see Figure 7). The GTVs are dedicated to the evaluation of substrates and moulding compound.

Table 2 - Test Vehicles definition

	Substrate material		Moulding compound			Plating	
	S1	**S2**	**M1**	**M2**	**M3**	**P1**	**P2**
GTV1	X		X			X	
GTV2		X	X			X	
GTV3		X			X	X	
GTV5		X		X		X	
GTV6	X			X		X	
OETV	X		X			X	
WTV		X	X			X	

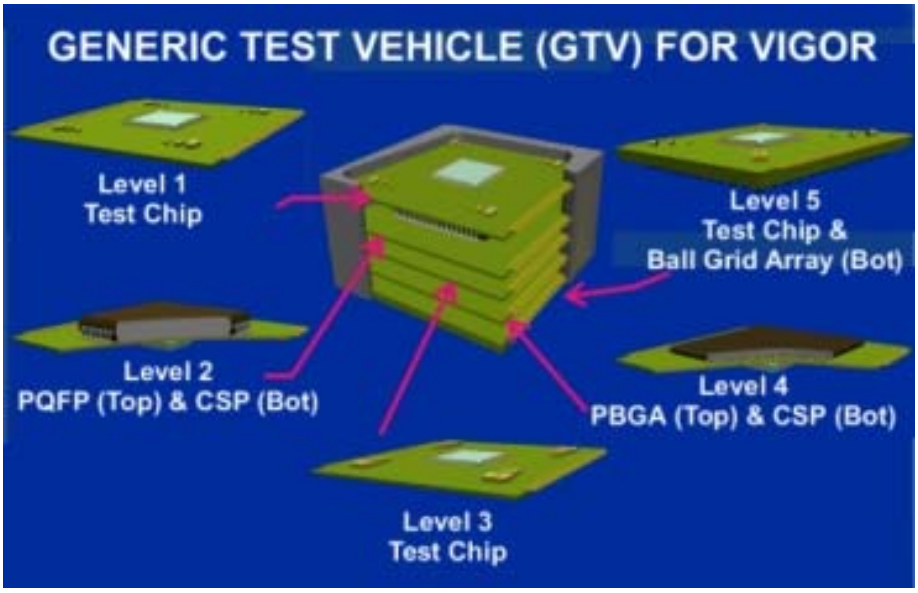


Figure 7 - GTV Description

The Test Vehicle for opto-electronic (OETV) is considered as an hybride module because it is manufactured with two parts. The first part uses the same levels as the generic Test Vehicle: levels 2, 3, 4 and 5. The second part is an opto electronic level. One of the challenge is to assemble these parts. The assembly of this vehicle, on motherboard, is based on an interposer because of temperature limitation due to optoelectronic devices.

The overall dimension is 35x35 mm square. In fact, it depends on the number of I/Os used to the vertical interconnection, on the one hand, and on the final dimension for the module, on the other hand. The pitch for vertical tracks is 0.635 mm; 200 In/Outputs have been required to complete the vertical interconnections for the GTV and OETV modules, that means 50 In/Outputs per face. The levels 1, 3, and 5 are populated with the same test die, with four groups of three capacitors (1206, 0805, 0402 formats - X7R type) and a resistor (0805 size, 2.87 k Ohms). It allows to get a symmetrical module in order to be closed to the modelization and the simulation results. The ceramic capacitors have different orientation on each level: XX on level 1, YY on level 3, and XY on level 5. Concerning the silicon die, the corrosion tracks, the heaters and diodes and the daisy chains are used on each die. We expect to measure the humidity sensitivity, the thermal conduction and dissipation, and to evaluate the thermo mechanical stresses on the top, the middle, and the bottom levels of the module. The level 2 is populated by: a fine pitch PQFP (Plastic Quad Flat Pack) with 176 leads, 0.40 mm pitch, 20x20 mm body size, a CSP (Chip Size Package) with 46 eutectic solder balls, 0.75 mm pitch, 6x7 mm body size. The level 4 is populated by: PBGA (Plastic Ball Grid Array) with 169 eutectic solder balls, 1.50 mm pitch, 23x23 mm body size, a CSP with 56 eutectic solder balls, 0.50 mm pitch, 6x6 mm body size. The PBGA is the largest component (27x27 mm) and its location is defined to be closed to the Wireless demonstrator's partitioning. The final down level (level 5) is also populated, on the bot, by a BGA with 624 hard solder balls, 1.27 mm pitch.

Its overall dimension is critical in comparison with the module one (35x35 mm). Some daisy chains will be defined on the corners in order to test the vertical interconnection reliability.

PCB Layout Designs

SOLECTRON is in charge of all the PCB layout designs thanks to its capabilities in CAD tools and design guidelines. The flow chart describes the different steps from Test Vehicle definition to manufacturing ‘see Figure 8). At first, the electrical schematics have been done in order to connect each net to a ball; it takes into account the schematic on each level and obviously the vertical one. Afterwards, the design is managed by Cadence tools. The design of vertical interconnection is realised as PCB design due to the electrical schematic. 3D PLUS is in charge of the validation of each design in order to verify the compliance with specific 3D design rules. The final step is to analyse the designs for manufacturability (DFM), assembly (DFA) and test (DFT). The DFX is supported by Valor Trilogy software which is linked to a powerful data base. Each circuit is panellised by 4 to optimise the assembly. The GTV schematics capture has been done on ViewDraw from Innoveda (Mentor Graphics). The approach was to build a hierarchical architecture in order to be able to have a global net-list of the entire 3D structure with a top level for the Z axis interconnection diagram and a break-down of schematics for each layer (cf. Figure 9). At the top level of the hierarchy each layer is considered as a component. The entire module is then assigned to a macro component that can be used in the final application with a possibility to go down in the schematic of the module itself during the design of the final product. The Figure 10 illustrates the design of a representative level. The two mechanical holes for stacking has a 58 mm distance centre to centre. And the overall dimension is 72x45 mm. The designs of the vertical interconnections are symmetric and some tracks are not connected for the GTV because there are dedicated to the OETV (see Figure 11).

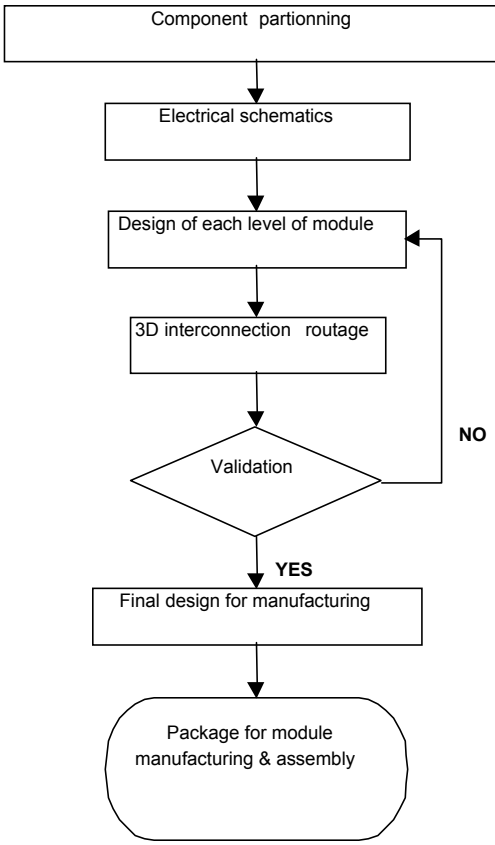


Figure 8 – Design Schematic

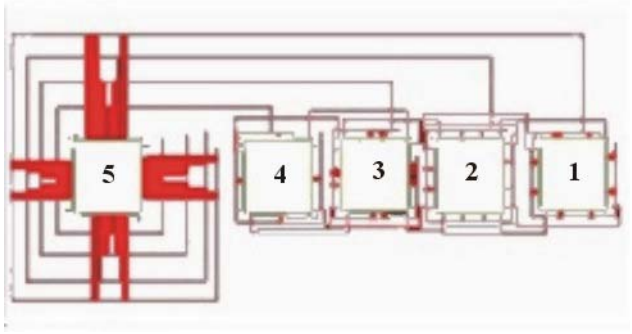


Figure 9 – Global Schematic

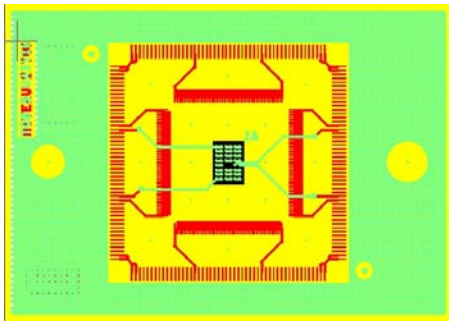
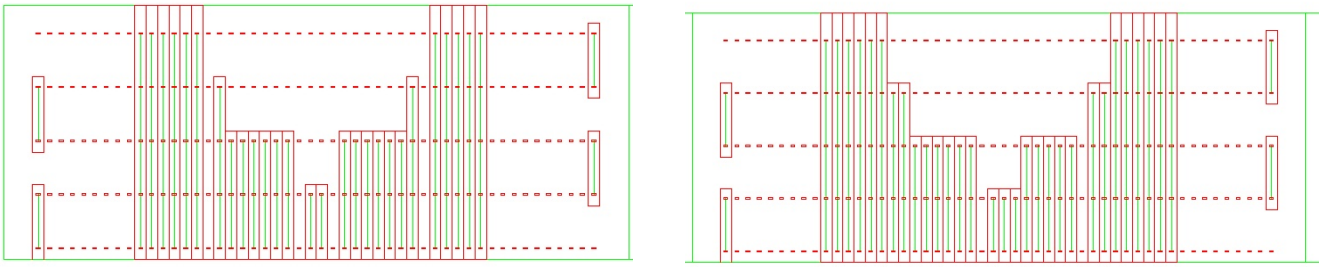


Figure 10 – Layout of Level 2
(Red: top side, Green: bottom, Black: soldermask)



Vertical interconnection on faces 1 & 3 Vertical interconnection on face 2 & 4

Figure 11 - Vertical interconnections

An abstract on the generic design rules are:

- Unplated holes for the flowing of resin between levels
- Through holes on the level 5 are covered by soldermask in order to avoid any flowing of resin on the solder balls
- Reduce the area with soldermask because of a weak adhesion of the moulding compound on such material
- The pitch of copper tracks is 0.635 mm; 0.20 mm width

Assembly & GTV manufacturing

Following our procedures, a visual inspection is done on all panels. Concerning the components, this step is dedicated to the bare dice mainly. The PCBs and plastic components are baked to prevent any kind of humidity issues during assembly (see Figure 12). After assembly, an X-rays inspection is done on each ball grid arrays components (PBGA, CSP). Concerning the levels 1,3 & 5, a Chip-On-Board process is made with die attach, wire bonding, and Dam&Fill encapsulation. As regards to the level 5, a balling process has been defined to populate the bottom side with hard solder balls (90Pb/10Sn). Hard solder ball are specified due to the expected weight of the module; then during the reflow step, the stand-off between motherboard and the module is controlled. All circuits are routed from the panel and a final electrical test is done. The traceability is ensured by a bar code which is attached on each circuit (cf. Figure 13). Therefore, there is a specific label for each circuit. It permits to get a full traceability and then to extract quality report. All levels are Surface Mount Technology. Concerning the levels 1,3 and 5, there is a mixed process which includes SMD for passive components and Chip on Board for bare dice. The assembly prototype line is presented on Figure 14. The reflow profile has been optimised and it reached a unique profile for

the top and bottom sides. A motherboard is designed to measure the electrical performances of the modules during the environmental tests.

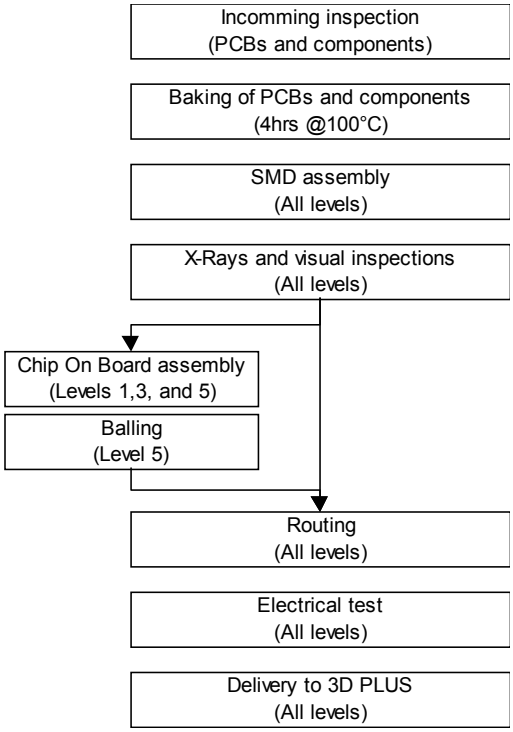


Figure 12 – Flow Chart of the First Level Assembly

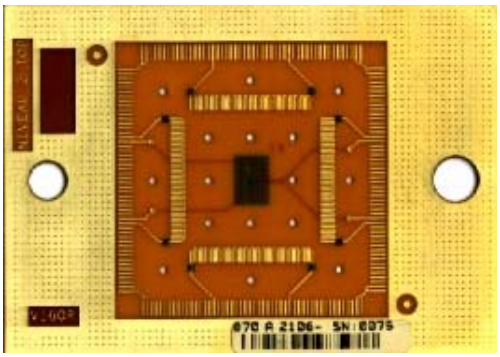


Figure 13 – Bar Code on the level 2 (ID 870), BT Epoxy Dielectric (SN75)

Screen printing
Stencil: Electro-formed screen with 150 µm thick excepted to level 2bot and 4bot (125µm)
Equipment : DEK infinity 265

Placement
Equipment : Europlacer EP600
Tool : carrier

Reflow
Equipment : Paragon P150
Tool : carrier

Figure 14 - Typical Assembly Prototype Line

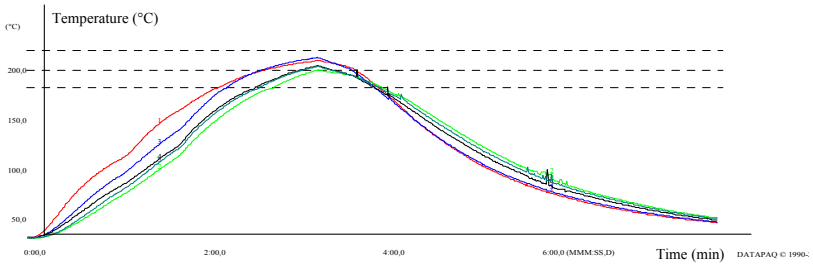
Balling process

Another critical task that has been developed within VIGOR project was solder ball attachment on substrate. This process is generally used by components manufacturers and not SMT assemblers. For this project new equipment, called Tin-Up from Applied Microtech which is dedicated to BGA/CSP components solder balls removal and re-attach, was evaluated. This equipment is well adapted to prototype and low volume activity. A view of the equipment is given in Figure 15. Manufacturing had a first experience on eutectic (63Sn/37Pb) solder ball attachment at prototype level but no experience at all on hard ball (90Pb/10Sn) process. VIGOR project gave us the opportunity to develop hard ball attachment process. A description of the solder ball attachment process flow is given.

As Level 5 of GTV was out of standard size specification of Tin-Up equipment, special tooling was designed internally and manufactured to be compliant with the equipment reflow area. Mini-stencils 200µm and 250µm thick were made by laser cut and were used respectively for solder paste printing on substrate and solder ball (90Pb/10Sn) deposit. Water soluble Alpha Metals WS609 solder paste was used for paste printing. Solder balls were deposit under vibration system. Clamp shell and fixture were also developed to allow substrate handling during reflow operation.

Figure 15 - View of Tin-Up Equipment Dedicated to Solder Balling

Before any solder ball attachment, process had to be set-up and optimised reflow profile had to be defined (see Figure 16). For that purpose, a dummy substrate was mounted with thermocouples and temperatures were then recorded. Due to the large size of the substrate, a thermal gradient equal to 9°C was obtained from one ball to another one. Peak temperature was varying from 201 to 210°C and time to reflow (at 183°C) was varying from 73s to 107s which are classical time from rework station. From this first experiments where more than 50 substrates had solder ball attachment, we obtained a yield after first assembly equal to 87%. Defects were attributed to solder pad lifting on 3 substrates. This phenomenon is probably linked to weakness in adhesion between copper and dielectric in the PCB substrate and study are now ongoing to understand the root-cause of such defect. The major process defect was lack of reflow of solder paste and it was explained by an imperfect heat transfer from heater to component due to co-planarity problems. During these trials, we noticed also that tooling and stencil cleaning was a major parameter. In the following works, optimisation of the balling process has to be performed together with characterisation of the solder joints: solder joints strength measurements by shear test, solder ball co-planarity and centring.



	Peak Temperature	Reflow Time
External ball	210 °C	107s
Center ball	201 °C	73.5 s
External ball	203.5 °C	99 s
Internal ball	205.5 °C	81 s
Internal ball	204.5 °C	81 s

Figure 16 - Reflow Thermal Profile Defined for Solder Ball Attachment on GTV Level 5

Test vehicle manufacturing

During manufacturing of test vehicles a problem occurred: the pads' lifting during removing a RTV protection after wet plating. It has been observed that the pads incriminated are none functional one, that is to say not connected to via. The encountered problem is linked with the weakness of copper pad adhesion observed during the balling process.

Second level assembly

The second level assembly is driven by a motherboard and a module. The physical characteristics of the GTVs, 43 grams and 22 mm height, lead to select some specific pick & place equipment's. On the Bordeaux site, there are two equipment's which are compliant with these specifications: a Panasonic and a Fuji QP2. Thanks to these machines, the module can be picked and placed with a suction nozzle. To our specific application, we have defined a custom nozzle. We have decided to use the Fuji QP2 with a custom nozzle. The assembly has been produced on a typical production line: screen printer, pick and place, reflow oven. The optimised reflow profile is illustrated in the Figure 20. The challenge is to establish some temperatures in order to obtain the following criteria:

- A reflow duration (above 183°C) between 30 and 90 s
- A maximal reflow temperature between 200 and 235°C

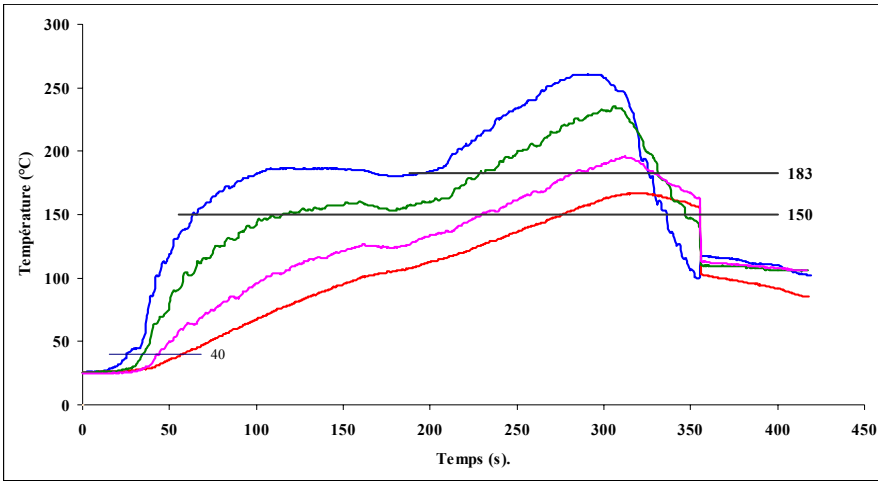
In order to measure the temperature on the motherboard, closed to the solder balls and inside the module, some thermocouples have been used:

- On the motherboard
- Inside the module (on level 1)
- Closed to the solder balls located on the centre of the BGA
- Closed to the solder balls located on peripheral of the BGA

The temperatures of each oven's zone are different between the top and the bottom heaters in order to limit the temperature inside the module. The Paragon P150 has 10 zones:

	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5	Zone 6	Zone 7	Zone 8	Zone 9	Zone 10
Top heater temperature (°C)	**180**	**200**	**200**	**190**	**190**	**190**	**240**	**260**	**280**	**260**
Bottom heater temperature (°C)	**210**	**210**	**210**	**190**	**190**	**190**	**250**	**280**	**290**	**290**

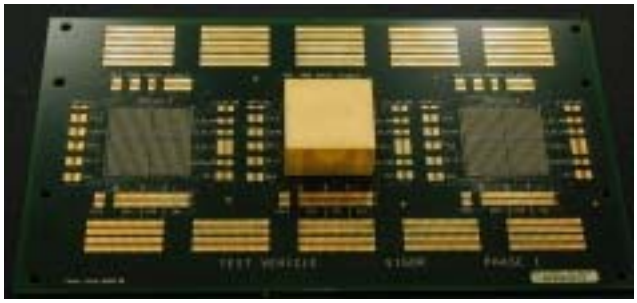
Some thermal gradients between the central solder balls and the peripheral ones and inside the module (orange curve) are measured. There is a gradient of 43°C between the centre and periphery solder balls (see Figure 17). The temperature on the motherboard goes up to 265°C. This temperature is to high for a populated card with others active and passive components; this observation should be discussed and the solder ball's distribution will be studied in order to reduce the thermal gradient and fortunately the temperature on the board. We notice that the temperature on the level 1 is around 170°C which can occur some defects on the die and more especially on wire bonding.



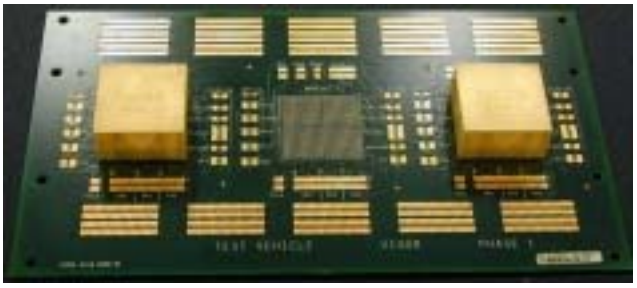
Blue curve: Motherboard surface temperature
Green curve: Peripheral balls temperature
Pink curve: Central balls temperature
Orange curve: Internal module temperature

Figure 17 - Flow Profile

With regard to the assembled modules, the electrical test is completed. Some straps have been managed on the motherboard to repair some modules. These defects are appeared after the assembly, then it could be due to the thermal stress induced during the reflow. The assembly on motherboard are illustrated on the Figure 18.



1 GTV module on 1 motherboard



2 GTV modules on 1 motherboard

Figure 18 - Module Assemblies

Environmental Tests

The environmental test strategy is based on the thermo mechanical stresses only because different materials are evaluated mainly. The reliability of the vertical interconnections, the internal connections and the solder ball connections are specifically evaluated. Next to this first set of vehicles, the functional demonstrators will be defined, manufactured, and qualified with power on tests. Then a qualification step with 500 thermal cycles (+125°C/-55°C – slope 5°C/min – stage 20 min.) are followed by an evaluation one up to 1500 thermal cycles. As it describes on the Figure 19, humidity tests are managed; it's a cumulative test. After the 500 thermal cycles, all the materials (moulding compound, plastic components, substrate,…) are aged; it supposes the initiation of cracks and voids. During the humidity test, the water ingress is promoted by the weak areas such as micro cracks either on the plating or inside the moulding compounds. Moreover, the selected sequences are defined to allow a comparison with the JEDEC 020B standards. No standard is able to give baking conditions for such large plastic body package. A reference of each series is kept at room temperature.

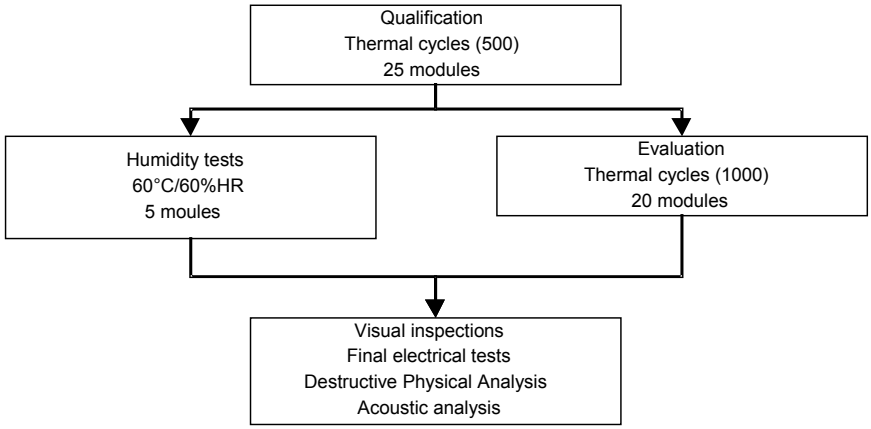


Figure 19 - Environmental Test Flow

The measurements are made every 100 cycles. Concerning the global results, no evolution has found in the frequency response of the capacitors an the resistors. The other results are gathered in the table 3. We can notice four kind of failures:

- Ones are considered as early failure as they are detected before the thermal cycles (t0) or after only 50 cycles (t+50). They are not significant for the qualification plan because they are considered as infant mortality of failures due to the assembly stress and the encountered problem on copper pad adhesion of the level 5.
- Ones internal failures of the module are reported. This concern only one kind of failure: wire bonding between two corrosion tracks of the test die detected on level 1 and 5.
- Ones can not be distinguished between a solder ball failure or an internal module failure on level 5 only.
- Ones are reported due to a ball solder joint.

Thanks the vertical interconnection, it's possible to discriminate between an internal failure and solder ball one. It manages a manual measurement directly on the vertical tracks. It's impossible to do this measurement on the level 5 because the connections are embedded on the substrate. The wire bonding failures are mainly related to the test die located on level 1 and 5 and never on the level 3. The vertical interconnections present any kind of defect. Concerning the SMD assembly, no defect is identified. For both internal failures and solder ball failures, some destructive physical analysis would be useful to validate and to locate exactly the defects. It must be noted that die was identified as a high stress region in previous thermo

mechanical simulations. Eight modules have passed the qualification without any defects: GTV2 series. The GTV1 and 6 series are minor defects.

The S1 substrate exhibits a good behaviour associated with the M1 and M2 moulding compounds. The S2 is compliant with the M1 moulding compound only. About the moulding compounds, the M1 has confirmed its high reliability. The M3, characterised by the higher CTE (32 ppm/°C), has the worst behaviour. These tests have validated the high stress located on the level 1. Thanks to the theory of stratified, the assembled module is characterised by a neutral plan of stress which is located between the level 3 and level 4. Because no failure has been checked on these levels. On both sides of this neutral plan, the absolute stresses increase. This approach allow to understand the high areas of stresses which are located on the level 1 and on the level 5 and on solder balls area. Moreover, the thermal measurements have shown a high temperature on the top of the module, the level 1. The second step of the validation plan: "packaging evaluation" is actually in progress. This step consists of thermal cycles up to 1500 cycles with measurements every 250 cycles. Only 13 modules from the initial set of 19 modules were kept for this packaging evaluation.

Table 3 - Results after 500 Thermal Cycles

GTV	Materials	Status
1	S1 + M1	Passed
2	S2 + M1	Passed
3	S2 + M3	Failed on level 1 & solder balls
5	S2 + M2	Failed on solder balls
6	S1 + M2	Passed

The other six modules are dedicated to the moisture sensitivity classification test in conformity with the IPC/JEDEC J-STD-020B standard; it attempts an equivalent JEDEC classification for this kind of module which are not taking into account in this standard yet. After a baking period of 24 hours at 125°C the modules are exposed at 60°C/60%RH conditions followed by 3 reflow steps, then electrical test will be performed. The process is resumed in the Table 4. An additional humidity test is realised with level 2 conditions. The GTV1, GTV2 and GTV3 modules have been submitted to the last test even if they have been stressed by 60°C/60%RH test before. The driving force is the behaviour of raw dielectric material which is major way for the humidity diffusion. The S1 (GTVs 1 and 6) and S2 (GTVs 2,3 and 5) are represented on the matrix.

Table 4 - Humidity Test Description

Process	GTV1	GTV2	GTV3	GTV5	GTV6	JEDEC level
Baking @125°C – 24 hours	X	X	X	X	X	
20 hours @ 60°C/60%RH		**X**				
3 Reflow cycles		**X**				**4**
40 hours @ 60°C/60%RH	**X**		**X**			
3 Reflow cycles	**X**		**X**			**3**
120 hours @ 60°C/60%RH				**X**	**X**	
3 Reflow cycles				**X**	**X**	**2a**
Baking @125°C – 24 hours	**X**	**X**	**X**			
168 hours @ 85°C/60%RH	**X**	**X**	**X**			
3 Reflow cycles	**X**	**X**	**X**			**2**
Visual inspection	X	X	X	X	X	
Electrical tests	X	X	X	X	X	

Generally most of the plastic packages are specified as JEDEC level 3. That means the floor life of SMD duration before re-bake is 168 hours (1 week). This duration is compliant with the lead time of current assembly process. But the aim of the qualification is to get the limit of the module. That explains to reach an equivalent of JEDEC level 2. Following the Table 5, all the modules are passed the different conditions. The electrical tests are correct, it notices some drifts of resistance measurements but acceptable. It don't observe any kind of failure (see Figure 20) on the modules excepted on the GTV3. After a storage @85°C/60%RH during 168 hours followed by three reflows, a delamination is located on the corner of the level 1 (see Figure 21). This defect is occurred on the higher stress area in term of thermal flux. Then the module is defined as a JEDEC class 3.

Table 5 - Results after Humidity Test

GTV	Equivalent JEDEC level	Structure	Status
1	3	**S1 + M1**	**Passed**
	2		**Passed**
2	4	**S2 + M1**	**Passed**
	2		**Passed**
3	3	**S2 + M3**	**Passed**
	2		**Failed - Delamination**
5	2a	**S2 + M2**	**Passed**
6	2a	**S1 + M2**	**Passed**

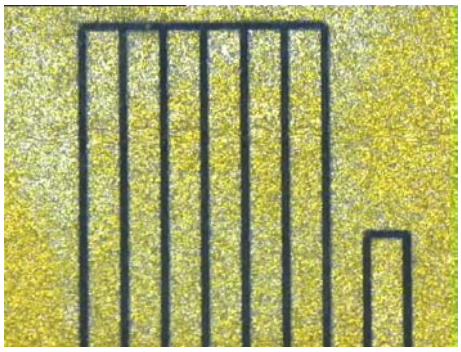


Figure 20 – Vertical Interconnection

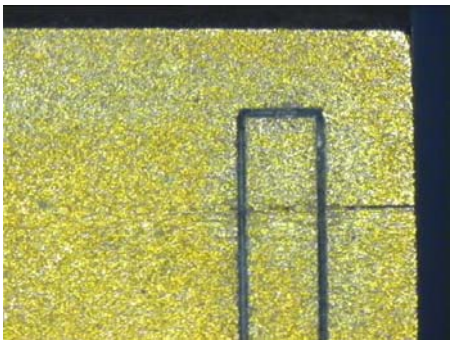


Figure 21 – Delamination on Corner (GTV3)

At the end of this set of test, some conclusions are listed:

- The S1 and S2 substrates associated with the M1 moulding compound have passed all tests after 500 thermal cycles and 85°C/85%RH 168 hours.
- The M3 moulding compound has failed the evaluation due to the delamination occurs on GTV3 and electrical measurement defects.
- The M2 moulding compound is an alternative to the M1 one
- The S2 substrate has passed excepted with the M3 moulding compound
- The S1 substrate has passed all the tests with the M1 and M2 moulding compounds

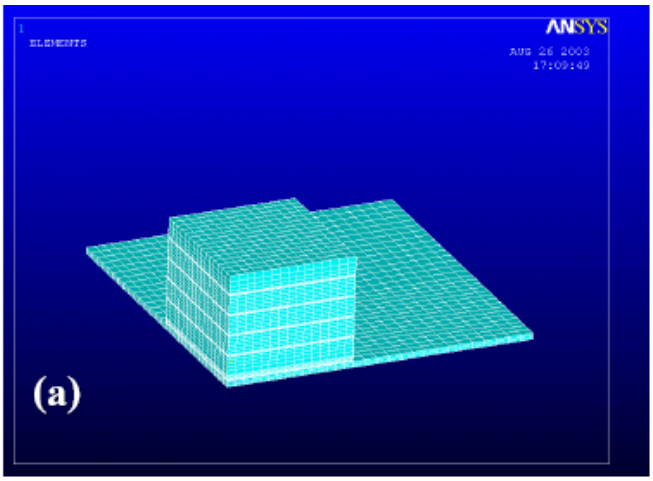
Thermal analysis by Finite Element

In order to determine isothermal cartography during reflow process of the GTV, simulations are performed using FEM ANSYS software. To optimise the model, the GTV module is simulated only with resin and PCB levels. Components and copper accurate design parts are not considered. The copper levels are considered in the modification of the thermal constants of the PCB level and components are integrated by resin levels. The values of the thermal constants of the PCB and resin are adjusted considering the experimental results (see Table 6).

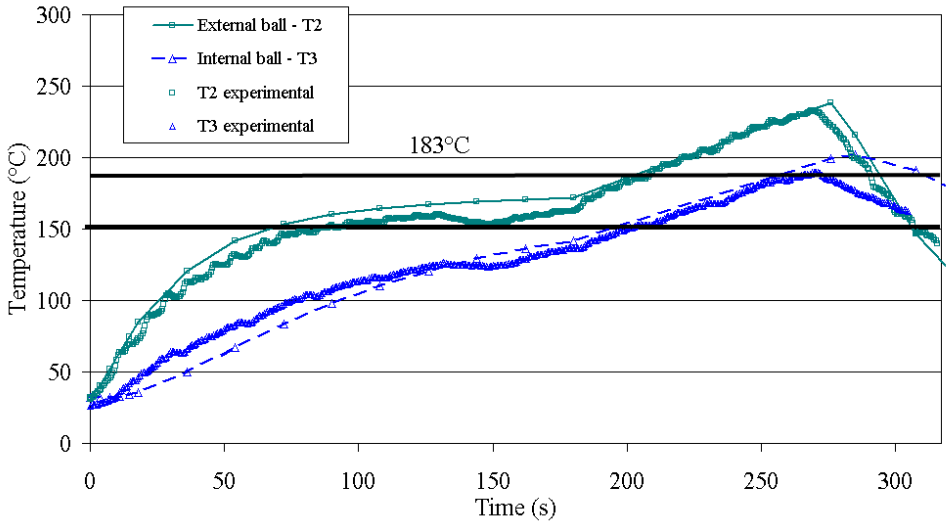
Table 6 - Thermal Material Properties

	Material	Constants for thermal simulations		
		Density (D) $kg.m^{-3}$	Heat capacity (C) $J.kg^{-1}$	Thermal conductivity (λ) $W.m^{-1}$
Material physical properties	Substrate	1200	1500	0.3
	PCB + Copper	1200	700	1
	Resin FP4450	1600	1250	0.6
	Resin + components	1700	1200	0.5
	Balls level (SnPb)	9000	10	50
	PCB motherboard	1800	500	1

Typical pattern is shown in Figure 22a and composed by 15524 nodes and 12825 quad type elements. Simulated results are given in Figure 22b considering time dependence temperatures previously defined (see Figure 22). The comparison between experimental and simulated temperatures time dependence shows well correspondence of temperature profile for internal and external ball. The simulated thermal cartography are given in Figure22a. The localisation of the efficient area for reflow of balls has been determined. The assembling process has been well modelled by Thermal ANSYS software. We can note that the difference between experimental and simulated temperature is close to 5 °C representing less than 3% of error. This difference is acceptable for temperature analyses because the accuracy of temperature measurement is generally around to 5% of error. Thanks to the thermal resistances integrated on the silicon dice; it's possible to study the heat transfer from the middle to outside on 1, 3, 5 levels only. The temperature inside is measured by a PN junction integrated on the die.



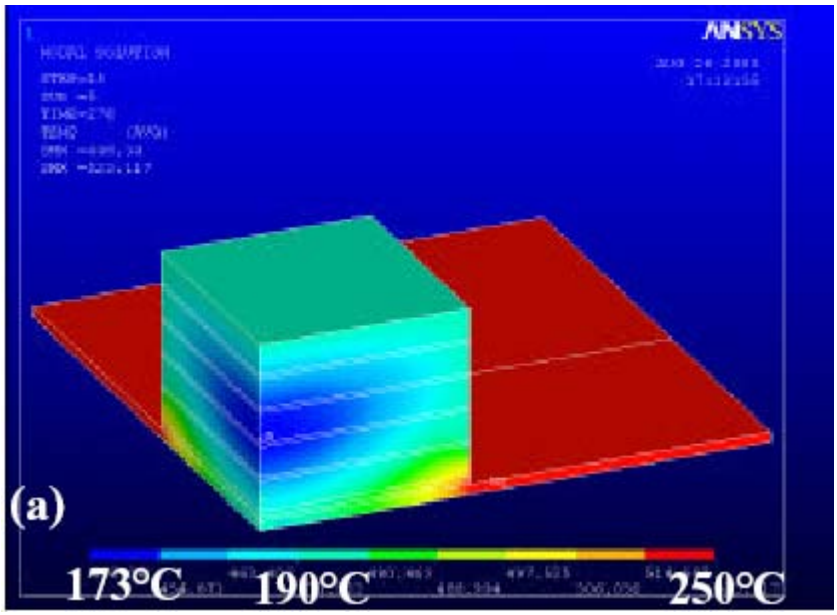
(a)



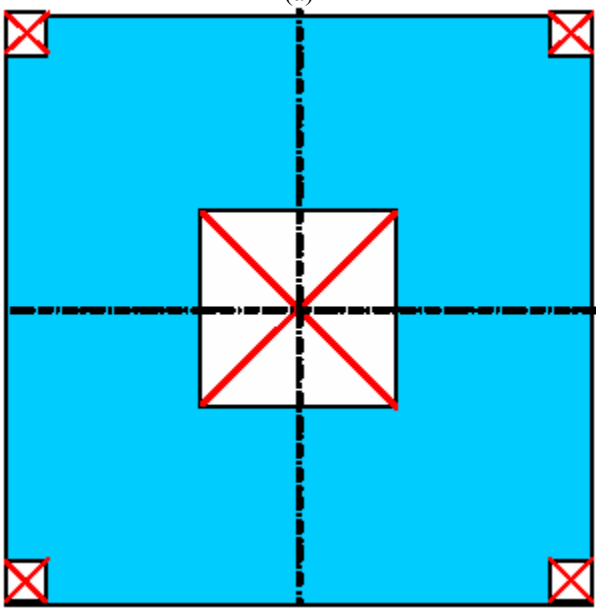
(b)

Figure 22 - Element and Geometry Model (a), Comparison between Experimental and Simulated Temperatures (b)

This analysis, validated by experimental measurements, allows to define the efficient area for balls reflow define by balls temperature upper than 190°C. This efficient area is presented on Figure 23 by bottom view and is equal to 7/9 of the total area of the GTV module.



(a)



(b)

Figure 23 - Isothermal Cartography (a) and Efficient Area for Balls Reflow (b)

The thermal management is pertinent in such module because it needs to have a sufficient heat transfer from the oven to solder balls and also to dissipate the heat ingress the module during the reflow. In fact a diode effect it requires between the bottom level and the other ones. The isothermal cartography is established but the balls level is represented by a parallelepiped solid and it is impossible to established stresses and strains cartographies. These are useful to evaluate the reliability of the balls during ageing tests or life tests. The limit ANSYS software modelling cannot allow to build a complete model with: GTV module, balls and PCB motherboard. Nevertheless, IXL Laboratory has created a new methodology allowing to modelled complete systems. This methodology is based on the specific function of ANSYS software: sub-structuring.

End-user Wireless application

There is a growing interest in wireless communication in automotive applications, based presently on different protocols. In fact, Siemens AT has fully developed and put into production on the Megane Scenic Renault a wireless unit for the measurement of the tyre pressure and transmission to the body computer. Nokian Tyres and VTT, among other partners, have developed an intelligent unit based on Bluetooth® technology for the measurement of pressure and temperature inside the tyre, monitoring also road surface changes. Commercial applications are targeted for high speed category tyres for vans and high-end passenger cars. During the next years, we will face standardization of wireless protocol / technology in the automotive sector, aimed at the system cost reduction. Finally a piezo-electric system has been used for the measurement of engine oil level/quantity in luxurious car: this unit is fully integrated inside the engine oil chamber and the communication toward the engine ECU is realized through radio-frequency local conversion. The automotive application will deal with the design and development of an autonomous general purpose module for wireless communication based on Bluetooth® technology. It will be integrated into a three-dimensional structure that will include:

- the micro-controller for the interface towards the field,
- the Bluetooth® transceiver and the related RF circuitry,
- the planar antenna and passive components.

It will also exhibit ruggedness and reliability typically required for automotive applications. This module will be used in vehicle electronic units in order to replace functions presently implemented by means of physical connections. Power supply functionality will be also investigated, in order to realize a true self-standing unit. This will be accomplished by means of an autonomous energy storage unit, such as battery, radio frequency or kinetic energy concept. These approaches have already been used in the automotive for stand-alone sensors (tyre pressure, oil level / quantity monitoring). The challenge is to integrate inside a single device a complete class 1 transmission up to 100 m) and 2 (transmission up to 10 m) BlueTooth® system with on-board software in order to avoid managing the uppers layers above the HCI and communicate by the most common interfaces (see Figure 24), quicker and more simple than HCI (200 Kbit/s). The functions included in the BlueTooth® demonstrator are:

- Microcontroller: it is the intelligent device able to manage the user interface; it processes the information provided by the external communication lines and then generates the proper set of HCI-commands;
- Memory: in order both to store the temporary data and to provide data buffer, a static random access memory (SRAM) is needed; a fast access time is required for maximum data transfer; logic gates are present for interfacing with microcontroller;
- Bluetooth baseband controller: the wireless system core is the baseband controller, which is the device that manages the set of commands in the first protocol layer (HCI) and then works directly with the RF transceiver;
- Radiofrequency transceiver: it is the digital-analog interface between the baseband controller and the RF section;
- Power amplifier: a RF power control circuitry is needed in order to implement a BlueTooth class 1;
- Radiofrequency switch: a RF high-speed switch is needed for the selection of transmitting or receiving mode; moreover it realizes the proper connection between embedded antenna or connector for external antenna and the circuitry.

Identification of the available and suitable components for implementing the functions required have been performed following the items:

- commercial availability;
- operating temperature range (industrial –30/+85°C);
- size (the overall area will be smaller than 35×35mm).

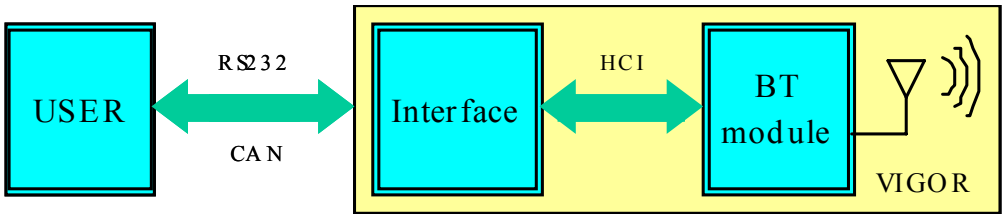


Figure 24 - Bluetooth Communication for BT Module

End-user Optoelectronic application

Optics and opto-electronics are already used in products in many market sectors and will be increasingly used at module and board level. In particular, the use of opto-electronic components, modules and sub-systems is anticipated in a growing number of avionics and space applications, such as sensors (e.g. for flight control, fuel metering, safety and security aspects) and passenger services (entertainment, onboard sales, etc.), as well as in automotive, computers, communications and portable equipment. The reasons include high speed / bandwidth, immunity from interference and noise (EMC/EMI/security /

safety) and, of course, to handle signals which originate in optical form, e.g. from sensors and in instruments. The optoelectronic application will realise a functioning 3D Module which incorporates opto-electronic components (photo-detectors and a VCSEL) and their associated electronics (see Figure 25). Multiple optical inputs at different wavelengths are fed into an optical waveguide splitter and separated by wavelength-division de-multiplexing. A single fibre carries the input signals and an output control signal in a bi-directional optical connection to the other parts of the system. The electronics in the 3D stack include a processor, memory and interface circuitry.

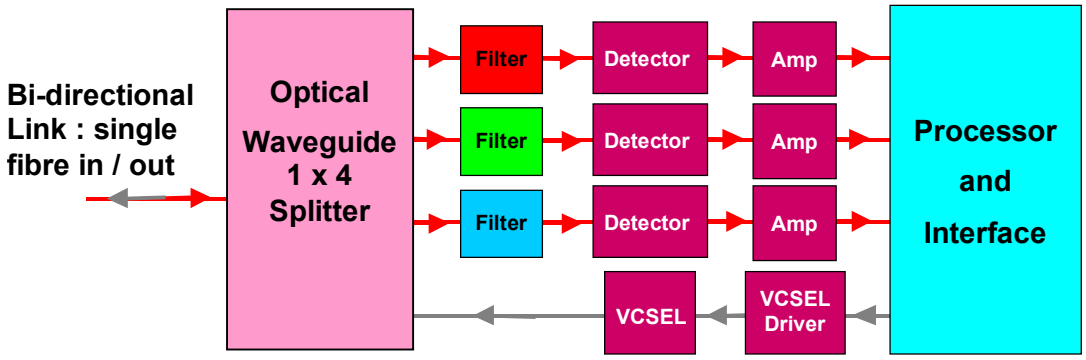


Figure 25 - Optoelectronic Connection and Signal Processing in a Module

The optoelectronics are on the top of the stack. Because of the temperature sensitivity of opto-electronic components, an interposer is used to attach the 3D module to its motherboard, rather than solder. The interposer has a contact array on the same pitch as the GTV (1.27 mm) and has the added advantage that the units can be readily removed and replaced.

Conclusions and Future Works

Besides the mobile phone sector, automotive and aerospace applications demand an important miniaturization of the systems. This project allows associating in 3-D very heterogeneous components, since they go from high-frequency components to opto-electronics components. The analysis of each cost carried out with a EMS world-wide leader allows targeting these volume markets. The reduction in weight and volume of the 3-D modules for these applications is at least 10 times. As a matter of fact, cost being a priority objective, the rule is to use component on the shelf (COTS) only. Almost all these components are packaged (plastic package, TSOP, CSP, etc). Some 3-D approaches exist, as presented in the beginning, called Chip On chip, which are not very much useable for SIP of such complexity (active, passive, opto-electronics, high-frequency components). The versatility of the 3D technology associated to its robustness, makes this approach the most cost-effective in term of dimension/cost compromise. The target of this project is to validate the capability of this 3-D interconnection technique to be industrialized for volume market. At the mid-term of the project, some cost savings have been reached and some of the technical improvements qualified.

The high reliability of the M1 moulding compound has been validated with the two substrates: S1 (aramid fibre/epoxy) and S2 (glass fibre / BT Epoxy / Anti CAF). These associations have permitted to get the equivalent JEDEC level 2. The M2 moulding compound can be considered as a reliable alternative of M1 one. Moreover, it's compliant with the VGOR objectives in term of cost savings. The M3 moulding compound has failed the tests thermal cycles and humidity; some delaminations are occurred after humidity test and missing electrical connections. Some of materials associations have reached the qualification level without defect and then they continue up to the failures. After 500 thermal cycles, few modules have been submitted to the humidity tests. This last test allows determining an equivalent of JEDEC level. The current status is a JEDEC level 2a. This result is important to settle a full compliance with the assembly lead time. These tests have demonstrated the reliability of this 3-D packaging and interconnection process.

Following the manufacturing of the generic test vehicles, some problems have been encountered on the adhesion of the solder pad to the connection substrate (level 5) after balling operation. The balling process has been identified as the origin of the adhesion missing. Some assumptions are proposed: weak adhesion of copper pad on dielectric raw material, plating (nickel/gold and tin/lead), pad design D1 (via in pad, microvia and dogbone), and pad design D2 (Solder mask define and copper pad define); All these parameters are integrated in a matrix for experimentation (DOE).

The first set of test vehicles have allowed to highlight the criticality of the thermal management inside the large module. The overall dimension are the largest for such module (35x35 mm square) but some thermal issues are checked and then it leads to a better understanding of the heat transfer during the reflow step and the life of the module. Some solutions are study thanks to the FEM support. By consequently the second set of vehicles will be focused on thermal management; it is named Thermal Test Vehicle (TTV). The Physical Vapour Deposition (PVD) process for module metallization is settled with the chromium-copper-chromium sequence instead of nickel-gold with current plating process. This new process allows to get a

better control on the parameters and to threat more than 800 modules per batch. The TTV modules will be metallized by the process. Moreover, some complementary studies lead to simplify the substrate technology; it's to think about no hole. That means using a double or four layer substrate without hole or window around the copper tracks dedicated to the vertical interconnection. This proposal is highlighted with the current leakage from consecutive copper tracks, for vertical interconnection, through the dielectric substrate.

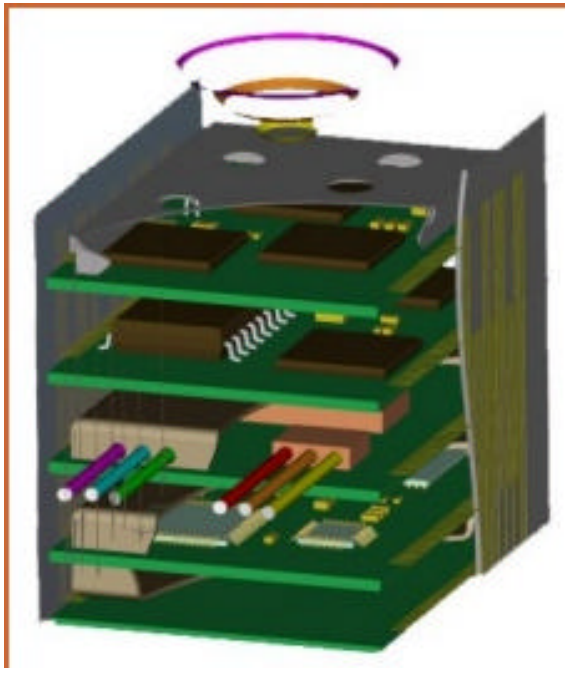
One can think that thanks to these applications and these future developments, the 3-D interconnection will definitively play a major role and that the System in Package concept has itself definitely supplanted the System on Chip.

Acknowledgements
We would like to thank the European Community for having accepted to fund this IST project

European project VIGOR

New industrial applications in 3-D interconnection

(Vertical InteGration of Optoelectronic and Radio (sub)systems)



Presented by

Dr. Val Alexandre

Design & Engineering services

Solectron France

APEX Conference - 24-26 Feb. 2004

SOLECTRON - 3D PLUS - BAE SYSTEMS - CR Fiat - IXL

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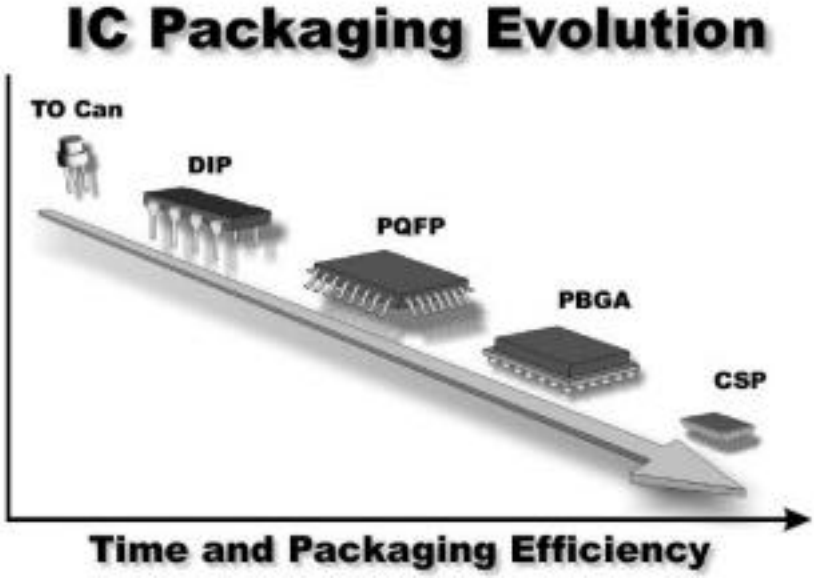
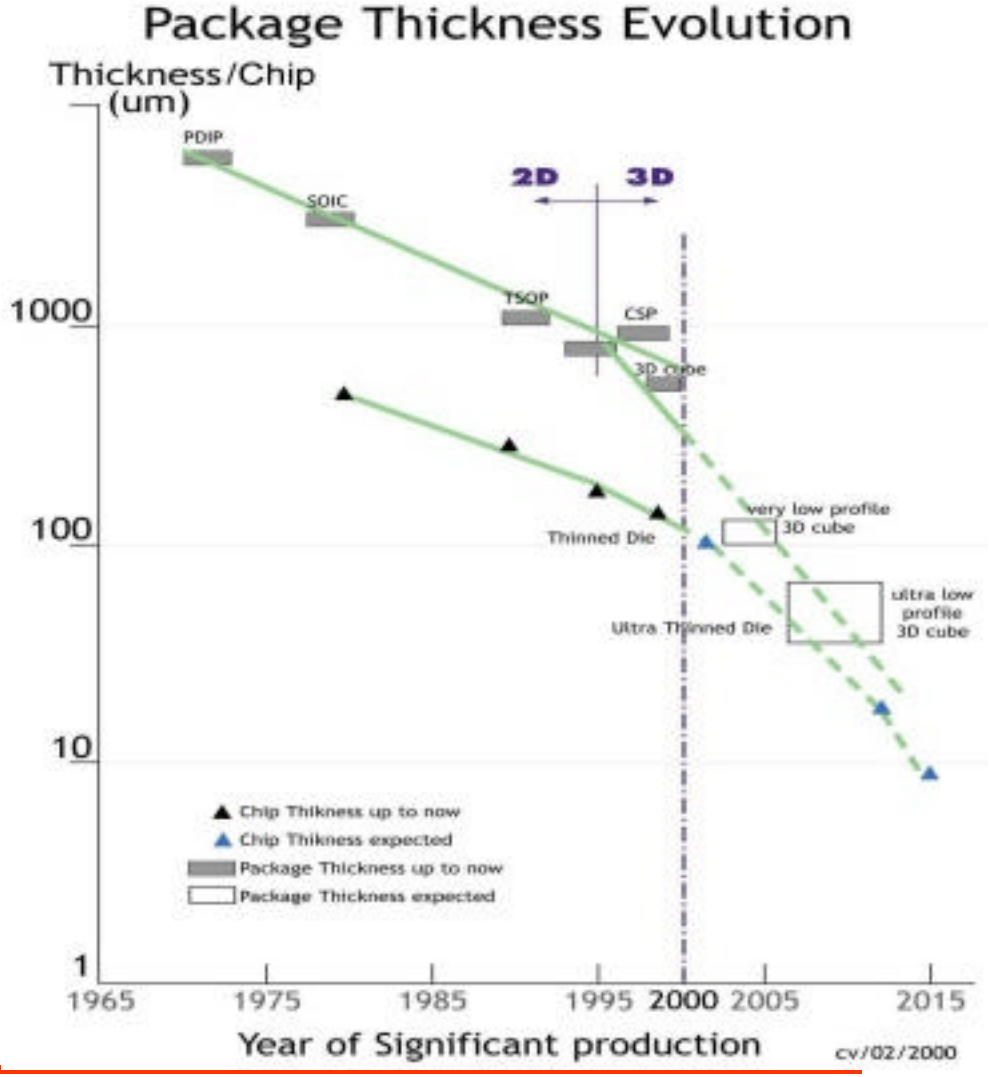
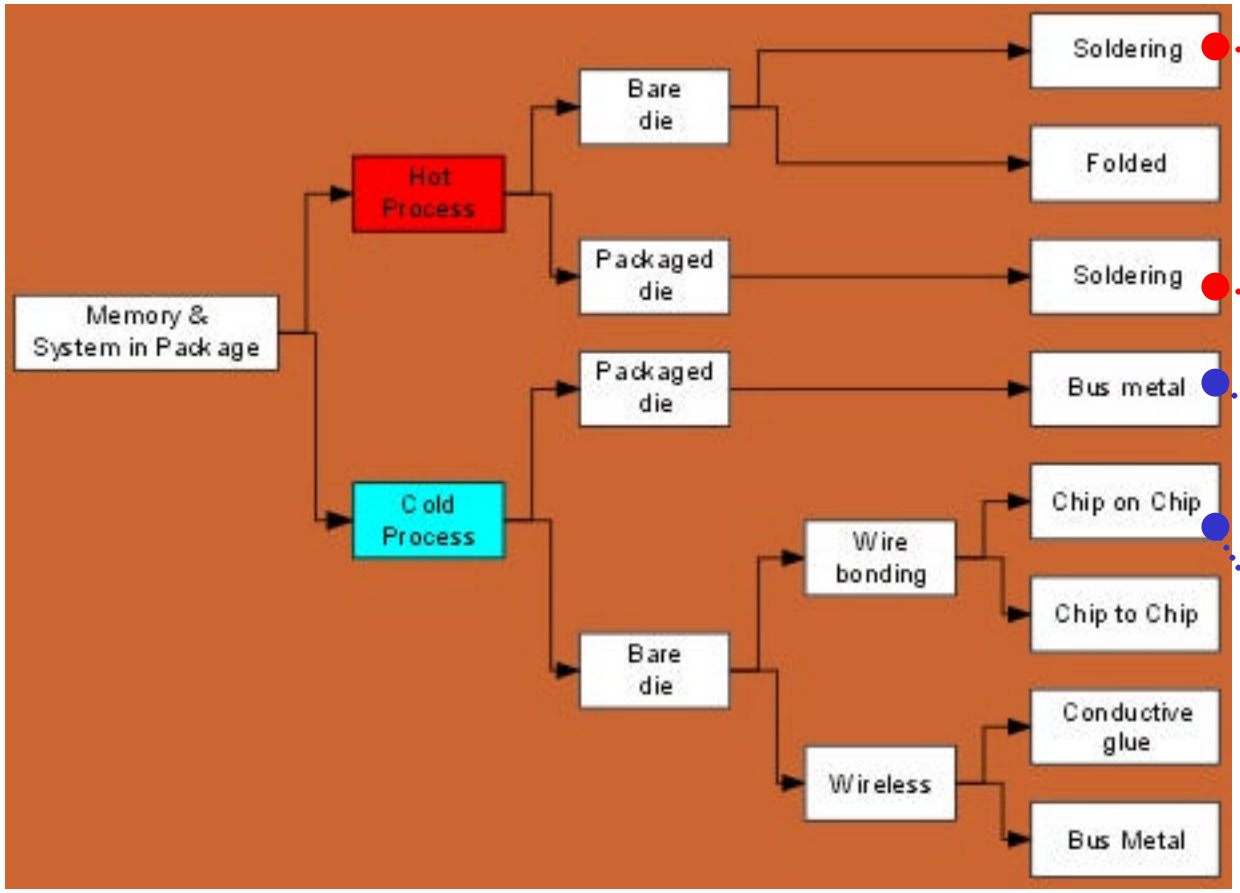
- 3-D interconnection
- Project description
- Highlights on Technical developments
- Generic test vehicles
- Qualification & Evaluation results
- Future works

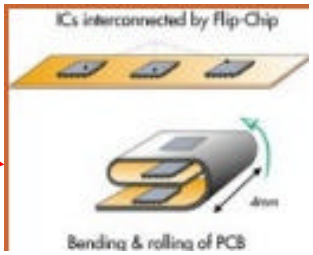
3-D interconnection



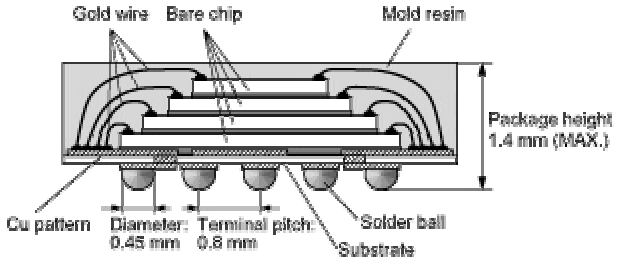


Several techniques





4-chip Stacked CSP Configuration Example



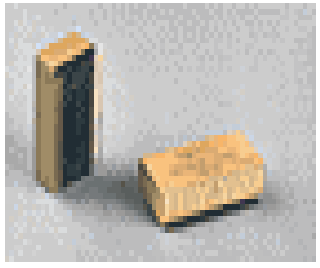
Project overview

- **Duration :** 3 Years
- **Starting date :** 4th April 2002
- **Private funding (50%) :** 1538 k Euros
- **Total Project budget :** 3076 k Euros
- **Solectron Human contribution :** 2.75 men / years
- **Partners**
  - **SOLECTRON (leader - EMS - Industrialisation) - France**
  - **3D PLUS (3-D Technology) - France**
  - **IXL (Reliability - Modelization / Simulation) - France**
  - **BAE SYSTEMS (End-user - Avionic market - Optoelectronic applications) - Great Britain**
  - **Centro Ricerche Fiat (End-user - Automotive market - Wireless applications) - Italy**

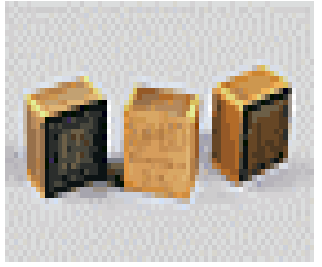
Main objectives

- To develop a 3D System In Package with versatile components
- To improve the 3D technology
- To get a cost effective module : optimisation & Industrialisation
- These improvements will be tested on Automotive (Wireless) and Avionics (Opto electronic) demonstrators

Hermetic package
(Pin Grid Array)

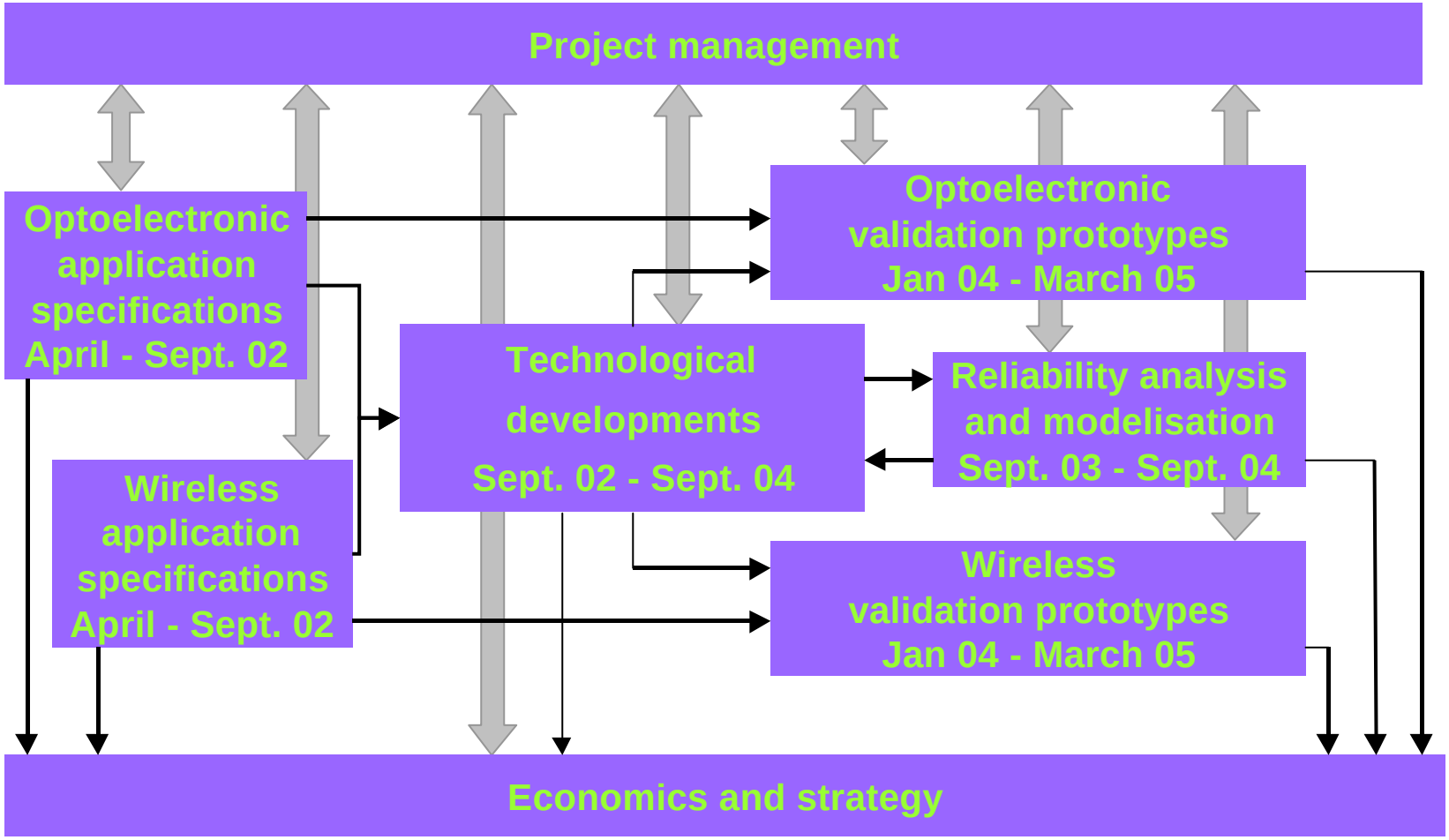


Memory package
(Gull wing leads)

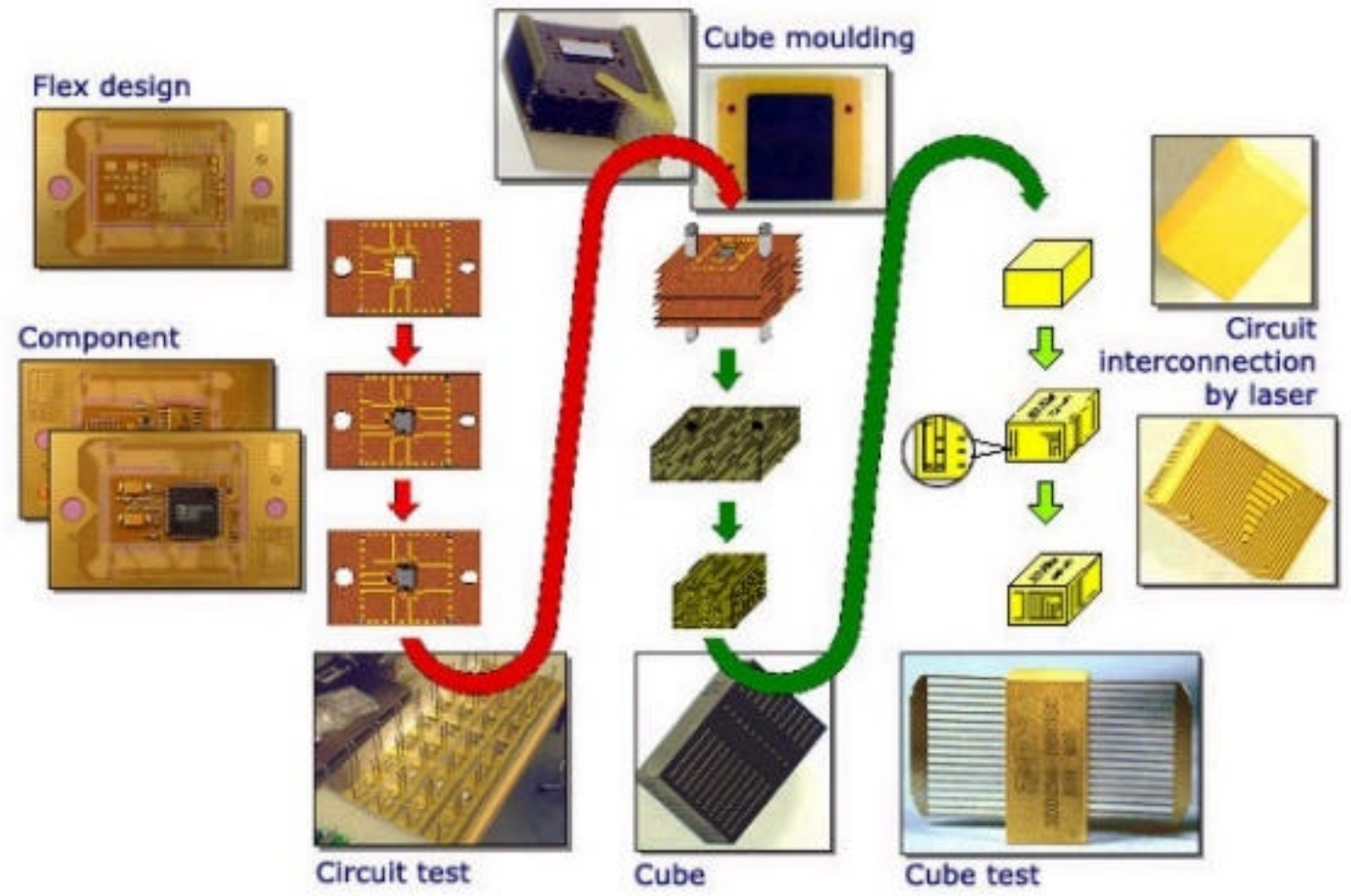


Microprocessor package
(BGA)

Work package description



3-D interconnection for VIGOR



Technical developments

- Molding compounds
  - Performances / Cost / Compliant with process
- Circuits
  - Lower cost techniques
  - Multi sources
  - Dielectric raw materials
- Stacking
  - Collective process / Yields
- Metallisation / Plating
  - Wet process : Ni / Au plating
  - Dry process : Cr / Cu / Cr metallisation (PVD)

Technical developments : molding compounds (1/2)

- Specifications
  - Low coefficient of thermal expansion (CTE)
  - High glass temperature transition (Tg)
  - Ionic purity for electronic grade
  - Mono component (low temperature storage)
  - Liquid encapsulation
  - Low viscosity for pouring
  - Cost / time savings

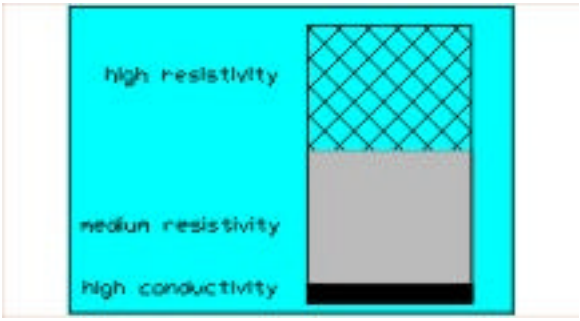
Technical developments : molding compounds (2/2)

	Material 1	Material 2	Material 3
Viscosity (mPa.s) **Method**	44 000 Brookfield 7-20 rpm	15 000 Brookfield 7-100 rpm	23 000 Brookfield 1410 rpm
Price (Euro/gr)	0,44	0,32	0,47
Curing schedule	0,5h@125°C + 1,5h@165°C	1h@175°C	0,5h@150°C
Density	1,77	1,8	1,69
Young modulus (GPa)	3	11	6
Chloride (ppm)	5	20	5
Sodium (ppm)	1	20	5
Tg	162°C	160-170°C	135°C
CTE (ppm/°C)	18	17-20	32
Thermal conductivity (W/m°K)	0,5	0,7	
Linear shrinkage (%)	0,15%	0,15%	

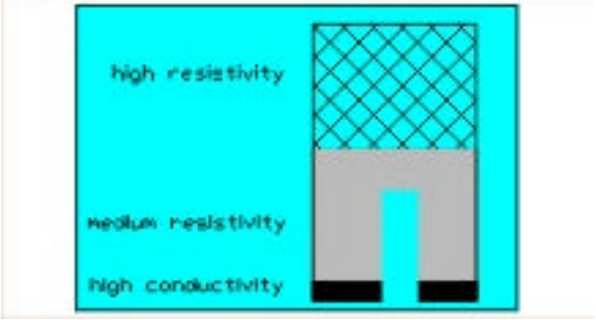
The Material 1 is the qualified molding compound.

Technical developments : circuit (1/5)

- The current PCB technique : „Flying lead“

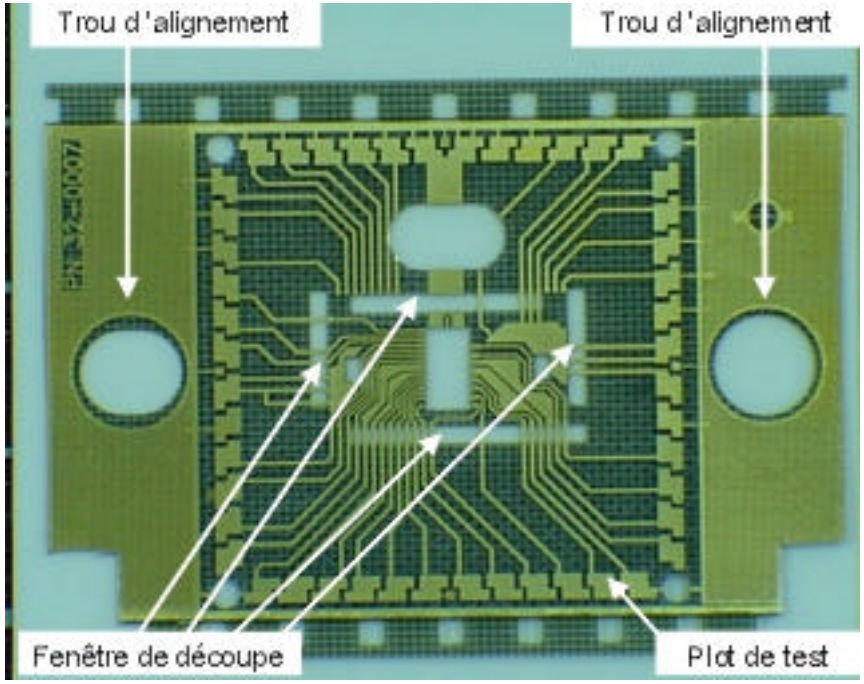


Flying lead allow a good insulation between tracks and prevent a region of medium resistivity.

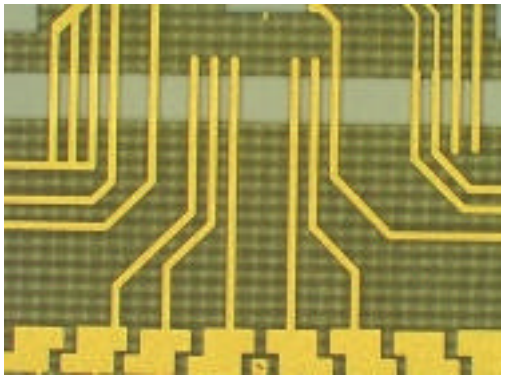


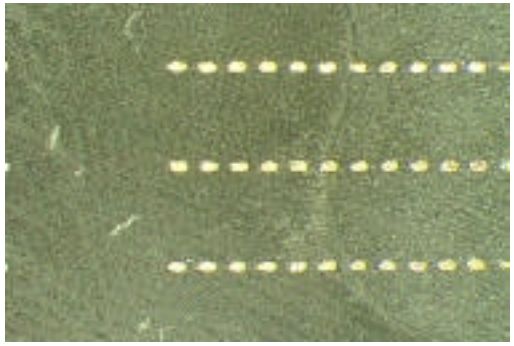
  - Advantages :
    - **Qualified CNES / ESA**
    - **Low current leakage < 1 nA**
    - **Homogeneity on each face after sawing**
    - **Large choice of high Tg materials**
    - **Laser beam focalization and etching**
  - Drawbacks (for industrialization) :
    - **Two PCB manufacturer (qualified)**
    - **High cost**

Technical developments : circuit (2/5)



„Flying Lead“ circuit



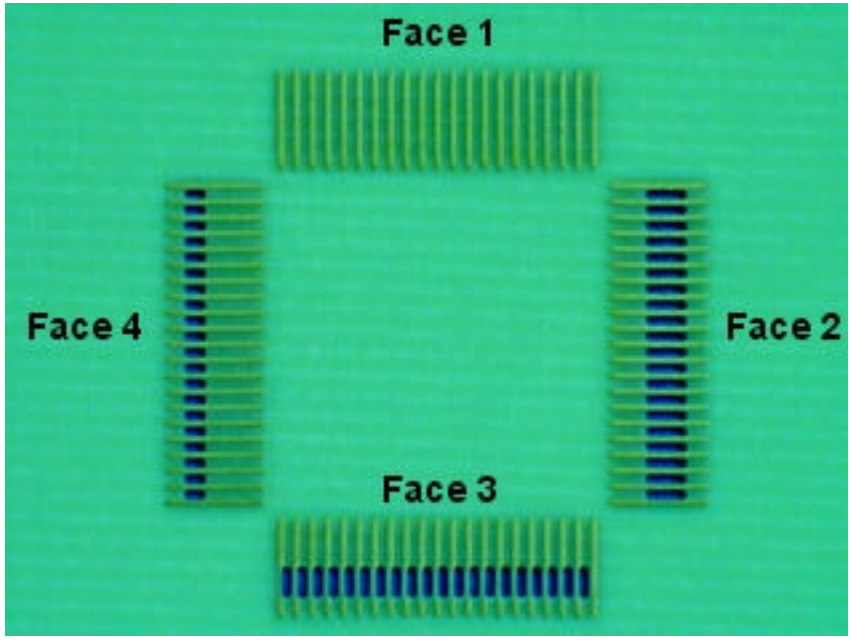


Face after sawing

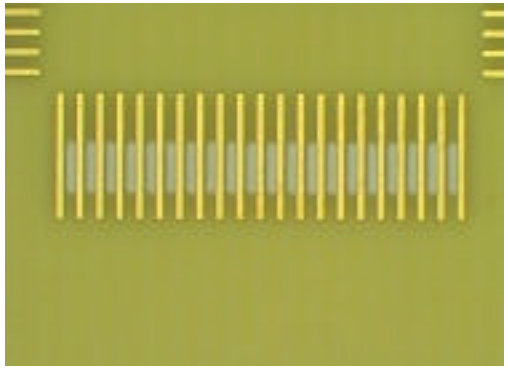
Technical developments : circuit (3/5)

- Alternative „Oblong Hole“ technique
  - Advantages :
    - **Multi sourcing**
    - **Cost reduction**
    - **Large choice of high Tg raw material**
  - To be evaluated :
    - **Current leakage**
    - **Compliant with process**
    - **Laser / Mechanical drilling**
    - **Ratio circuit thickness / hole diameter**

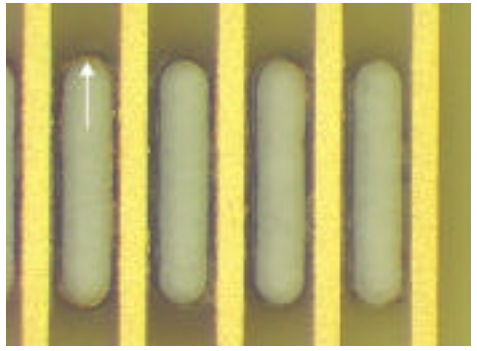
Technical developments : circuit (4/5)



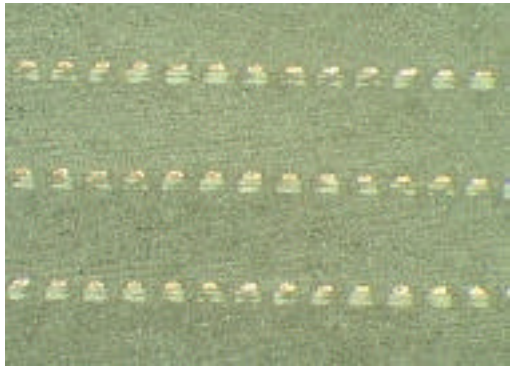
„Oblong hole“ test circuit



Mechanical drilling



Laser drilling



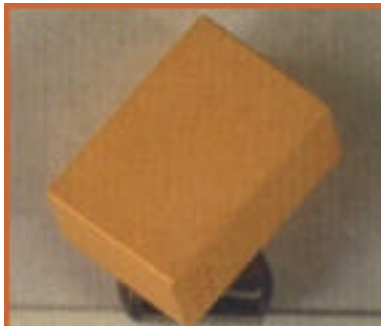
Face after sawing

Technical developments : circuit (5/5)

	Material 1	Material 2
Fiber	Aramid	Glass
Resin	Epoxy	BT/Epoxy
CTE (x,y) ppm/°C	11	12
CTE (z) ppm/°C	110	55
Tg	170°C	185°C
Dielectric constant (1 GHz)	3,9	3,8
Dissipation factor (10 GHz)	0,022	0,0014
Volume resistivity (M Ohm.cm)	$> 10^3$	10^6
Surface resistivity (M Ohm)	$> 10^3$	10^6
Water absorption (%)	0,32	< 0,05
Young modulus (G Pa)	15	30

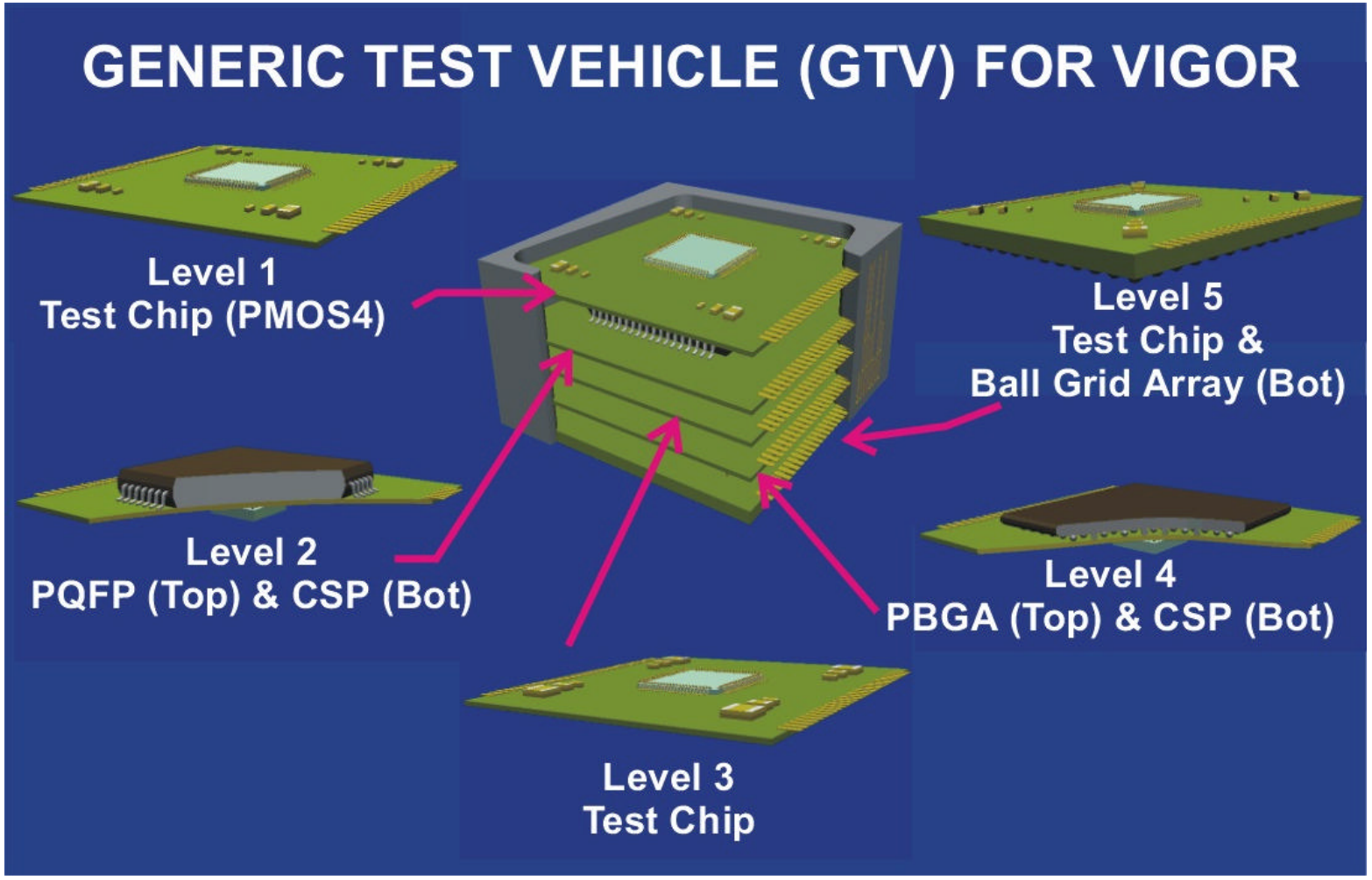
Technical developments : Plating/Metallization

- **Current technique : wet process (Plating)**
  - Technique from PCB plating
  - Chemical Nickel (2 µm)
  - Electrolytic Nickel (3-4 µm)
  - Electrolytic Gold (2 µm)
  - **Drawbacks :**
    - No compliant with in-line production



- **Alternative technique : dry process (metallization)**
  - PVD equipment with carrousel (800 to 1000 per batch)
  - Chromium and Copper sources

Generic test vehicle (1/3)



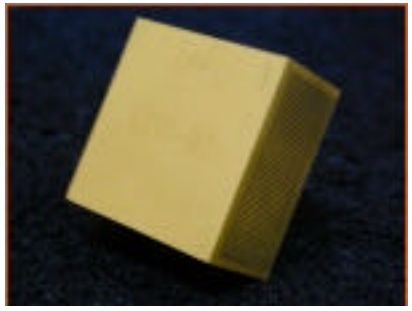
Generic test vehicle (2/3)

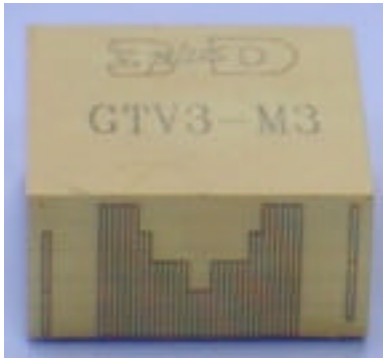
	PCB material		Molding compound		
	S1	S2	M1	M2	M3
GTV1	X		X		
GTV2		X	X		
GTV3		X			X
GTV5		X		X	
GTV6	X			X	

The plating is based on the wet process Ni/Au

Characteristics :

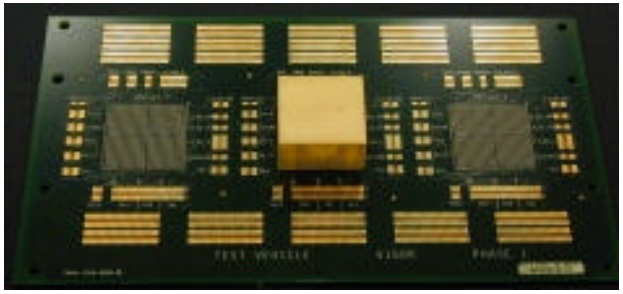
- Overall dimension : 35 x 35 mm
- Height ≈ 18 mm
- Mass ≈ 43 gr
- Hard balls = 624

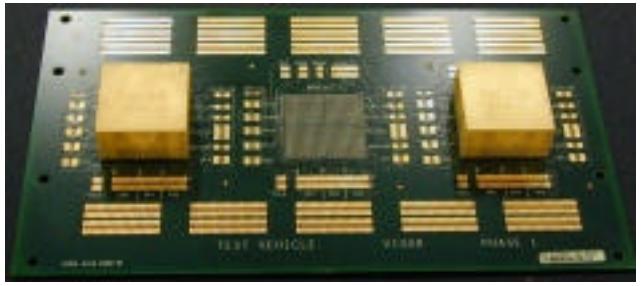




Generic test vehicle (3/3)

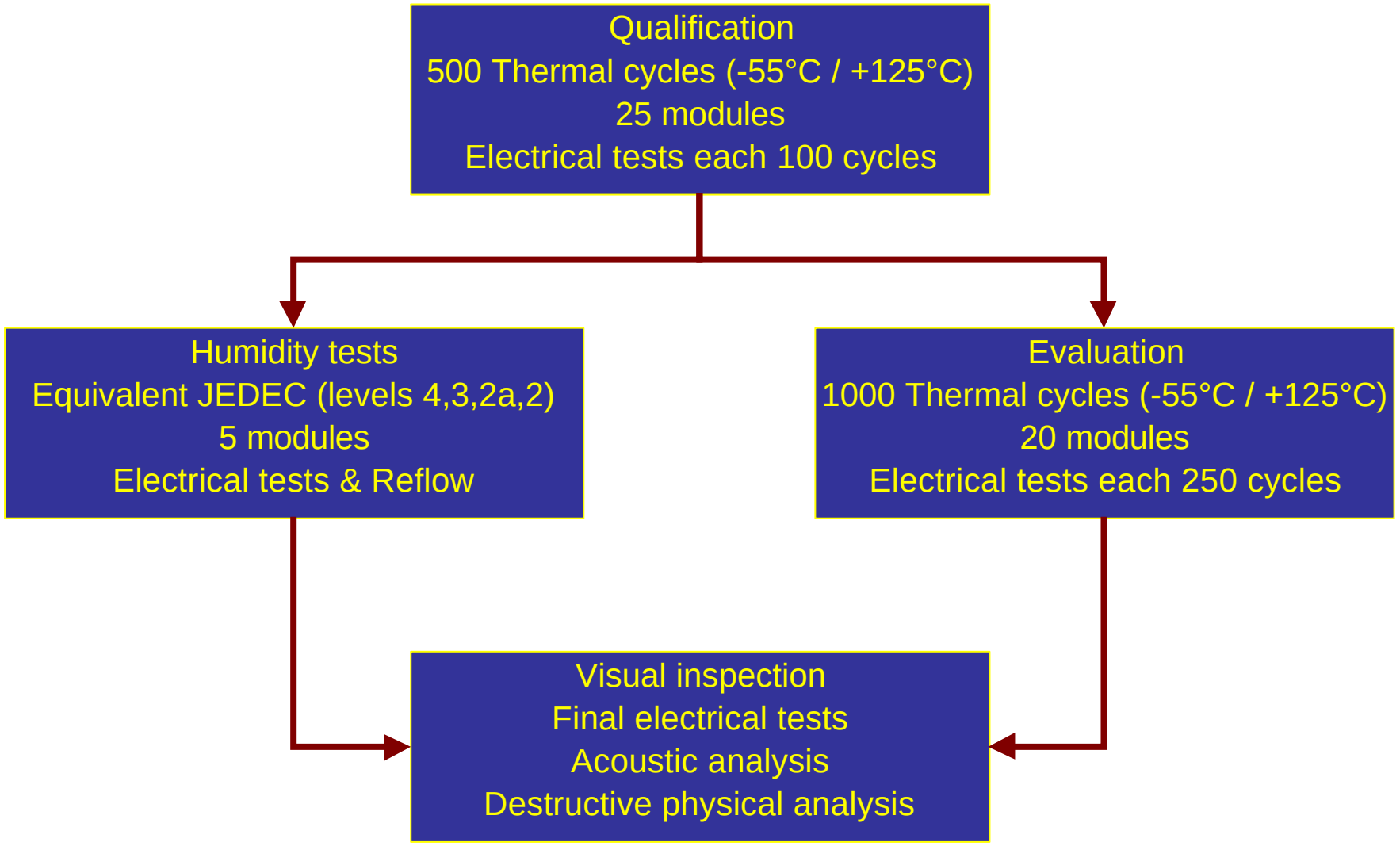
- **Assembly highlights**
  - The height is maximum for pick&place equipment
  - The reflow profile is critical
    - Temperature on motherboard up to 265°C
    - Thermal gradient between external and internal solder balls up to 43°C
    - High temperature on upper level 190°C





Motherboard (265x135x1.6 mm)

Qualification / Evaluation plan



Qualification / Evaluation results (1/3)

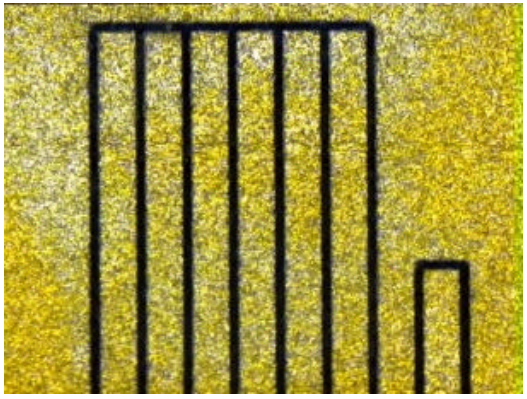
- **Qualification : 500 cycles / Evaluation : 1500 cycles**

Thermal cycles	Materials	After 500 cycles	After 1500 cycles
GTV 1	S1 + M1	**Passed**	**Passed**
GTV 2	S2 + M1	**Passed**	**Passed**
GTV 3	S2 + M3	**Failed (level 1)**	**Failed (level 1 + solder balls)**
GTV 5	S2 + M2	**Failed (solder balls)**	**Failed (solder balls)**
GTV 6	S1 + M2	**Passed**	**Passed**

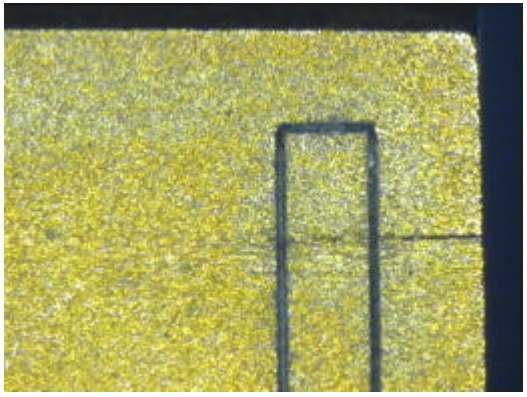
Qualification / Evaluation results (2/3)

Humidity test : equivalent of JEDEC level 3

	60°C @ 60%, RH 20 hrs Jedec level 4	60°C @ 60%, RH 40 hrs Jedec level 3	60°C @ 60%, RH 120 hrs Jedec level 2a	85°C @ 60%, RH 168 hrs Jedec level 2
GTV 1		Passed		
GTV 2	Passed			Passed
GTV 2		Passed		
GTV 3		Passed		Failed - Delamination
GTV 5			Passed	
GTV 6			Passed	



Vertical interconnection on GTV1



Delamination on GTV3

Qualification / Evaluation results (3/3)

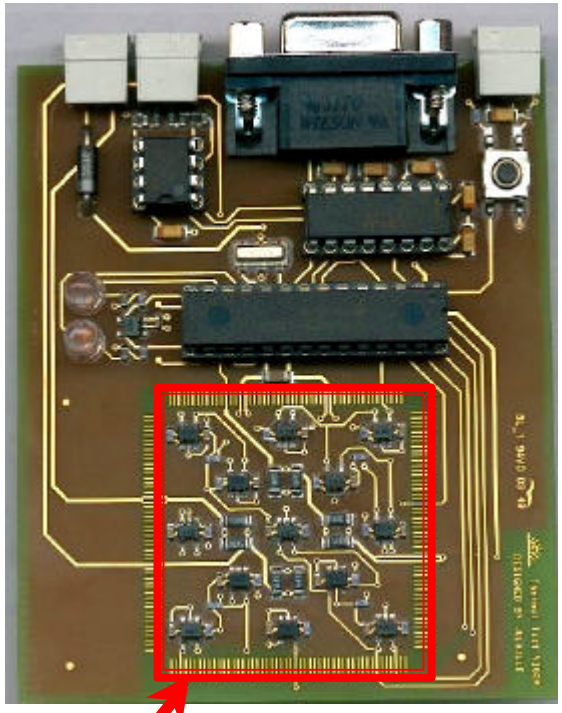
- All modules have an equivalent of JEDEC level 3
- S1 & S2 materials associated with M1 & M2 compounds pass the thermal cycles
- M3 compound has failed the tests
- M2 compound is an alternative to M1
- The solder balls have exhibited a weakness during thermal cycles

Discussions

- **The mid-term progress is highlighted by**
  - **A cost effective with « Oblong hole» technique**
  - **A curing schedule saving with M2 molding compound**
  - **Validation of new raw materials for printed circuit**
  - **An equivalent of JEDEC level 3**
  - **A thermal transfer**
    - During reflow step
    - During the life
  - **The solder ball attachement**

Future works

- **DOE on solder ball attachment included :**
  - **Design pad (µvia, dog bone,…)**
  - **Solder mask design**
  - **Plating (SnPb, NiAu, Sn, OSP)**
- **Thermal test vehicle :**
  - **Internal levels : full / partial copper layer**
  - **Interconnection level : smart copper layer partially connected to solder balls**
  - **Optimized area for solder balls**



Prototype Level : 13 Thermocouples (AD7415)
Heaters (4 W)

Thanks for your attention

- Web site : http://vigor.eu.free.fr (vigor)
- Acknowledgements to the European Community for having accepted to fund this IST project