Presented at IPC Printed Circuits Expo®
SMEMA Council APEX®
Designers Summit 04

Wafer Applied Underfill: Flip Chip Assembly and Reliability

Wayne Johnson, Qing Wang, Fei Ding & Zhenwei Hou
Auburn University
Auburn, AL

Larry Crane, Hao Tang, Gary Shi, & Renzhe Zhao
Henkel Loctite Corporation
Loctite Electronic Materials
Industry, CA

Jan Danvir, & Jing Qi
Motorola Advanced Technology Center
Schaumburg, IL

Abstract
Manufacturers of consumer electronic products are continuously striving to confer greater functionality to smaller, lighter, and less expensive packages, and flip chip is an important enabling technology for these product trends. Underfill between the die and an organic substrate is necessary to compensate for the coefficient of thermal expansion mismatch. The underfill dispense and cure step is not a typical process for an SMT factory, and demands additional capital equipment, floor space, cycle time and headcount.

An alternate approach to traditional capillary underfill is wafer applied underfill. The underfill is applied after wafer bumping and sawing, but prior to the picking of the individual die from the saw tape. This paper describes the coating and assembly processes. Liquid-to-liquid thermal cycle shock tests (-55^{o}C to +125^{o}C) have been performed on test vehicles assembled with the wafer applied underfill. First failures were over 1000 cycles. Weibull plots of the data are presented.

Introduction
Underfills that are compatible with the parts being processed have been a goal for some time, starting with the early work of Penissi et. al.[1] on underfills pre-applied to the substrate (fluxing underfills). These early materials illustrated some of the processing advantages inherent in pre-applying material prior to the attachment of the part. The shortcomings of this approach have also become apparent. Dispense and placement voids due to soldermask patterns and placement parameters are a common assembly challenge, particularly with area array die.[2,3] Filling fluxing underfill materials to high levels has also been shown to not be feasible. That is, the maximum incorporation of filler seems to be about 20% by weight, which is not sufficient to affect the CTE significantly. This limits the types of devices and applications (operating environments) that can use these materials.

Wafer Applied Processing
The materials and processes developed in this work use two compatible materials sets. The first is a filled bulk layer that provides the predominant properties of the cured underfill layer. This layer is stencil printed on to a pre-sawn wafer (still on wafer saw tape) and b-staged to yield a tack free layer. The coating process produces clean saw streets and there is consistently no bulk layer over the top the solder balls. Bulk layer over the top of the solder ball would compromise vision recognition during placement and filler particles trapped between the solder ball and the substrate pad would impede soldering, lowering assembly yield.

The second material provides the fluxing action. This material is unfilled. Two approaches are being developed in parallel. In the first approach, the fluxing material is screen or stencil printed on to the solder balls, then b-staged.[4] The flux coating can be printed either before or after the coating of the bulk layer.

Since both the bulk and fluxing layers are b-staged and tack free, heat must be applied to the die just prior to placement to soften the underfill, providing tack upon placement. Heating options have been identified for commercial, high volume pick and place systems. Figure 1 is a photograph of a heating station on a high volume pick and place system that has been demonstrated for assembly of wafer applied underfill. After die pickup, the die passes over the heating lamp in route to placement on the board. Heating of the wafer applied underfill to 60-80^{o}C is required to tack the die in place.

The second fluxing approach uses a liquid fluxing underfill that is dispensed onto the board just prior to die placement. This eliminates the need for a heating station on the pick and place system, but does require a dispense step. The combination of a pre-applied bulk layer and a fluxing underfill allows for a filled underfill system, lowering the underfill CTE. This overcomes one of the limitations of a fluxing underfill only approach.

With the bulk underfill applied, only a small portion of the solder ball protrudes (sufficient for easy vision recognition), reducing the chance of placement voids commonly observed when placing die into fluxing underfill. Furthermore, due to the controlled collapse provided by the bulk underfill, solder mask is not required. This eliminates the second source of dispense/placement voids observed with fluxing underfill assembly. Void-free assemblies are achieved using the FA-10 - 2x2 daisy chain die (10 mil pitch area array, 5mm x 5mm) as shown in Figure 2. Elimination of solder mask in the flip chip die area also eliminates one of the critical challenges in printed circuit board fabrication for flip chip assembly, increasing PCB yield and lowering cost.

The liquid fluxing underfill forms the fillet. If insufficient underfill is dispensed, incomplete underfilling and/or small fillets will result. Excess underfill dispense can result in die movement after placement. Table 1 presents the results of one underfill dispense weight (volume) study with FA-10 2x2 die (5mm x 5mm). The bulk coating layer on the dies was nominally 3.25mils thick. The results indicate good dispense process tolerance.

Figure 1 - Lamp Based Die Heating Station. (Photo Courtesy of Siemens)

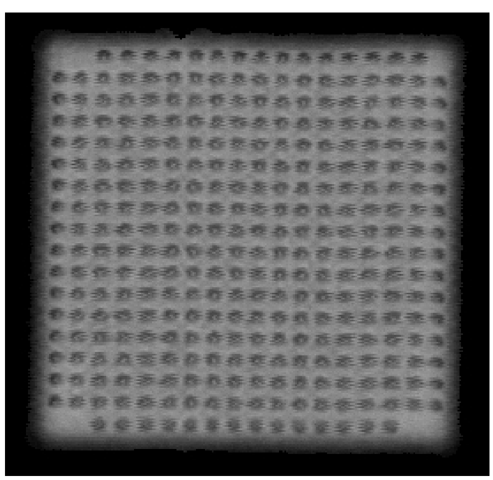


Figure 2 - C-SAM Images of FA-10 Die Assembled with Pre-applied Bulk Layer and Dispensed Liquid Fluxing Layer

Table 1 - Fluxing Layer Dispense Weight.

<3mg	3mg	3.5mg	4mg	5mg
Insufficient volume	Good	Good	Good	Die Shift

With both approaches (wafer applied flux and dispensed liquid flux), substrate baking is required. This step is necessary to remove moisture absorbed by the laminate and to also ensure the solder mask is fully cured. Absorbed moisture and solvents from under cured soldermasks will produce voids in the underfill during the reflow cycle. The wafers are shipped in metallized dry bags and if properly handled do not need dry baking. Dry baking is, however possible if required.

Figure 3 shows three reflow profiles evaluated to assemble die with the wafer applied bulk layer and the dispensed liquid flux layer. Die with 100% electrical yield have been assembled both at Motorola and Auburn using profiles A and B. If the soak time is extended as in Profile C, the underfill gels before the melting and collapse of the solder joint and the electrical yield is poor.

Figure 4 shows a cross section of the solder joints. The figure demonstrates good wetting, but the solder shape is different than typical flip chip solder joints. This is due to the absence of a solder mask. There is some wetting of the connecting trace, resulting in less solder volume in the joint. However, good stand-off is retained.

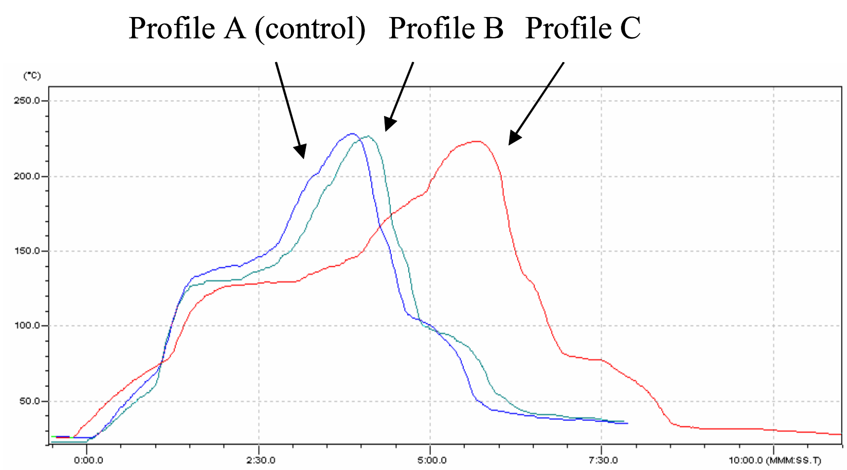


Figure 3 - Reflow Profiles Evaluated

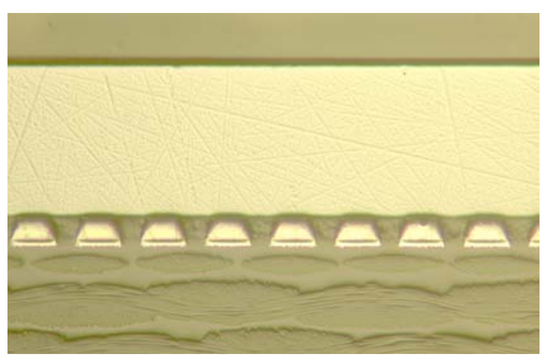
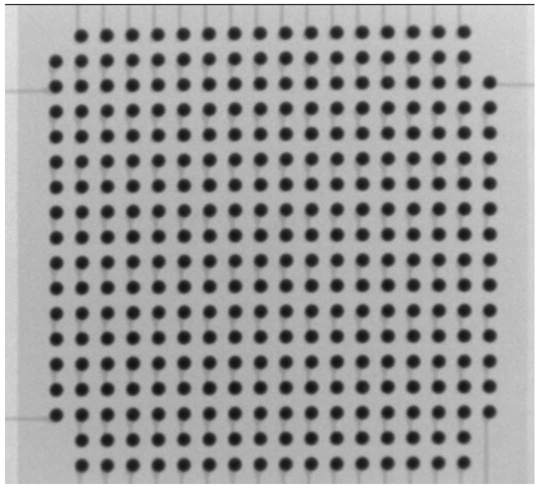
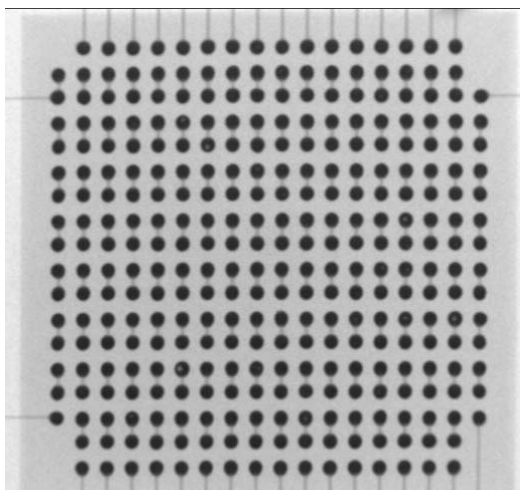


Figure 4 - Typical Cross Section of Assembled FA-10 Die with Bulk Underfill Layer and Dispensed Fluxing Layer.

Figure 5 shows self-align of the die in the presence of the bulk and liquid fluxing layer during the reflow cycle. This degree of self centering yields a robust placement process.



(a) After Placement – Die Shifted to the Right



(b) After Reflow – Die Centered on Pads

Figure 5. X-Ray Images Verifying Self-Alignment After Reflow.

The current material set requires a 30 minute post reflow cure at 165°C. Materials development is underway to eliminate this requirement.

Reliability Testing

Test boards (electroless Ni/immersion Au surface finish) assembled with FA-10, 2x2 (5mm x 5mm) test die have been subjected to liquid-to-liquid thermal shock testing (-55°C to +125°C). The hold time was 5 minutes at each temperature extreme with minimal transition time. Figure 6 shows the results from three recent thermal shock tests assembled with different fluxing material compositions (same bulk layer composition). The 1% failure point for Set 3 is approximately 1000 cycles and the slope is nearly 5, indicating end-of-life wear-out. Fluxing layer formulation work is ongoing to further improve the thermal shock reliability of the system.

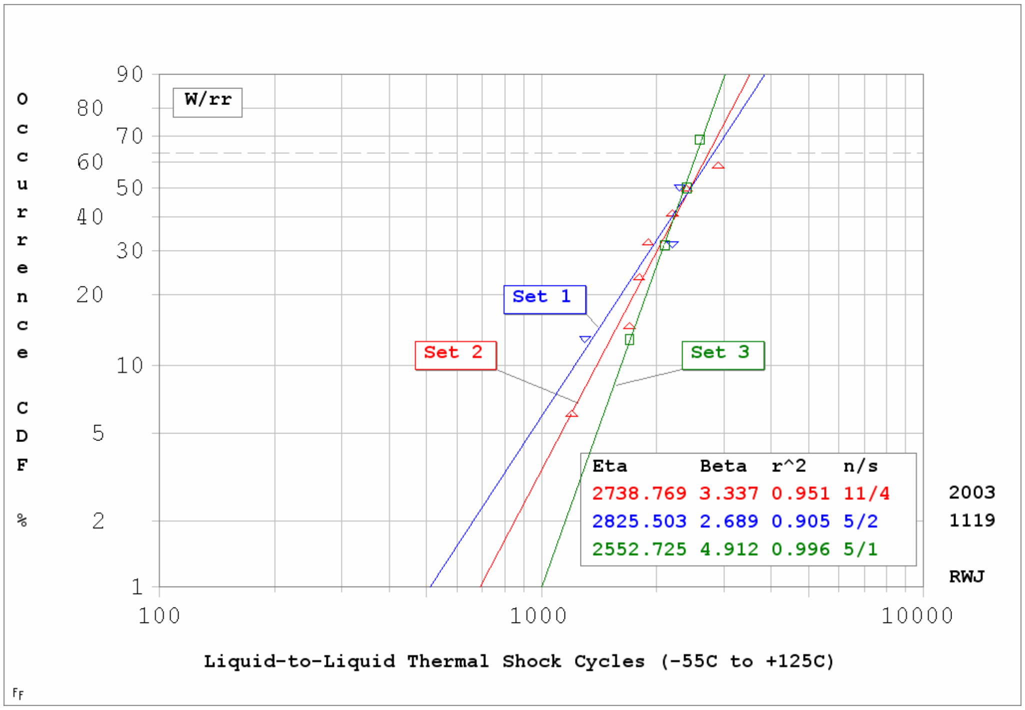


Figure 6 - Thermal Shock Results with Three Fluxing Material Compositions and a Common Bulk Underfill Layer

Failure Analysis

The samples were periodically inspected during the thermal shock test. Figure 7 shows evidence of fillet cracking that initiated after 3000 thermal shock cycles. Based on preliminary testing of earlier formulations, toughening agents were added to the fluxing material, significantly increasing the time to fillet crack initiation. Figure 8 shows a solder fatigue crack in a flip chip solder joint after thermal shock cycling. The crack is near the die, similar to failures with conventional capillary flow underfill. Figure 9 shows no delamination after 3000 thermal shock cycles.

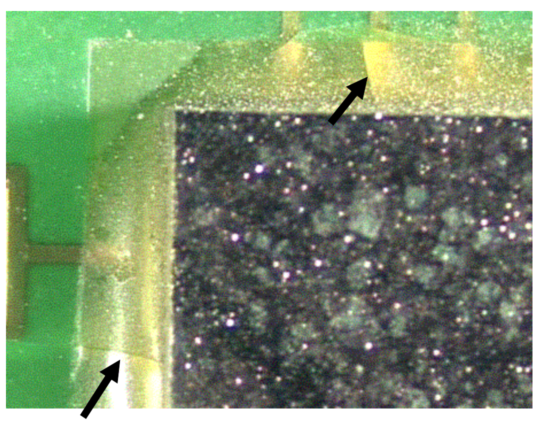


Figure 7 - Fillet Cracks Initiated after 3000 Thermal Shock Cycles

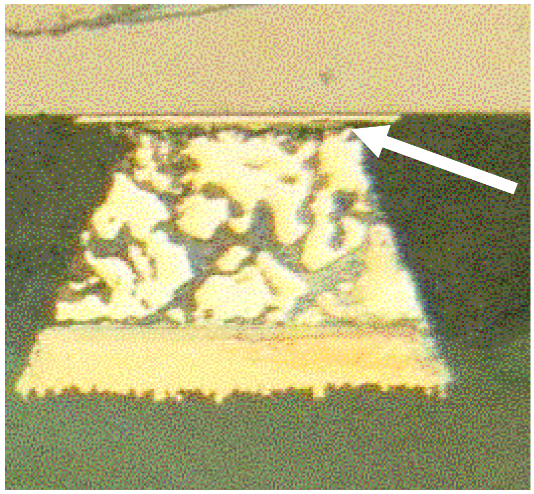


Figure 8 - Example of Solder Fatigue Crack

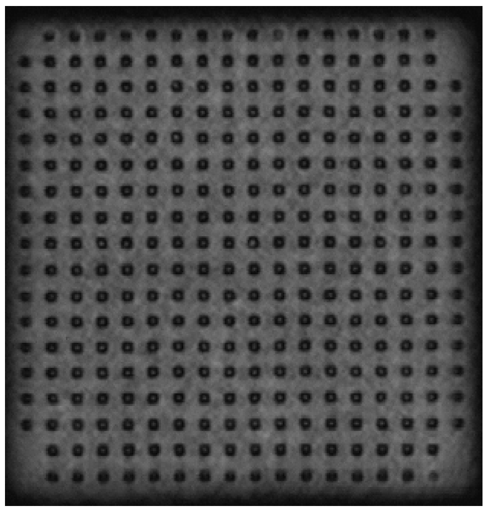


Figure 9 - C-SAM Image after 3000 Thermal Shock Cycles

Summary

Wafer applied underfill offers an opportunity to simplify the manufacturing process for flip chip-on-laminate applications. The basic processes have been demonstrated and initial thermal shock results are very encouraging, achieving 1000 cycles at 1% cumulative failures. Material formulation work is ongoing.

References

1. R. Pennisi, "Adhesive and Encapsulant Material with Fluxing Properties," U.S. Patent 5,128,746.
2. Renzhe Zhao, R. Wayne Johnson, Greg Jones, Erin Yaeger, Mark Konarski, Paul Krug and Larry Crane, "Processing of Fluxing Underfills for Flip Chip-on-Laminate Assembly," IEEE Transactions on Electronics Packaging Manufacturing, Vol. 26, No. 1, January 2003, pp. 75-83.
3. David Milner, Chetan Paydenkar, and Daniel F. Baldwin, "Effects of Substrate Design on Underfill Voiding Using the Low Cost, High Throughput Flip Chip Assembly Process and No-Flow Underfill Materials, " Proceedings of the IPC 2002 APEX Conference, January 19-24, 2002, San Diego, CA, pp. S18 – 2 – 1 to S18 – 2 – 7.
4. Wayne Johnson, Qing Wang, Fei Ding, Renzhe Zhao, Larry Crane, Mark Konarski, Erin Yaeger, Afranio Torres, Marc Chason, Jan Danvir, Nadia Yala, Jing Qi, and Prasanna Kulkanari, "Wafer Applied Underfills for Flip Chip Assembly," Proceedings of the International Conference on Advanced Packaging and Systems, Reno, NV, March 10-13, 2002, pp. 195-205.

Acknowledgement:

NIST-ATP funding Cooperative Agreement #70NANB8H007.

The authors wish to thank Dr. Michael Schen, program manager, Electronics and Photonics Technology Office, Advanced Technology Program, NIST for his technical contributions and guidance.