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Flip Chip Connections Using Bumps, Wells, and Imprinting

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Abstract
A conceptual framework for a new type of flip chip attachment is proposed. Gold stud bumps are provided on the chips, and wells filled with solder paste are provided on a flexible substrate serving as the system board. Pushing the stud bumps into the wells provides a bump/well connection, and heat is applied to melt the solder and make a permanent connection. An area array of bump/well connections can have a pitch of 100µ or less. The connections are projected to be mechanically robust, to support operating frequencies of 10GHz and above, and to support replacement of defective chips as many times as necessary. Imprinting provides a fabrication method having sufficient precision to shrink the trace and dielectric feature sizes by a factor of around 20 compared with conventional FR-4 boards, while still maintaining 50Ω traces. The same precision is used to eliminate redistribution layers that are normally required between the fine pad pitch of IC chips and the coarser pad pitch of a conventional board. By also using imprinting to fabricate the wells, a low assembly cost is achievable, potentially below 0.06 cents per lead. This compares with an industry cost as high as 2.5 cents per lead for performance flip chip PBGA[1]. The most advanced materials can be used including copper conductors and Cytop[2] as the dielectric. At 10 GHz, Cytop has a dielectric constant of 2.1 and a dissipation factor of 0.0007. The proposed manufacturing methods and assembly techniques can be applied to a broad range of microelectronic systems including high performance circuit boards, high density cables with controlled impedance, integrated passives, and stacked die packages.

Introduction
Although flip chip connections are widely recognized as technically superior to wire bonded connections, direct chip attachment represented only around 10% of IC packaging, assembly and test revenues in 2002[3] (includes CSP+FC/waferCSP). Reference 1 shows that the flip chip package category also accounted for around 10% of 95 billion IC shipments in 2002 (includes COB). This low penetration of flip chip methods is primarily because of difficulties obtaining known good die, problems with testing the finished assembly, problems with replacing defective chips (rework), and high cost per lead. This paper points to manufacturing methods that can potentially surmount the cost, testing, and rework hurdles, while maintaining the highest electrical performance and dramatically improving the thermal performance of the assemblies.

Executive Summary
1. New materials and manufacturing techniques are proposed for fabricating 10 GHz circuits on copper substrates. A new flip chip connection comprising a bump and a well is included; it has the advantages of low cost, ability to perform rework of defective chips, and excellent electrical performance. The mechanical bond is strong enough that an epoxy under-layer is not required, contributing to a convenient and effective rework capability, even for a pad pitch of 100µ or less.
2. Imprinting methods have not previously allowed multi-layer stacks with precise alignment (±2µ) between all of the layer pairs. This is because standard laminators rely on mechanical pinning for alignment, and the expansion/contraction of FR-4 materials has resulted in much coarser alignment tolerances. However, such alignment precision is available with current wafer aligners, and this capability can be integrated with the imprinting method to achieve the desired alignment accuracy.[4]
3. For improved thermal and electrical performance the proposed interconnection circuits are fabricated on copper substrates. The substrate form factor can be like a silicon wafer or a large flat panel.
4. To imprint multi-layer circuits using the best available materials, new methods are required for selectively heating the layers in the stack. It is proposed that by integrating a power resistor and temperature sensors with the embossing tool, this capability can be realized.
5. The basic process for hot embossing is described.
6. A method is described for electroplating and polishing to achieve a dual-damascene process for patterning 2µ thick copper with a minimum feature size of 2µ.
7. A variation on the imprinting technique is described for building a special assembly layer atop the interconnection circuit. This layer includes wells that can be filled with solder to accept gold stud bumps, to implement the proposed flip chip connection structure.
8. Two techniques are described for imprinting multi-layer structures using the best available materials.
9. The preferred type of bump for the proposed assembly structure is a gold stud bump. Proven equipment can produce the bumps with a pitch of 100µ or less, and a cost per bump of around 0.04 cents currently.

10. The bump/well connection provides high-performance flip chip capability including a tight pitch, a strong mechanical bond, excellent electrical performance, and re-workability. The cost per lead is estimated at 0.06 cents currently, much lower than other flip chip methods.
11. The precision of imprinting and CMP can produce controlled impedance circuits having dimensions about 20 times smaller than conventional FR-4 circuits. The methods appear to be compatible with the most advanced dielectric materials for high frequency operation.
12. To date, complex flip chip assemblies have not been testable at high frequency due to the physical problem of connecting the assembly to the tester. This has limited cost-effective assemblies to approximately 10 chips or fewer. By integrating a test chip using the proposed techniques, assemblies comprising hundreds of chips may be practical and cost-effective.
13. Circuits may be partitioned into digital, analog, and RF groupings for convenience and electrical isolation.
14. The copper substrate may be folded into a serpentine structure for improved thermal performance plus electrical isolation between component groups.

New materials and New Manufacturing Techniques for Fabricating High Density Interconnect (HDI) Circuits

A dual damascene process is proposed. Imprinting[5] provides an opportunity to fabricate fine copper features in a multi-layer circuit using high performance dielectric materials like Cytop. Table 1 compares important properties for three leading dielectric materials: benzocyclobutene (BCB[6]), liquid crystal polymer (LCP[7]), and Cytop.

Table 1 – Comparison of Important Properties for Three Leading Dielectric Materials

Property	BCB	LCP	Cytop
CTE (ppm/ºC)	52	17	74
Melting Point (ºC)	N/A	280	N/A
Relative dielectric constant	2.65	2.9	2.1
Dissipation factor	0.0008	0.002	0.0007
Moisture uptake (% by weight)	0.14	0.04	<0.01

Also a novel epoxy-based composite[8] can potentially be used for capacitors and between power planes, producing a capacitance density greater than 1000 pF/mm^2. This material can be spin-cast and cured using procedures similar to those developed for other polymers. Copper traces with line width and space as small as 2μ have been reported using electro-formed nickel embossing foils.[9] Also, the walls of the imprinted copper features can be dense and smooth if high-quality electroplating methods are employed. Chemical mechanical polishing (CMP) provides a well-proven method for creating planar surfaces at each copper level, and also for maintaining good thickness control of the interlayer dielectric. A typical requirement on the tolerance of a controlled impedance trace is 50Ω ± 10%. The combined precision of imprinting and CMP allow the characteristic impedance to be achieved and controlled within acceptable tolerances while using thin dielectric layers. This leads to short vias with low inductance, capacitance and resistance, and smaller inductive loops than have been achievable with conventional methods and materials. Dr. Eric Bogatin[10] has highlighted the importance of smaller inductive loops. It is projected that the precision of imprinting will enable trace widths of 6μ and internal vias with 6μ diameter. This combination of small copper features and thin dielectrics can lead to high frequency operation. Although the frequency performance has not yet been characterized, it is projected that the circuits will operate well at 10GHz, particularly for packages and small boards where the maximum trace length is limited.

A special assembly layer is fabricated on top of the HDI circuit, to create wells at each input/output (I/O) pad location. Solder paste is deposited in the wells using a squeegee, forming compliant receptors for stud bumped devices, as will be further described. The preferred solder paste is indium-based, such as Indalloy 290,[11] containing 97% indium and 3% silver. This lead-free solder has a melting point of 143°C, lower than that of solders currently used in production, and this leads to a reduction in thermal stress induced during assembly and rework.

Imprinting is a new manufacturing process for printed circuit boards, although compact disks have been made this way for many years. Dr. Bogatin reported in 2001[12] that CDs have 1μ features, and almost 1 billion square feet per year are produced at a cost of pennies per square foot. The equipment required for embossing is simpler than for a thin film semiconductor facility, which might otherwise be used to create similarly precise circuit structures. The photo-tool (mask or reticle) is replaced with an embossing tool (stamp). The complex photolithographic exposure system is replaced with simpler equipment including aligner/laminator, electroplating system, and polisher. Both equipment sets require thin film coaters and etchers. New methods are proposed in this paper for overcoming the problem of using hot-embossing to build multi-layered circuits using the same or similar dielectric materials, all softening at approximately the same temperature. An additional difficulty has arisen from the unpredictability of separating the imprinting tool (stamp) from the dielectric material being patterned. Although the side walls of the imprinting tool are created with a positive taper and mold release agents are used, the tool and the circuit may need to be wedged or pried apart. This paper introduces the method of vapor-assisted release

(VAR) to overcome this problem. The dielectric material is prepared with a solvent to create the right viscosity for spin coating onto a wafer. The cure cycle is stopped just short of completion. The stamp is locally heated during the imprinting step; a small amount of residual vapor is driven out of the dielectric material and causes the stamp to be released automatically. This is an important capability for low cost production. After release and removal from the lamination station, a slow cure at a lower temperature is used to stabilize the dielectric material before continuing the process.

Alignment Stack in Preparation for an Imprint Cycle

A schematic of the alignment stack is shown in Figure 1. Details of the preparation of each layer will be further described in subsequent figures. For an 8-inch wafer size the glass carrier for the embossing tool will be approximately 10 inches on a side, having a thickness of approximately 0.2 inches. For manufacturing convenience, the embossing features are created separately on a quartz wafer that is bonded to the glass carrier using a solder release layer; this allows the glass carrier to be re-used with multiple embossing wafers. The recommended solder release material is Indalloy 183 comprising 88% Au and 12% Ge, having a eutectic melting point of 356ºC. This material can be screened on as a paste, keeping the alignment targets clear. The preferred thickness of the quartz wafer is 0.5 mm. The vertical separation between alignment targets (Δy) is approximately 0.6 mm and the target layer-to-layer alignment accuracy is $\pm 2\mu$, requiring optics developed for large exposure gaps. It is difficult to expel the air between flat surfaces as they approach at distances of the order of a micron, so the lamination chamber must be evacuated. The vacuum pump performing the evacuation must tolerate noxious vapors that are emitted from the dielectric material during the heated portion of the imprint cycle. However, this creates the benefit of automatic release of the embossing tool. With some equipment and process modifications, these operations can be performed using wafer aligners and lamination presses that are available from Suss Microtec.[13]

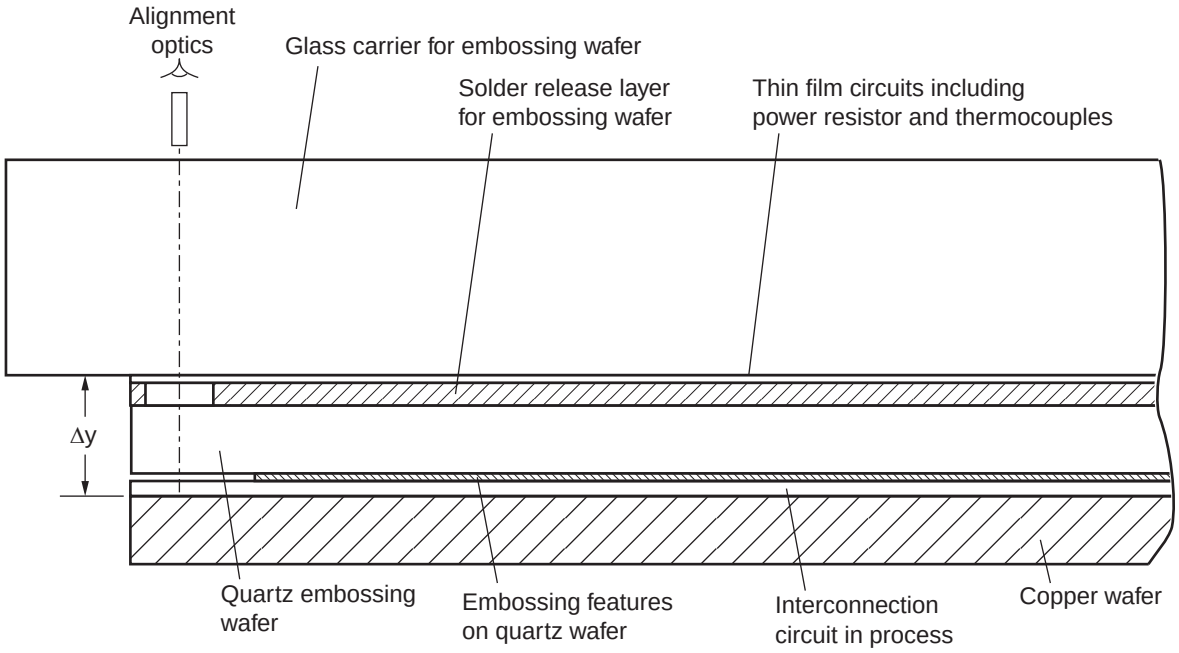

Figure 1 - A Schematic of an Alignment Stack

Preparation of the Copper Wafer Substrate for the HDI Circuit
For convenience the copper substrate for the interconnection circuit is shaped like a silicon wafer, as shown in Figure 2.

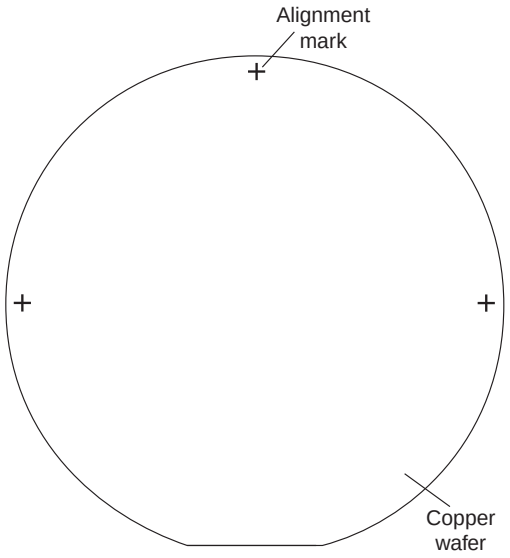

Figure 2 - Silicon Wafer

The wafer diameter can be anywhere between 4 and 12 inches. Test coupons and prototypes can be created less expensively using smaller wafers. Larger wafers can be used for production, and flat panels can also be used for the highest volumes. Flat panel display fabrication equipment is available for coating and plasma etching, up to a panel size of 1870 x 2200 mm. In the future, this could lead to imprinting methods applied to large panel sizes. Since the imprinting tool can be fabricated on a glass panel of the same size, and since the imprint cycle would be short compared with a step and repeat exposure cycle, the economics could be attractive. Whatever the substrate size, its material may be plain copper or cold-rolled dispersion strengthened copper[14] (DSC). DSC is much stronger than ordinary copper, yet its electrical and thermal properties are almost identical. The preferred thickness is 0.5 - 0.6 mm, the same as for a standard silicon wafer. This will be convenient for later chemical mechanical polishing (CMP), and also will allow post-process bending of the copper to enable improved cooling structures, as will be further described. To provide good adhesion of subsequent polymer layers and to prevent oxidation of the copper during processing the wafer is coated on both sides with Cr. Finally, alignment marks are patterned in the surface by laser machining.

Preparing the Imprinting Tool
Figure 3 shows the first step in preparing the imprinting tool: thin film Au is patterned to create a power resistor and alignment marks on a glass carrier. The power resistor is used to heat the imprinted layers selectively; this provides a new capability for multi-layer circuits and for fabricating material stacks wherein some of the layers cannot tolerate the embossing temperature of other layers. This is in contrast to conventional laminators wherein the entire stack is subjected to the same temperature. An adhesion layer of titanium is sputtered onto the wafer and then gold is sputtered or plated to a thickness of 0.5μ, creating a sheet resistivity of approximately 10mΩ/square. Patterning of the gold is achieved using a lift-off process. For a resistor with 600 squares, the total resistance is around 6Ω. At an applied voltage of 55V, the power generated is around 500W. This provides the flexibility to produce rapid heating cycles for the imprinted materials. Since the thermal mass of the imprinting region is small and is surrounded by relatively heavy members in the lamination press, cooling cycles can also be rapid. In addition, integrated temperature sensors are provided so that the heating and cooling cycles can be precisely controlled.

In Figure 4 a coating of silicon oxy-nitride (SiO_xN_y) has been applied through a mechanical mask to cover the power resistor, providing electrical isolation between the gold conductor and the thermocouple probes shown. Each thermocouple probe includes a junction formed between thin film Pt and thin film Pd[15] with a Ti adhesion layer to the underlying silicon oxy-nitride. It will be useful to monitor the rate of temperature stabilization as well as the maximum temperature, so probe sites near the center and the edge of the power resistor are included. The probe near the edge of the glass substrate provides a reading of the temperature seen by the adjacent surfaces in the lamination chamber, and a limit may be set for proper equipment function. The preferred temperature for imprinting the Cytop material is 220ºC, when it has a low viscosity. At 410ºC it begins to decompose and toxic materials are formed.

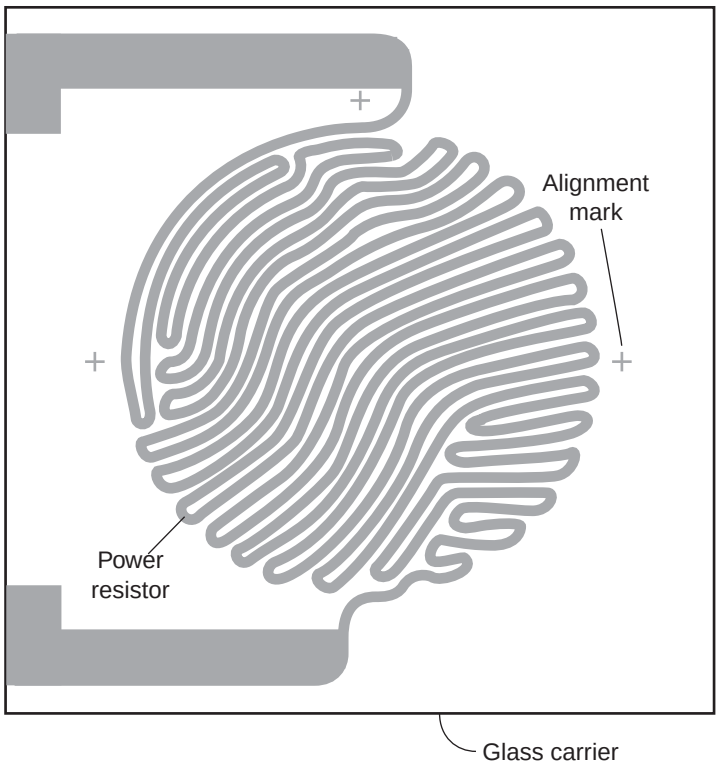

Figure 3 - First Step in Preparing the Imprinting Tool

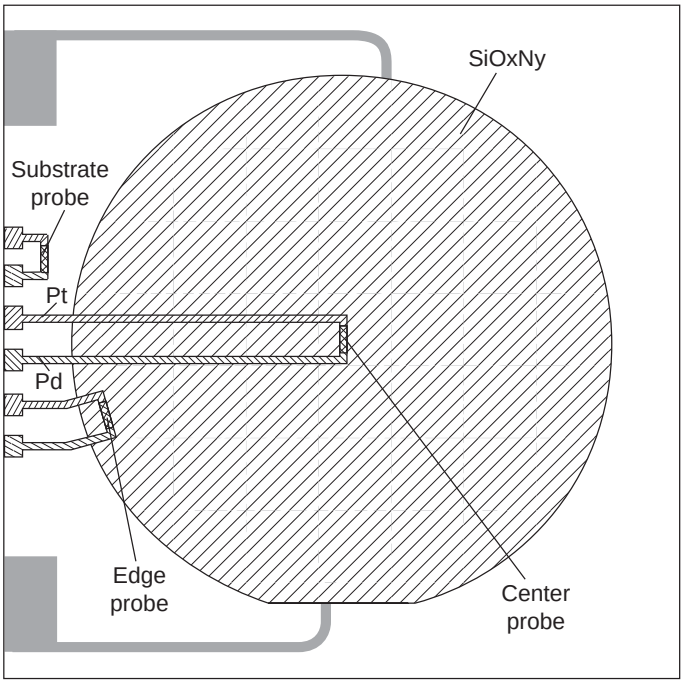

Figure 4 - Coating of Silicon Oxy-Nitride

The embossing features are patterned on a silicon wafer (or glass panel) using a thick film resist. Tokyo Ohka Kogyo[16] manufactures a suitable resist; 6-8μ thick resist layers can be spin-cast and patterned to form trench and via features. The sidewalls of the features preferably have a positive taper of approximately 5 degrees, and the taper angle can be controlled by varying the exposure intensity.[17] The resist is hard cured and then the pattern is transferred to a quartz wafer of similar dimensions using electroformed nickel in place of the resist.[18] This process involves producing negative and positive topographies. Such an electroformed nickel tool is suitable for production, reportedly producing around 100,000 imprints per tool. Faster turn-around can potentially be achieved by making a short-run imprinting tool using the imprinting fabrication facility. In this case, the resist image is modified to allow for a 1-2μ overcoat of plated nickel. This wall thickness of nickel

may be strong enough to fabricate prototype quantities of a new design, especially if the dielectric material has a low viscosity when heated. If this approach proves feasible for the chosen materials it could significantly shorten the development time of an imprinted circuit, as well as reduce the cost of tooling.

Figure 5 shows the final embossing tool, after bonding the quartz wafer to the glass carrier of Figure 4 using a solder release layer. The preferred material for the solder release layer is Indalloy 183[19] with a melting point of 356ºC. As mentioned previously, it can be screened onto the wafer as a paste, keeping the alignment marks clear. A square area is available as shown for the embossing features associated with an HDI circuit. High-performance cables can be produced using the same HDI process, so the peripheral regions of the wafer may be utilized to include them. The cables will have controlled impedance traces that terminate at each end in an array of gold stud bumps or wells, with the bumps or wells at a 100µ pitch. Because of the copper backing, the cables can also be formed into three-dimensional shapes.

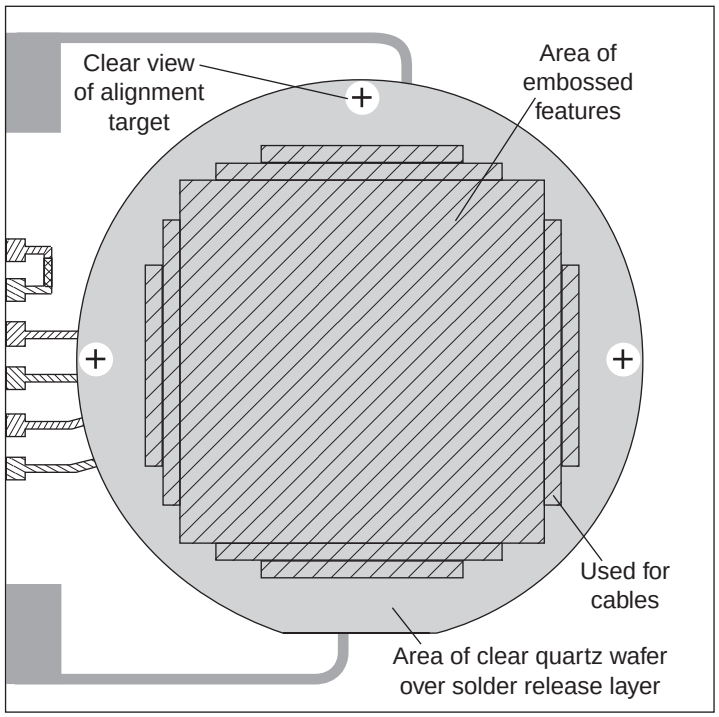

Figure 5 - Embossing Tool, after Bonding the Quartz Wafer to the Glass Carrier

The Imprinting Process

Each layer of an interconnection circuit can be imprinted using a tool with trench features and via features. The trench features will be used to create copper lines or traces, and the via features will be used to create vias that reach down to a trace on a layer underneath. The basic imprinting geometries are shown in Figure 6.

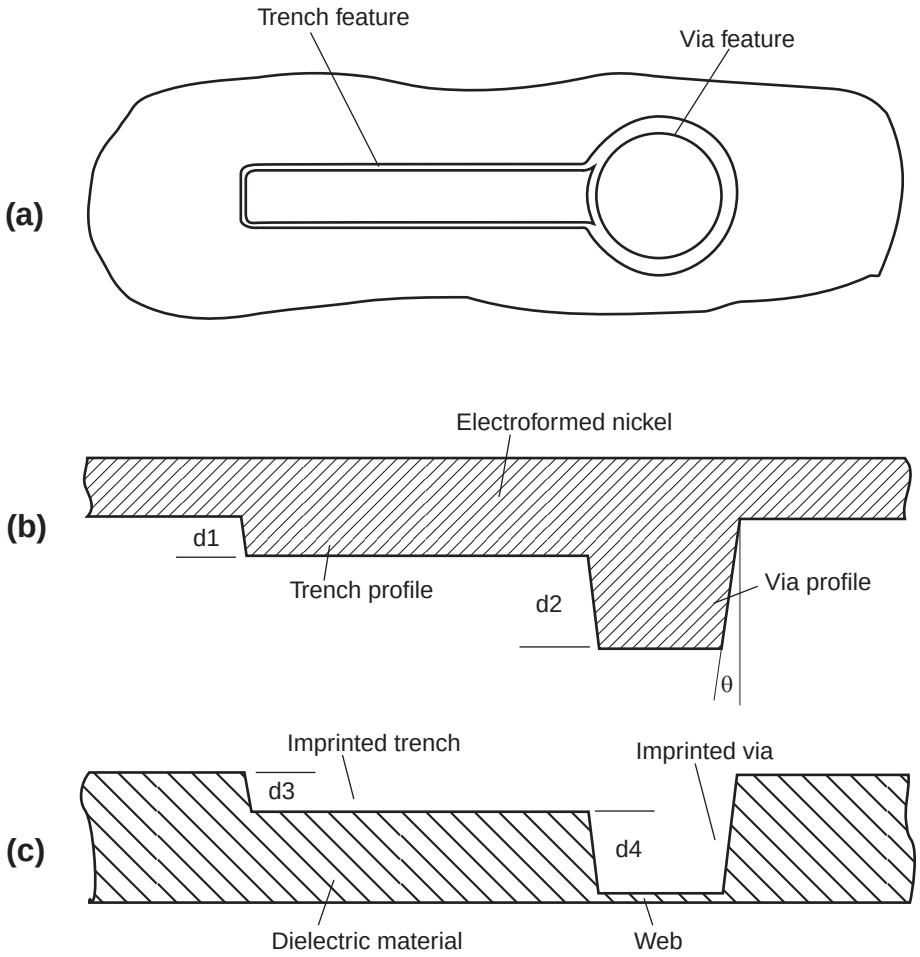

Figure 6 - Basic Imprinting Geometries

Figure 6(a) shows a top view of a fragment of an imprinting tool that includes a trench feature and a via feature. Figure 6(b) shows the same fragment in cross-section, with a depth d1 for the trench feature, and a depth d2 for the via feature. The positive taper angle, θ, is shown which is preferably around 5° for ease of release. Also the aspect ratio of the via (height divided by diameter) is preferably not greater than around 4 for ease of release, and also for ease of a subsequent electroplating step that fills the vias with copper. Figure 6(c) shows the result of imprinting the tool into the dielectric material. The spreading characteristics of the dielectric material depend on its viscous properties, but it is typical for the trench to imprint faithfully (d3=d1) and for the via imprint to leave a thin web remaining at the bottom (d4<d2). This would prevent contact between the via metal and an underlying trace, so it is removed with a dry plasma etch.

The metallization process

Figure 7 shows a summary of the process steps for metallizing with copper. In Figure 7(a) the previous layer has been polished and an exposed copper trace is shown. Figure 7(b) shows the profile after the imprinting step, including trenches and vias, and with a thin web remaining at the bottom of the via. Figure 7(c) shows the result of dry plasma etching to remove the web, exposing the copper trace beneath. Figure 7(d) shows a thin layer of sputtered Ti/Cu coating the entire surface and Figure 7(e) shows the result of electroplating the copper. Modern electroplating processes include layered chemical baths[20], and periodic pulse reversing power supplies[21] to effect plating from the bottom up, thus achieving void free via structures. Figure 7(f) shows the completed copper layer after CMP.

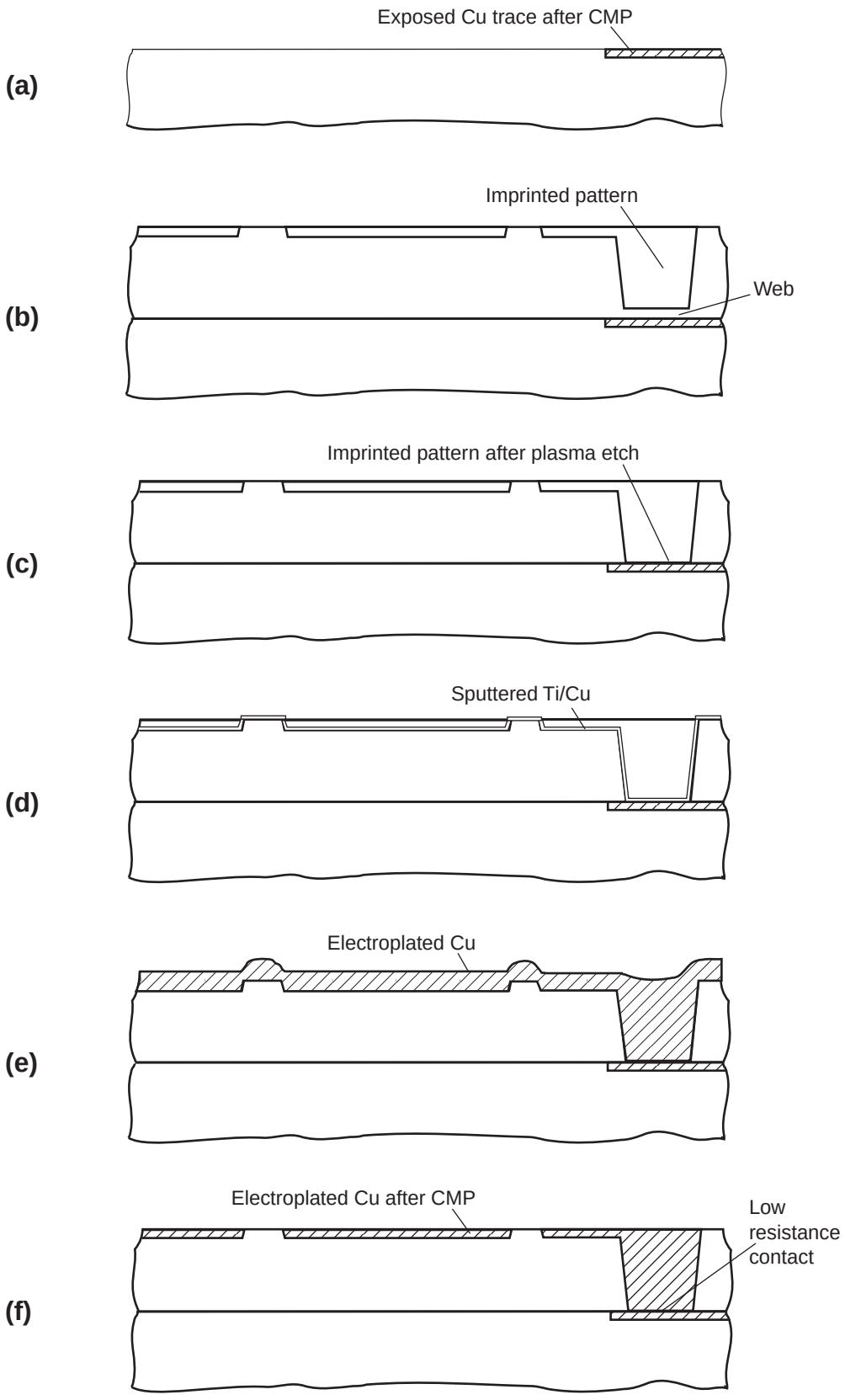

Figure 7 - Summary of the Process Steps for Metallizing with Copper

Imprinting the wells of the special assembly layer

Imprinting and CMP provide an effective and inexpensive way to create the wells, as shown in Figure 8. Figure 8(a) shows a completed interconnection circuit with exposed copper traces. In Figure 8(b), a dielectric material such as an unfilled epoxy has been spun onto the wafer, and imprinted to form the shape of the well. For the proposed structure, the epoxy material is chosen to accommodate a subsequent solder melt temperature of 143ºC. A web of dielectric material remains and is subsequently removed by dry plasma etching. A Ti/Ni coating is applied by sputtering as shown in Figure 8(c); the nickel forms a diffusion barrier to the copper, to prevent contamination of the solder materials. Figure 8(d) shows that CMP has removed the Ti/Ni coating, except in the wells. In Figure 8(e), an indium-based solder has been deposited in the wells using a squeegee. The amount of material in a well is 1.5×10^{-8} gm, at a material cost of approximately $3.48/gm. The cost of the wells is primarily in the patterning of an extra layer, estimated at $20 initially. Assuming 100,000 wells per 8-inch wafer for moderately I/O intensive chips results in a fabrication cost of 0.02 cents/well. As will be discussed, the cost per stud bump is currently around 0.04 cents. Adding the well cost of 0.02 cents to the stud bump cost of 0.04 cents provides a total cost of approximately 0.06 cents for each bump/well connection under these assumptions. This figure does not include allowances for yield and rework costs. The cost per well is further reduced if a large panel size is used, and ongoing efforts to increase the bumping speed will further reduce the cost per stud bump.

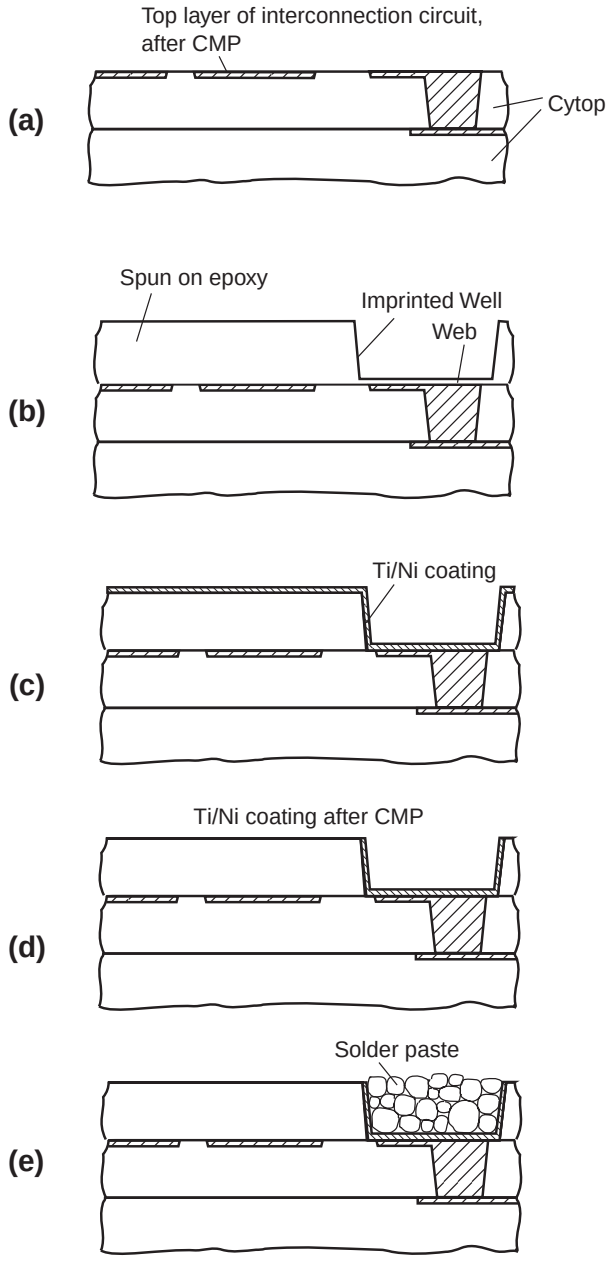

Figure 8 - Imprinting and CMP Provide an Effective and Inexpensive Way to Create the Wells

The Multi-Layer Imprinting Problem

In a multi-layer circuit, there are multiple dielectric layers. If the same dielectric is used at each layer, with the same softening temperature, then how are the bottom layers protected from collapse or distortion when a new top layer is imprinted? This paper introduces two methods to solve this problem: the use of support rails near the edge of each layer and selective heating of the dielectric stack. The support rails provide a limit stop for the imprinting action, and the selective heating provides for heating and softening of only the topmost dielectric layer. Figure 9 shows the support rails. They are provided near the outer edge of the embossed region. The sinusoidal overlapping pattern is tolerant of misalignment between layers, and the open structure enables good flow of the dielectric material during the imprinting cycle.

Figures 10 and 11 illustrate selective heating of the dielectric stack. In Figure 10 the embossing tool is spaced apart from the top dielectric layer, and heated using the power resistor to selectively soften the top layer.

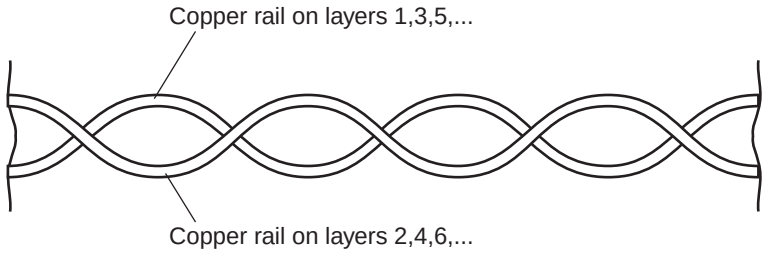

Figure 9 - Support Rails

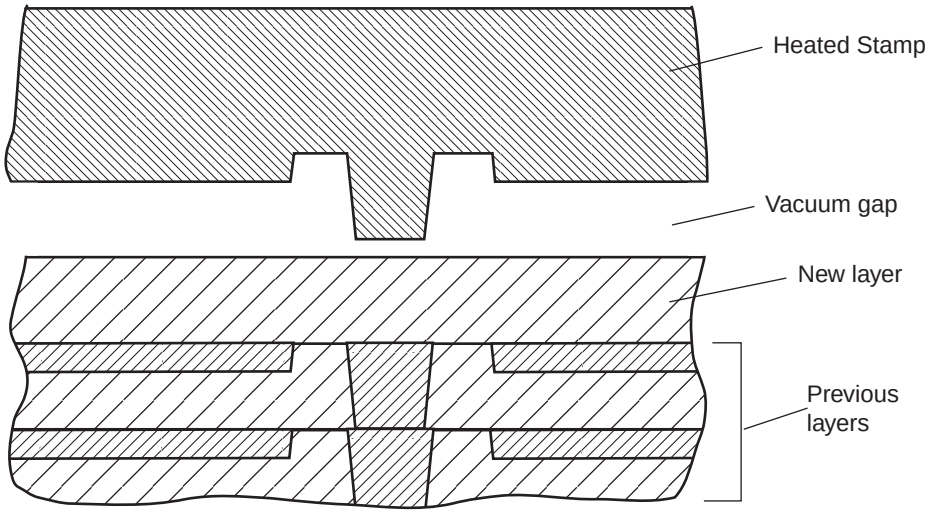

Figure 10 – Heating of the Top Layer of the Dielectric Stack

In Figure 11, the tool has been pressed into the dielectric layer. The nickel embossing features are maintained at 220ºC while they slowly penetrate the Cytop. A control system can sense the temperatures at the thermocouple probes and adjust the current flowing in the power resistor to achieve this. When full penetration of the embossing tool has been achieved the copper rail features of the tool will be in contact with or in close proximity to the copper rail of the previous layer. This end point can be detected by the measured amount of penetration, or the degree of resistance to the imprinting stroke. Vaporization of residual solvent in the dielectric will be acting to eject the embossing tool. When the end point is reached, the lamination force is removed, and the embossing tool will eject automatically. Current to the power resistor is then immediately ramped to zero.

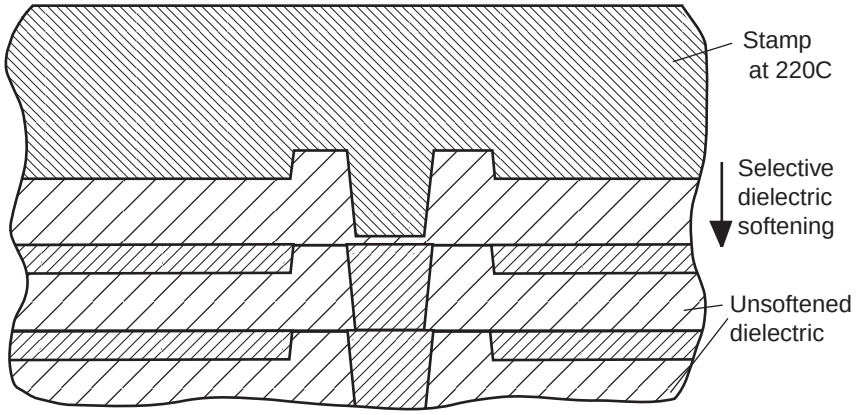

Figure 11 – Pressing the Stamp into the Dielectric

Gold Stud Bump

Having described the imprinting process, we shall turn our attention to flip chip assembly. Figure 12 shows a stud bump that can be created by the WaferPro bonder from Kulicke and Soffa[22]. The process for forming the ball of the stud bump is the same as used in a conventional wire bonder, employing the application of heat, pressure, and ultrasonic energy. This process is robust and can be applied to I/O pads of chips from almost any vendor. If an 18μ diameter gold wire is used, the bonder can be configured to make stud bumps with a ball diameter of around 50μ, and also an overall height of 50μ. This is a smaller diameter than most solder balls used in flip chip assembly and it enables tighter pad pitches; a pad pitch of 100μ is used in this paper, but finer pitches are possible. The beard is created by precisely shearing the gold wire as the bonding tool pulls away from the bonding surface. Height uniformity is excellent, with the tips of the beards coplanar within a few microns across a 200 mm wafer. For 100k bumps on a 200mm wafer, the cost per stud bump is approximately 0.04 cents, assuming gold at $385/oz and a production environment. Because gold is more ductile than tin-lead solder, and because the stud bump has a pointed shape, it is more mechanically compliant than a solder ball equivalent.

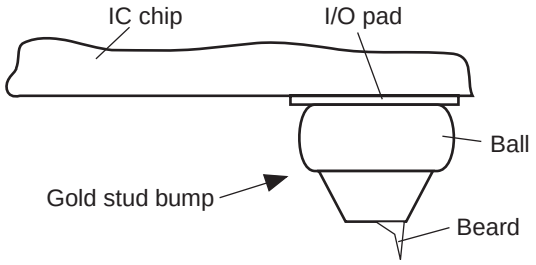

Figure 12 - Stud Bump

Flip Chip Connection

An IC chip is aligned, and the stud bumps are inserted into the wells as shown in Figure 13(a). Because the solder paste is soft, and because the well has a depth of approximately 15μ, the chips can be inserted reliably without breakage. The beard is soft and conforms to the bottom of the well.

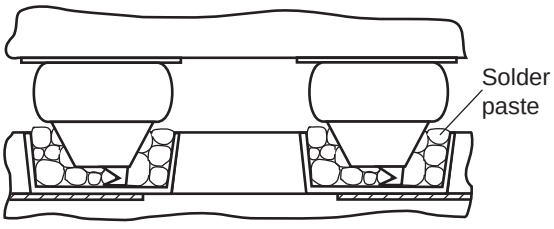

Figure 13(a) - Stud Bumps are Inserted into the Wells

Figure 13(b) shows the completed bump/well connection, at a pitch of 100μ. The solder paste has been melted to form a permanent connection, although it can still be reworked, as will be further described.

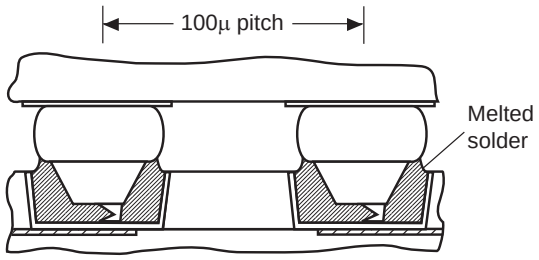

Figure 13(b) - Completed Bump/Well Connection

Controlled impedance structures

Taking advantage of the precision of imprinting and CMP, the layouts described herein have the design goal of routing signals with maximum density at a 10GHz sinusoidal rate. Copper has a resistivity of 1.673 μΩ-cm and a skin depth of 0.65μ at 10 GHz. A trace thickness of 2μ is chosen to provide ample manufacturing tolerance above the required 1.3μ. Of the available dielectric materials, Cytop is chosen because it can be effectively patterned using imprinting methods and because of its excellent dielectric properties: relative dielectric constant of 2.1 and dissipation factor of 0.0007 at 10 GHz. An offset stripline, Figure 15, with a characteristic impedance of 50Ω is used for single-ended signals, and a broadside-coupled stripline, Figure 14, with a differential impedance of 100Ω is used for differential signals. The characteristic impedances are calculated using boundary finite element analysis provided in the Si8000 tool from Polar Instruments[23]. The design approach is to optimize the case of short traces, and to keep the package or board size as small as possible. The narrow traces recommended have significant resistance losses and the maximum acceptable trace length is yet to be determined in practical applications. The differential pair structure and the single-ended structure have different line widths but the same vertical dimensions for copper and dielectric; this means that differential and single-ended circuits can co-exist on the same board.

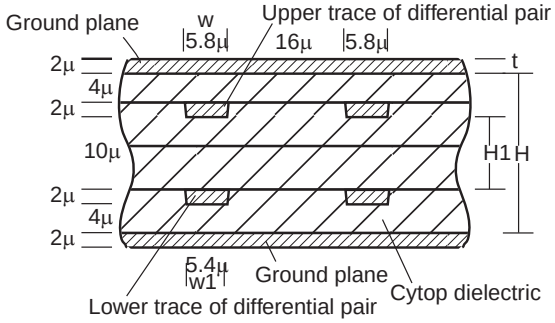

Figure 14, Z_{diff} = 100Ω - Broadside-Coupled Stripline

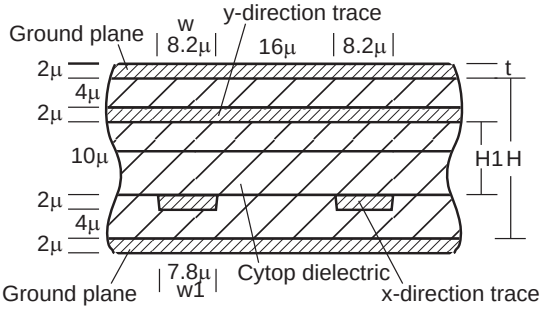

Figure 15, Z_0 = 50Ω Offset Stripline

Figure 16 shows a layer stack up using the structures of Figures 14 and 15. The signal vias have adjacent ground structures that provide a return path and controlled impedance during the vertical transition. The overall structure can include capacitors as shown, and inductors at the middle level. The relative scale of the bump/well connection is also shown. For 3D packaging structures described in section XIV, a potential problem may be that the epoxy materials crack when folded. This needs to be tested; heating of the material while folding may help to avoid cracking. If cracking cannot be eliminated, other composites using polyimide as the base material may be pursued.

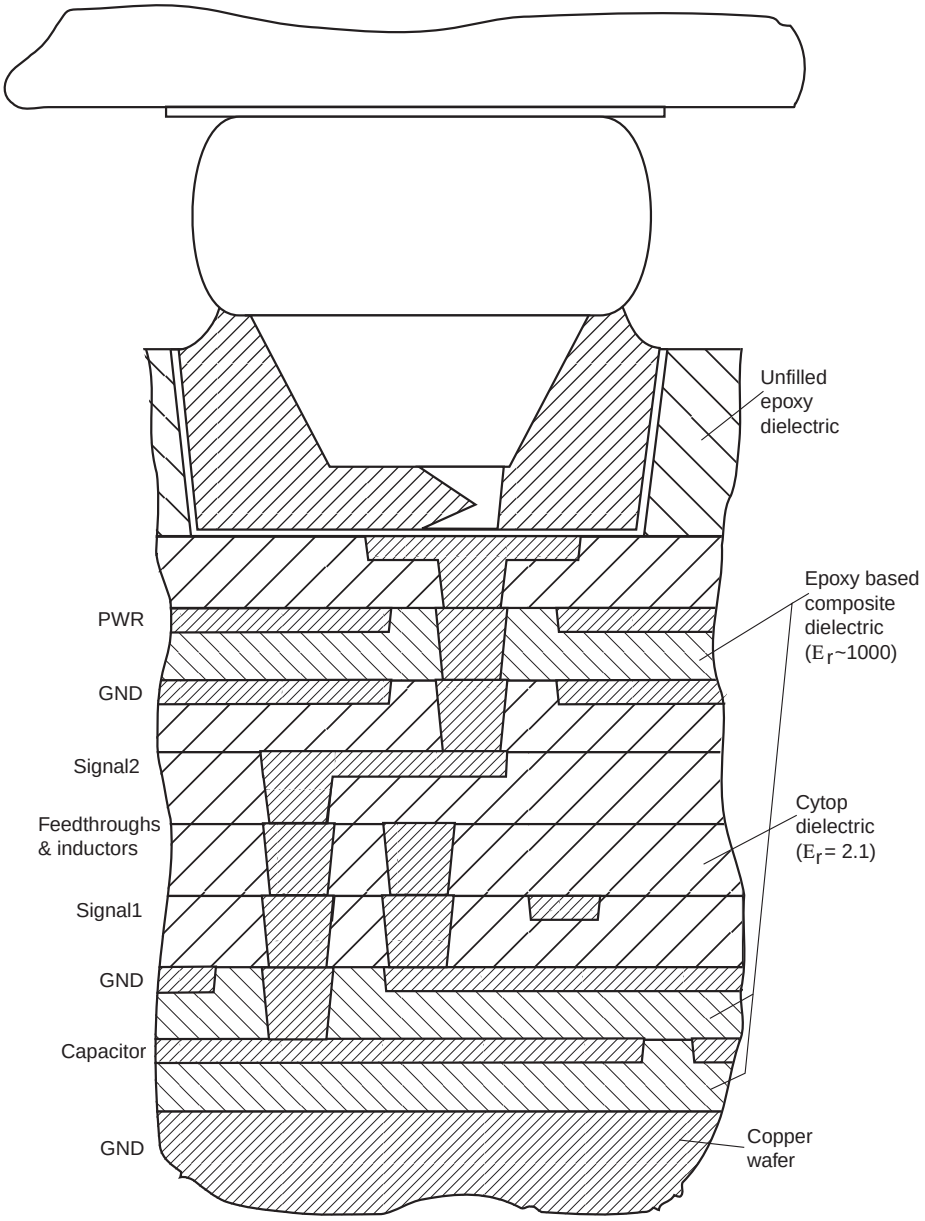

Figure 16 - Layer Stack Up Using the Structures of Figures 14 and 15

Using the Power Mesh Architecture described by Happy Holden[24] the number of imprinted layers can be reduced from 9 to 4, as shown in Figure 17. This is accomplished by laying signal traces between power traces on each signal/power mesh layer. Signal and power traces are orthogonal on the two layers. Controlled impedance connections are implemented as offset coplanar striplines. Although high-value capacitors and small inductors are not provided with this arrangement, the manufacturing cost is roughly halved.

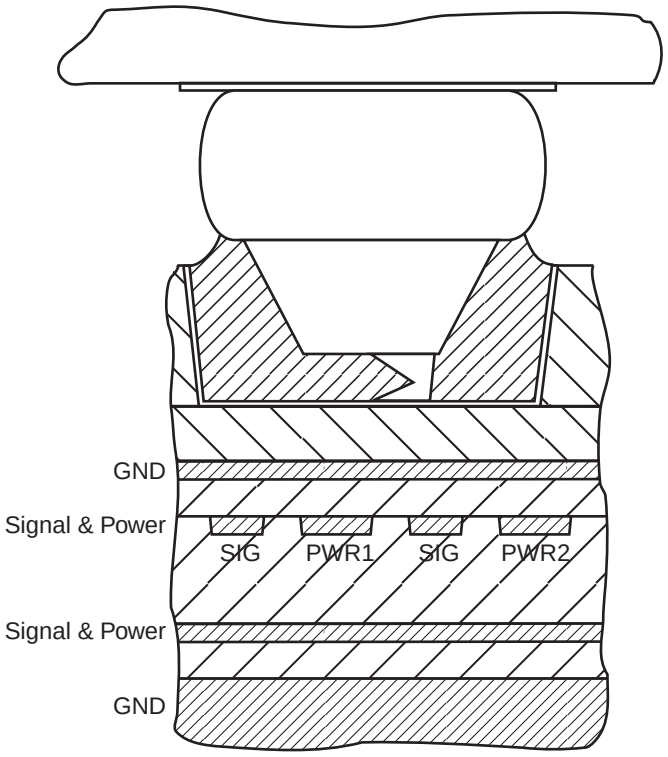

Figure 17 – Reduction in Imprinted Layers with Power Mesh Architecture

Functional Testing at full System Speed Using Tester-On-Board

It is not much use having the capability of creating complex flip chip assemblies if they cannot be tested and reworked. High speed functional testers require the system nodes to be connected to the tester nodes using short leads, in order to sense dynamic behavior at high speed. For wafers and packaged parts this can be accomplished using standardized test interfaces or fixtures. However, there are currently no good ways to accomplish this for board assemblies comprising a number of flip chip mounted die. This helps explain why we have not seen system assemblies including a large number (say greater than 10) of flip chip mounted die. Figure 18 shows a functional block diagram for Tester On Board (TOB). In this method, a test chip is included on the system board. It provides high-speed sampling circuits and comparators, and interfaces with a support computer for low-speed transfers of test files. The support computer has a plug-in board that handles low-speed testing chores such as boundary scan. For failing systems, the test operator is guided by diagnostic software contained in the support computer, so that defective chips can be identified and replaced. The rework process involves heating the copper wafer to a temperature below the melting point of the solder in the wells, directing hot inert gas at the defective component so that its solder melts (and not that of its neighbors), and the stud bumps are withdrawn from the wells. Touchup may involve cleaning the area around the wells, and adding more solder. Then a new part can be assembled and the system retested. This rework capability may be available even at dense pad pitches of 100μ or less.

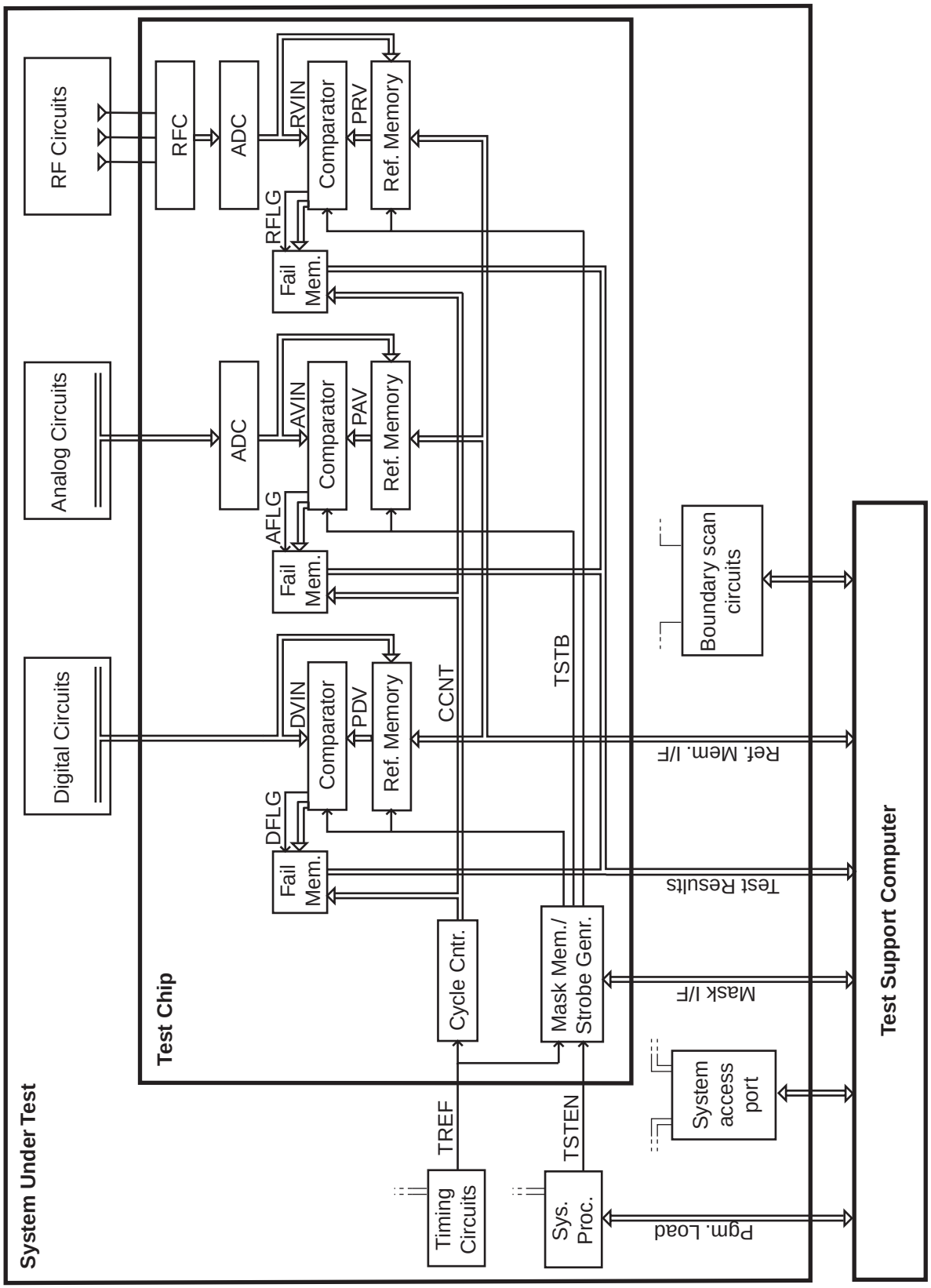

Figure 18 - Functional Block Diagram for Tester On Board (TOB).

A circuit Partitioned by Signal Type
Figure 19 shows a circuit assembly wherein the signal types are separated for convenience and electrical isolation. Also, the flip chip mounted chips are arrayed in rows, with clear areas between the rows. The clear areas may be used to create folds in the assembly after all testing and rework is completed. Many of the chips in this assembly may be integrated passives, attached using the bump/well methodology.

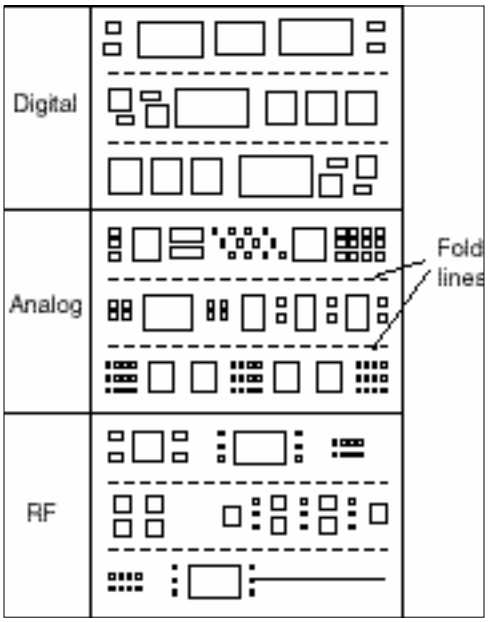

Figure 19 - Circuit Assembly wherein the Signal Types are Separated for Convenience and Electrical Isolation

Concept for Cooling and Isolation of Component Groups
Figure 20 shows one possible arrangement for folding the circuit assembly and providing good heat-sinking capability. In addition to providing effective thermal paths for heat dissipation, the folded copper provides shielded compartments that effectively isolate component groups from one another, from the point of view of electrical interference.

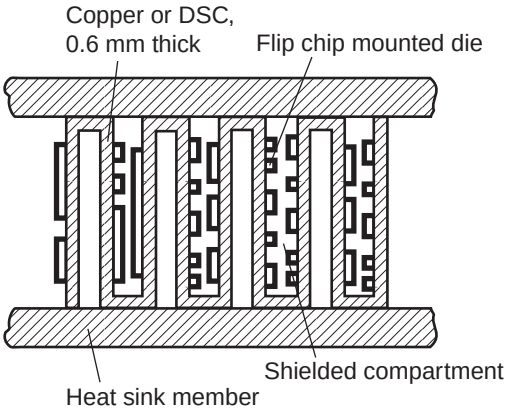

Figure 20 - One Possible Arrangement for Folding the Circuit Assembly and Providing Good Heat-Sinking Capability

Conclusion
At a conceptual level, new techniques for flip chip assembly have been proposed. Imprinting methods are presented as a means to produce precise HDI circuits and circuit assemblies at low cost. New testing and rework methodologies have been described. The proposed structures need to be tested and characterized; the estimates and projections contained herein provide an idea of what might be possible.

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3. Dr. Shiuh-Kao Chiang, Prismark Presentation, ECTC Panel Discussion, May 2003
4. Two-sided embossing tools have been used to produce 1μ accuracy between a single pair of layers, but no similar accuracy between such pairs within a stack.
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Flip Chip Connections Using Bumps, Wells, and Imprinting

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Outline of Presentation

- Current Impediments to Flip Chip
- Solution Space
- Potential Results
- Proposed HDI* Structure: Materials
- Proposed HDI Structure: Key Dimensions
- Review Imprinting Basics
- Imprinting Technique: Precision Alignment
- Imprinting Technique: Selected Heating of Dielectric Stack
- Thin Film Circuits for Selective Heating
- Imprinting Technique: Vapor Assisted Release (VAR)
- Imprinting Technique: Limit Stop Using Guard Rails
- Escape Routing
- System In Package
- Heat Sink Arrangement
- HDI Cable
- Conclusion

* High Density Interconnect

Current Impediments to Flip Chip

- **Lack of rework capability**
- **Poor Cooling**
- **High cost per lead**
- **Availability of Known Good Die**

Solution Space

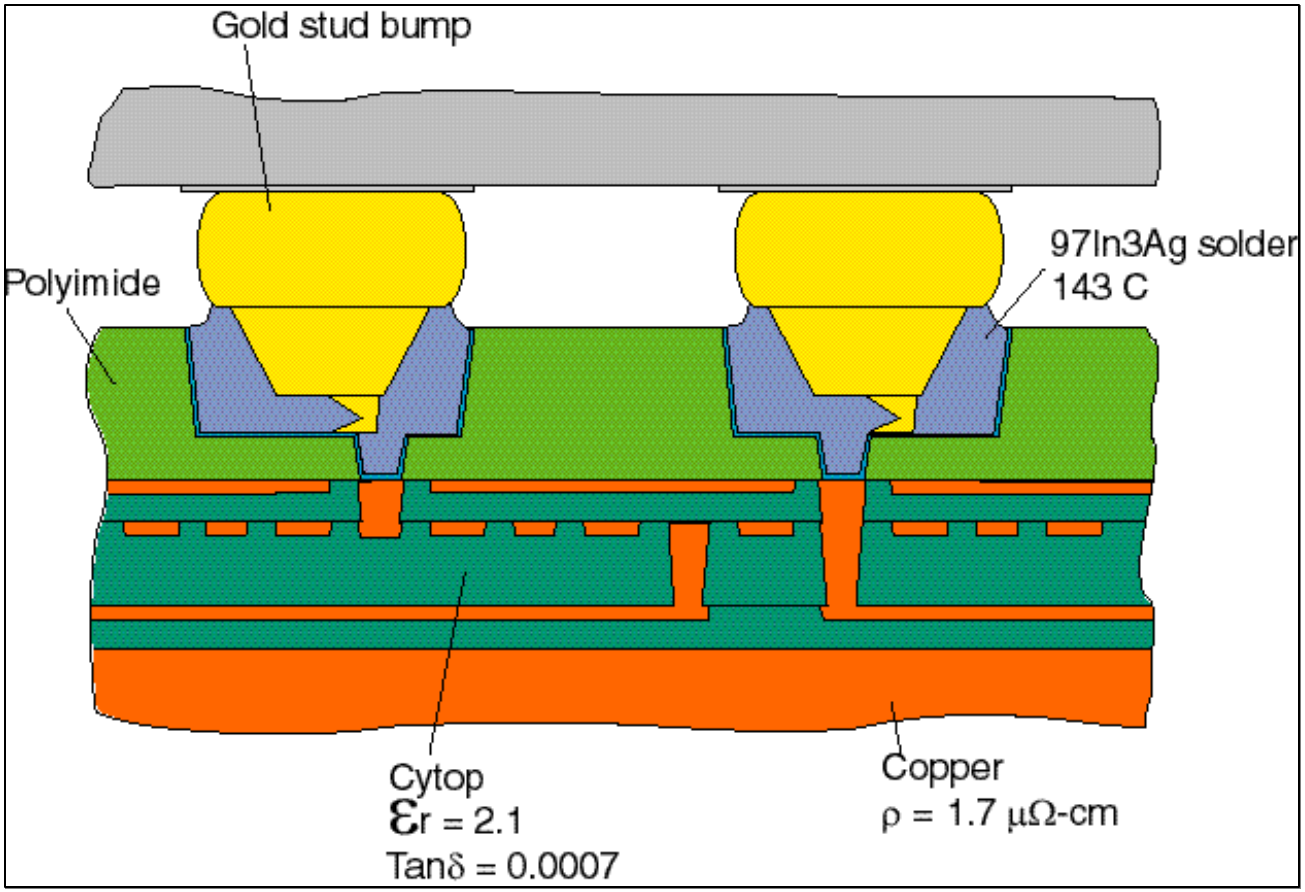
- **Bumps & Wells => Effective Rework**
- **Enhanced Imprinting Method + CMP***
  - Dual Damascene Copper circuits
  - Low fabrication cost
- **New (Test + Burn In + Rework) methodology**
  - Tester On Board (TOB)
- **New dielectric material - Cytop**

* Chemical/Mechanical Polishing

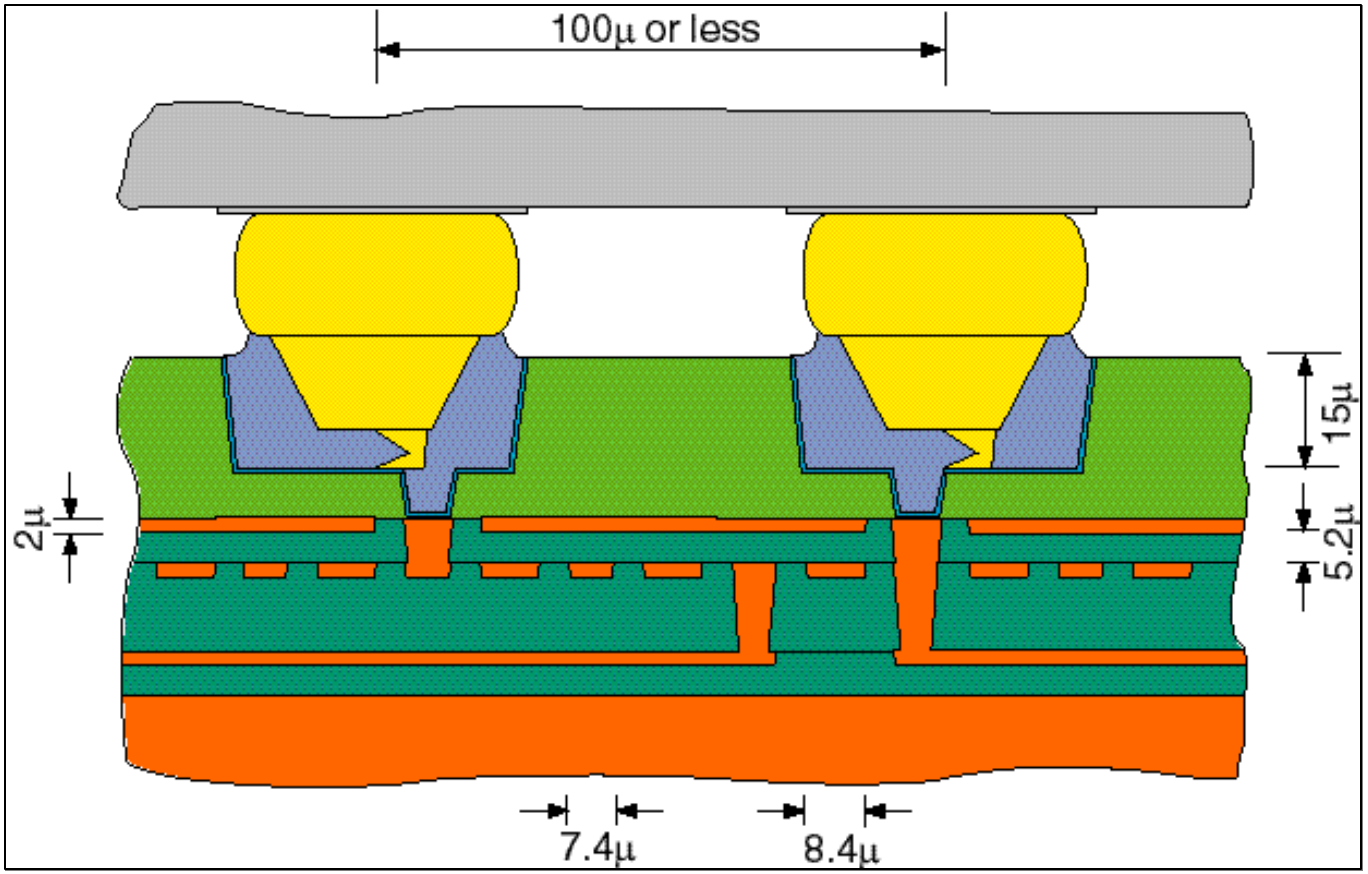
Potential Results

- **Practical and effective rework**
- **Effective cooling**
- **~ 0.06 cents per lead**
- **Plus:**
  - 10 Gbps performance
  - New complexity limit for testable/reworkable flip chip assemblies
  - HDI boards and cables, using the same techniques

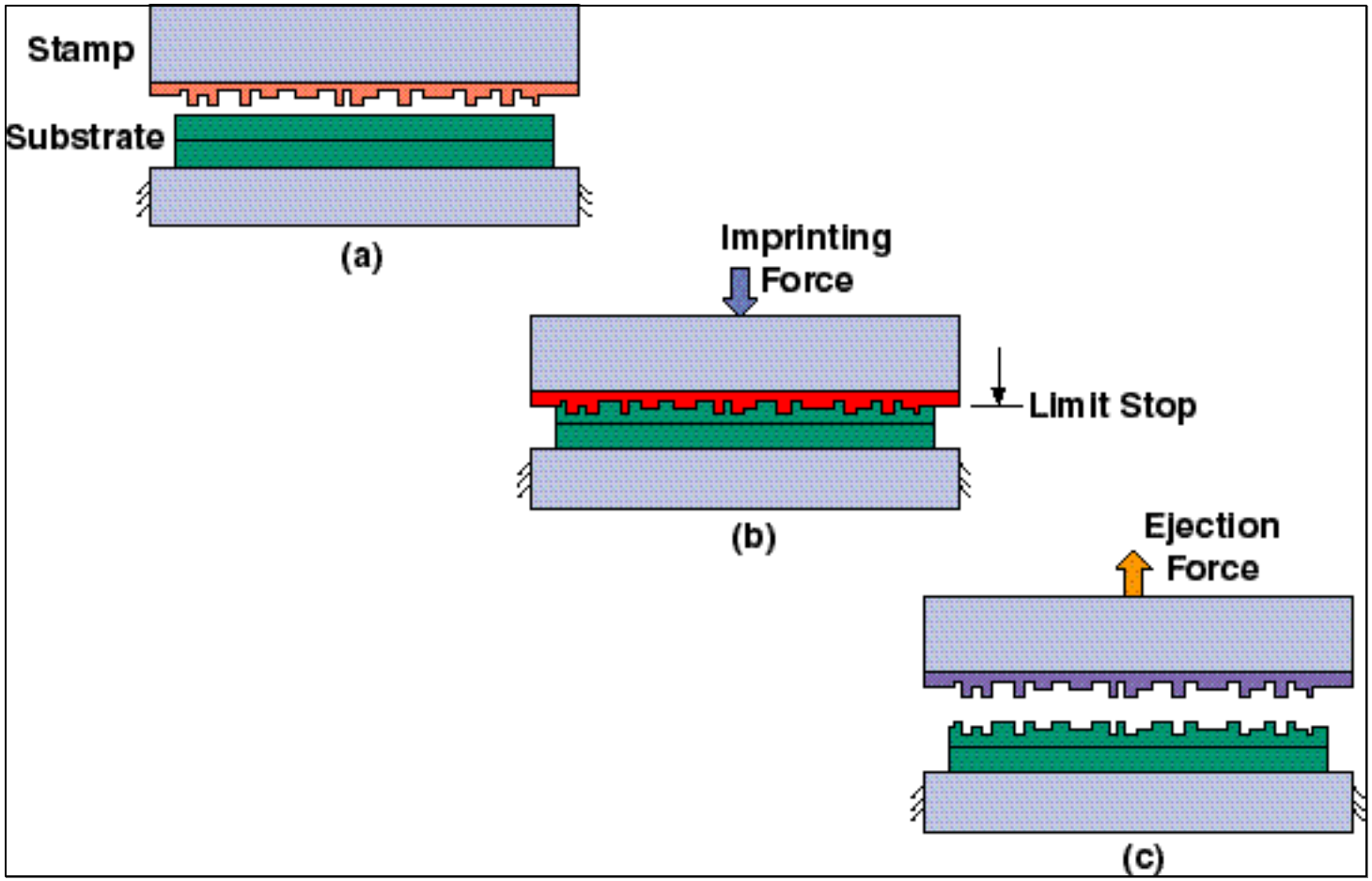
Proposed HDI structure: Materials



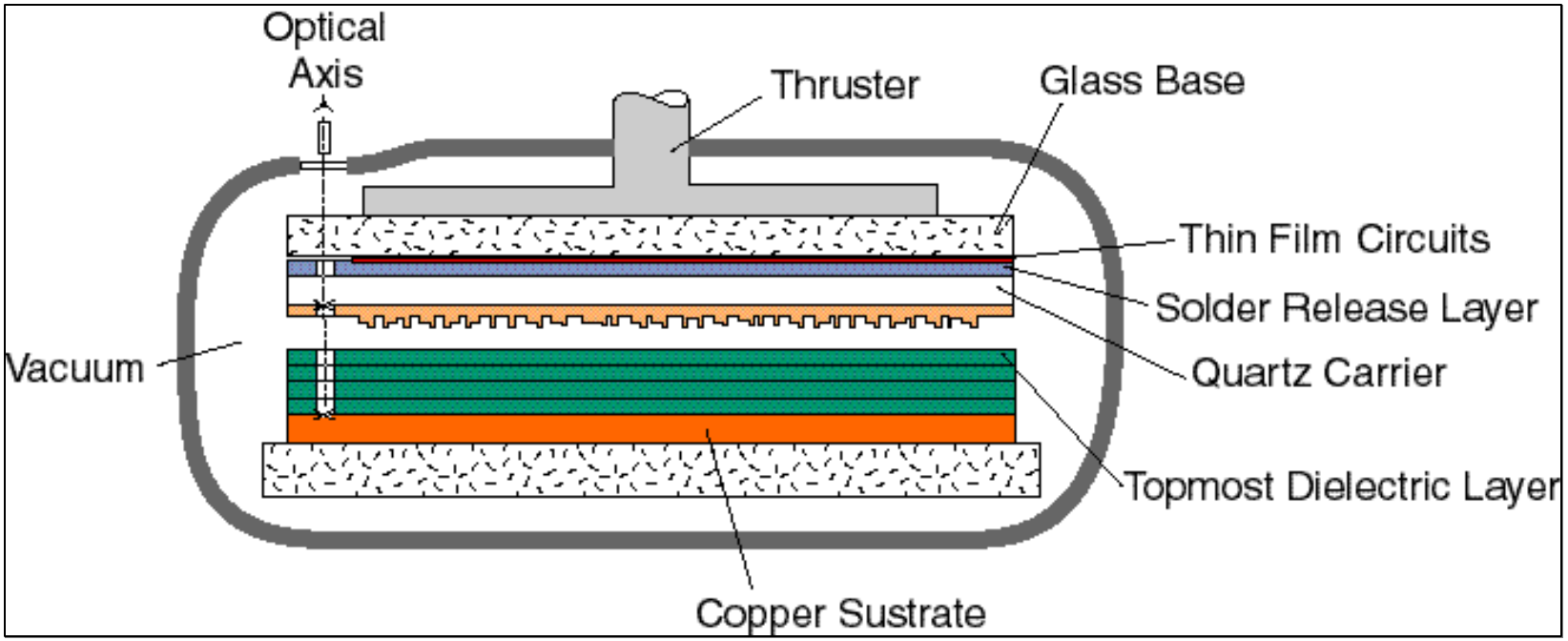
Proposed HDI Structure: Key Dimensions



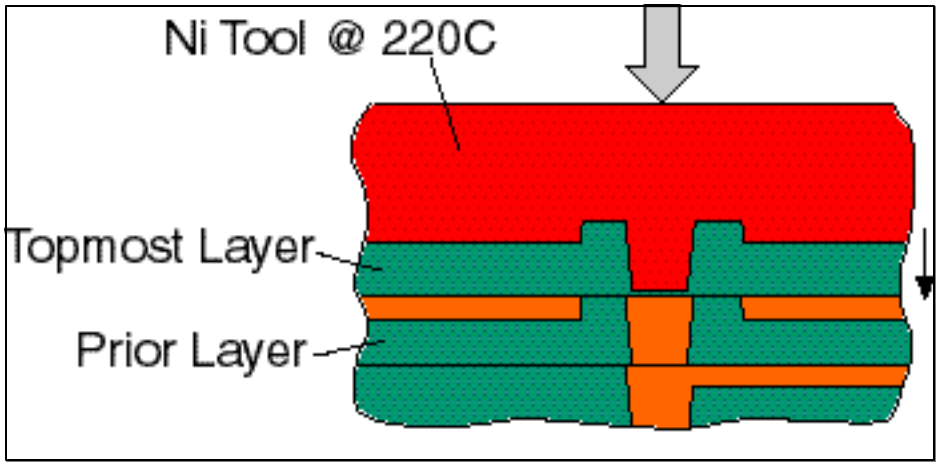
Review Imprinting Basics



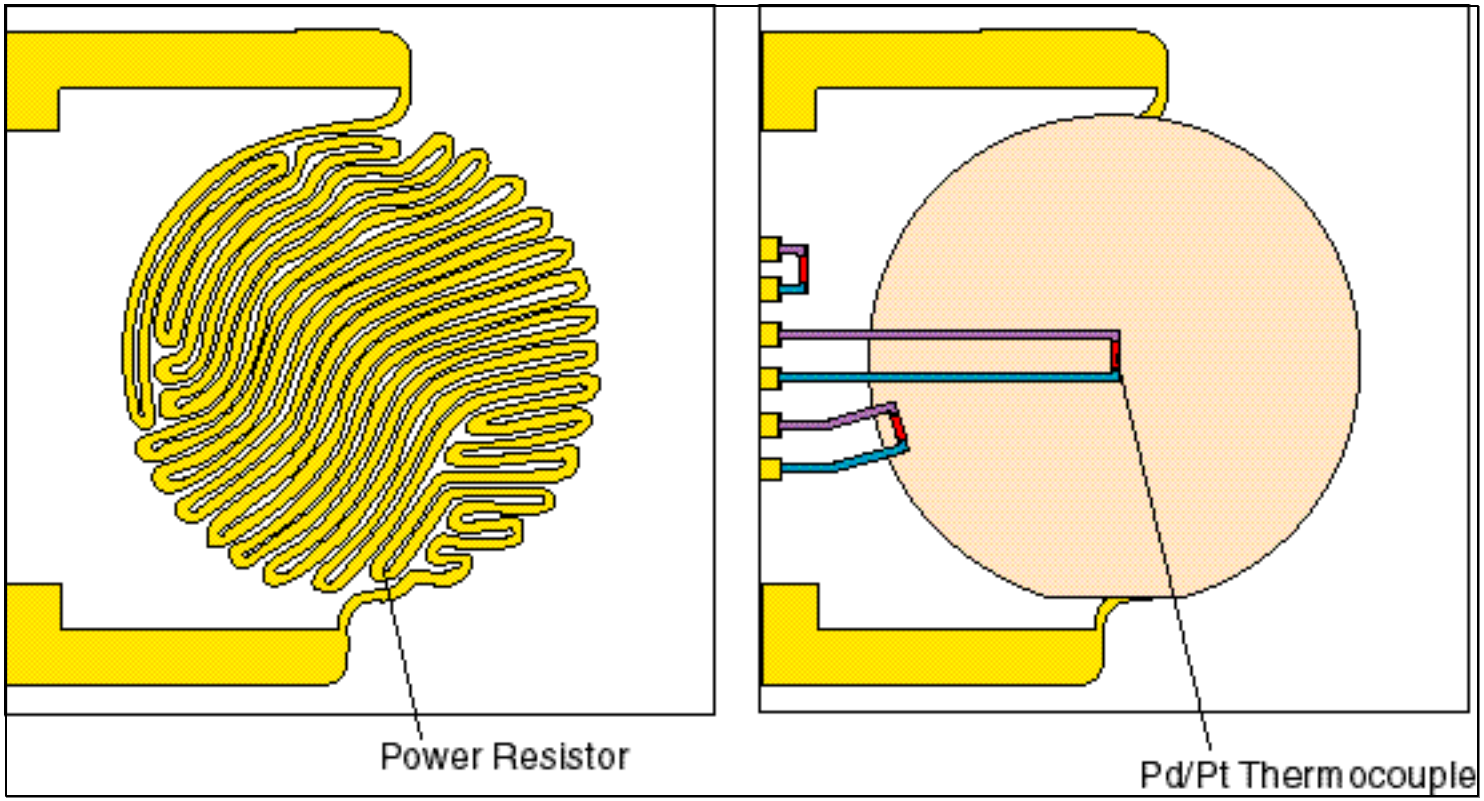
Imprinting Technique: Precision Alignment



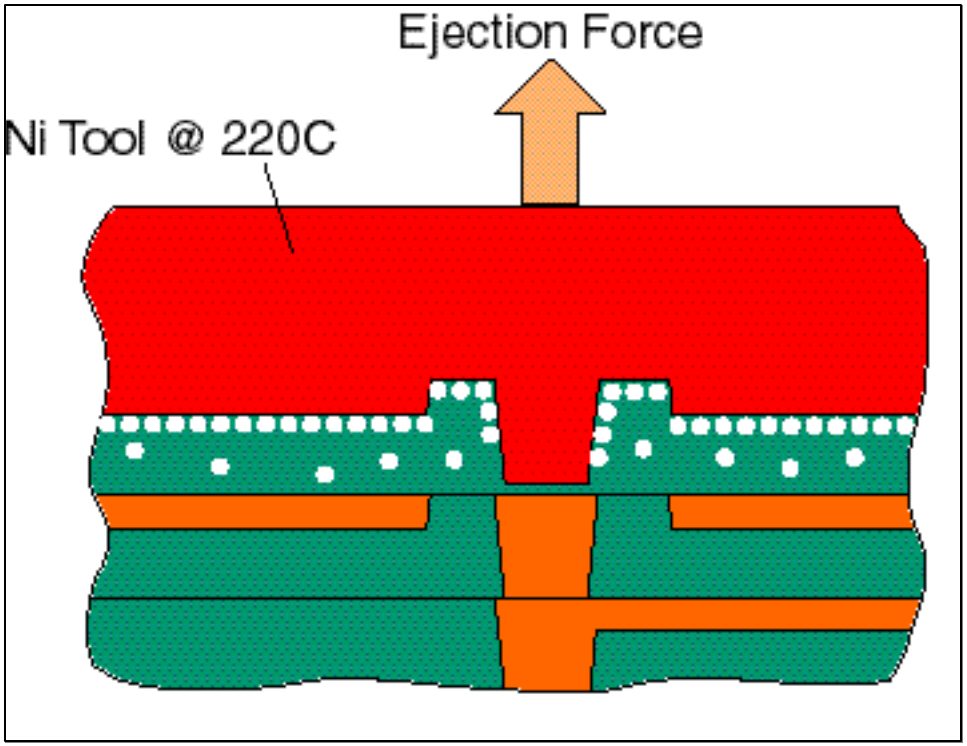
Imprinting Technique: Selected Heating of Dielectric Stack



Thin Film Circuits for Selective Heating



Imprinting Technique: Vapor Assisted Release (VAR)



Imprinting Technique: Limit Stop Using Guard Rails

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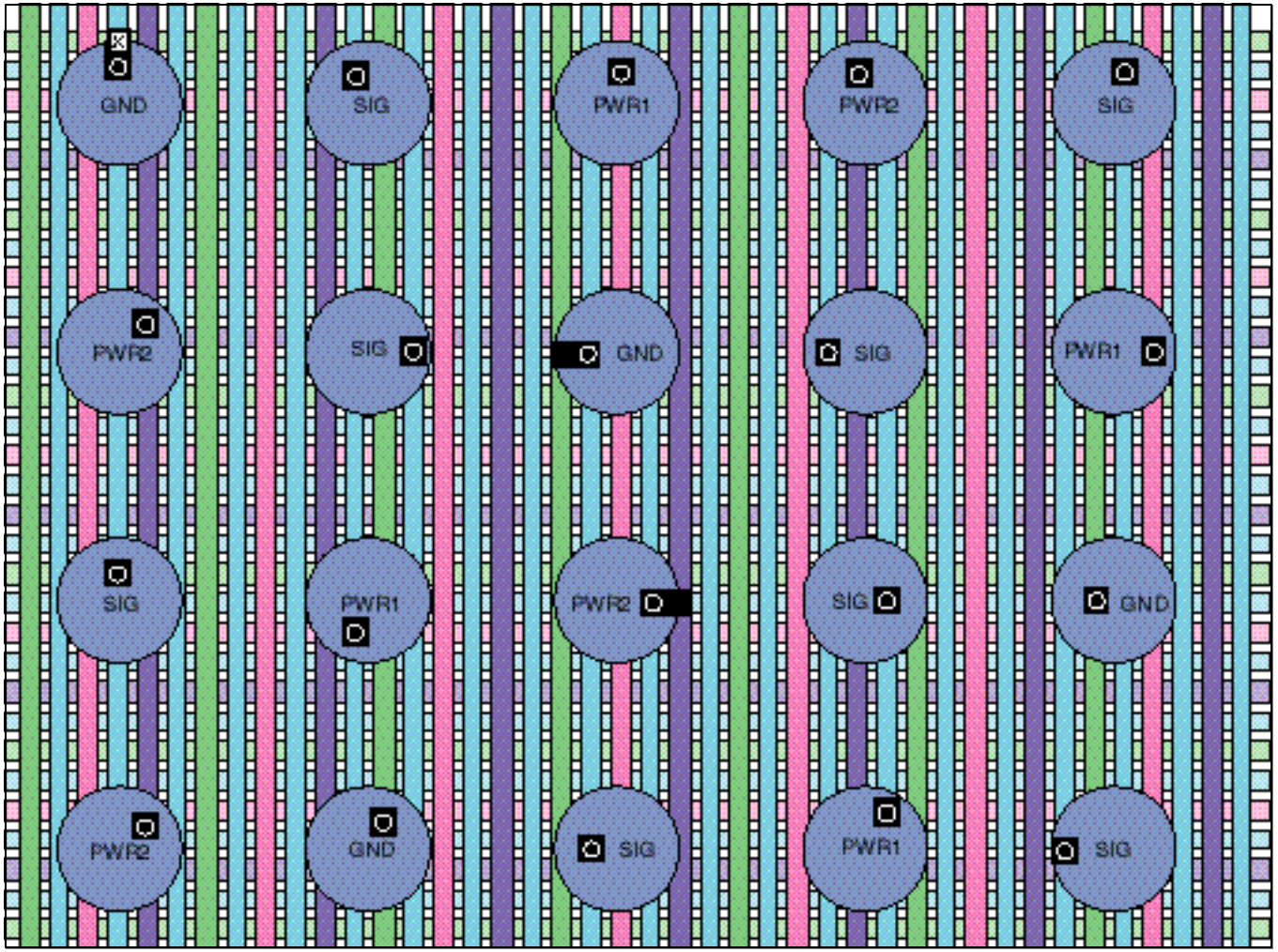
Escape Routing



System In Package

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Heat Sink Arrangement

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HDI Cable

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Conclusion

- **Rework is achievable**
- **Good cooling is achievable**
- **~ 0.06 cents per lead is achievable**
- **Next Step:**
  - **Characterization**