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Enhanced Eutectic Solder Bump for Increased Flip Chip Reliability

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Abstract
Applications using flip chips in high temperature and high current designs have increased in recent years, and this trend is expected to continue. Markets utilizing these designs include high performance ASIC, high frequency/RF, and mid I/O products. The migration of flip chip use into these designs can be attributed in part to the improved solder bump thermal fatigue life which has been realized with the use of underfills, as well as to smaller final metal pad/passivation openings being used by IC manufacturers. The need to use flip chips under harsher operating conditions has prompted work to address reliability concerns with several diffusion related failure mechanisms. These concerns have surfaced in response to results of high temperature storage (HTS) and high temperature operating life (HTOL) tests. In HTS tests, UBM (Under Bump Metallurgy) consumption has been observed. In HTOL tests, UBM consumption as well as solder and UBM electromigration have been observed. On flip chips with a bump structure utilizing eutectic 63Sn37Pb over a sputtered thin film Al-NiV-Cu UBM, the HTS and HTOL reliability is a function of the UBM thickness – increasing the UBM thickness can have a positive effect on reliability. However, in general a thin film UBM provides better bump thermal fatigue life, excellent protection to the underlying aluminum, and is less likely to cause silicon cratering or passivation cracking.

A new approach to increasing the UBM thickness and thereby improving flip chip reliability regarding diffusion related failures (while maintaining thin film characteristics), is to use an enhanced eutectic SnPbCu solder bump containing a small amount of Cu in the 1% - 3% range. During bump reflow, the Cu in the enhanced eutectic SnPbCu solder bump has been shown to precipitate out along the UBM/Solder interface, effectively forming a thicker UBM. This effectively thicker UBM has been shown to extend the performance life of the structure in HTS and HTOL testing as compared to 63Sn37Pb while maintaining equal performance in thermal fatigue life as evidenced by thermal cycle (TC) testing. This paper presents data showing the increased reliability performance of the enhanced eutectic SnPbCu bump structure as compared to 63Sn37Pb. Assembly and manufacturing characterization data demonstrating the excellent quality and manufacturability of the SnPbCu bumps is also presented.

The liquidus temperature of SnPbCu alloys increases with increasing Cu %. Increasing Cu % beyond a certain level would necessitate increased process reflow temperatures. Tests indicate that for purposes of wafer bump and circuit board assembly reflows, enhanced eutectic SnPbCu alloys in the range of 1% - 3% Cu can be processed using standard eutectic 63Sn37Pb reflow profiles. Data is presented showing that alloys within this composition range provide significant reliability benefits.

Keywords: Enhanced eutectic SnPbCu, flip chip reliability, UBM consumption, electromigration.

Introduction

The benefits of flip chip packages are well known. Advantages in size, I/O count, electrical performance, reliability, heat dissipation, and cost are driving yearly increases in flip chip use [1, 2]. Earlier reliability issues with solder bump thermal fatigue life due to the thermal mismatch between substrate and chip have been mitigated with the use of underfill [1, 2]. The improvements in thermal fatigue life as well as the shrinking final pad/passivation openings being employed by IC manufacturers has driven flip chip use into more severe operating environments. Under high temperature and high current conditions, several diffusion related failure mechanisms have been seen. Under bump metallurgy (UBM) consumption has been observed in high temperature storage (HTS) testing. In high temperature operating life (HTOL) testing, solder and UBM electromigration have been observed.

UBM consumption is the conversion of the UBM into UBM-Sn intermetallic compounds (IMC's) such as Cu-Sn and Ni-Sn. As the UBM consumption progresses the bump becomes increasingly resistive, eventually resulting in an open bump and electrical failure [3, 4]. Information available in the literature shows that the presence of gold finish on the substrate to which the flip chip is attached can accelerate UBM consumption [4, 5]. Since Ni/Au finishes are widely used on laminate circuit boards a more robust UBM/solder structure not significantly affected by the presence of small amounts of Au is needed for high temperature applications.

Solder and UBM electromigration involve the migration of the solder and UBM metals/IMC's in the direction of electron flow [3, 6]. Both types of electromigration can cause bumps to become resistive or open. It should also be noted that in addition to the electromigration failure mechanisms, UBM consumption can also be a dominant failure mechanism in HTOL testing due to the high temperature regimes used in the test.

Sputtered thin film UBM's such as Al/NiV/Cu provide many advantages over alternative UBM structures such as the plated copper mini bump [7]. These advantages include increased bump thermal fatigue life, excellent corrosion protection for underlying metallization, as well as low residual stress and low thermal strain on the silicon (minimizing silicon cratering concerns) [8]. For high temperature, high current applications, increasing the thickness of the thin film UBM can be beneficial.

A novel approach to increasing the effective thickness of the UBM while maintaining beneficial thin film characteristics has been developed by engineers at Delphi Corporation (patent application filed) [3]. The method developed involves utilization of a near eutectic SnPbCu solder alloy in the bump formation process. This "enhanced eutectic" SnPbCu solder bump has been shown to significantly improve reliability against diffusion related failure mechanisms. Upon cooling after bump reflow, the excess copper in the enhanced eutectic SnPbCu bump precipitates out along the UBM/solder interface as Cu-Sn IMC's. This additional layer of Cu-Sn IMC's effectively creates a thicker UBM thereby adding the protection against diffusion related failure mechanisms while maintaining thin film UBM characteristics.

In order to maintain eutectic 63Sn37Pb bump and assembly reflow parameters the copper concentration in the SnPbCu alloy must be maintained below the SnPbCu ternary eutectic composition. The enhanced eutectic SnPbCu alloy is formulated in such a way that the bump and assembly reflow temperatures/parameters typically used for eutectic 63Sn37Pb can also be used for the enhanced eutectic SnPbCu.

This paper details use of the enhanced eutectic SnPbCu alloy with thin film Al/NiV/Cu UBM. Reliability, quality, and assembly of the enhanced eutectic bumps are discussed.

Reliability

Descriptions of the test die used in the various reliability tests are shown in Table 1.

Table 1 - Reliability Test Die Specifications

Die Type	Die Dimensions (mil)	UBM Cap Diameter (um)	# Bumps/Die	Bump Pitch (um)	Bump Layout	Notes
FA10	200 x 200	102	317	254	Full Array	Used in HTS and HAST test
PB10 – 2a	200 x 200	152	64	254	Peripheral	Used in TC Test I, II
PB10 – 4a	400 x 400	152	128	254	Peripheral	Used in TC Test III
PB10 - 2	200 x 200	120	64	254	Peripheral	Used in TC Test IV
PB10 - 4	400 x 400	120	128	254	Peripheral	Used in TC Test IV
PB08 - 2	200 x 200	102	88	200	Peripheral	Used in TC Test IV
PB08 - 4	400 x 400	102	176	200	Peripheral	Used in TC Test IV
PST2	100 x 100	152	32	460	Peripheral	Used in HTS and HTOL test

Thermal Fatigue Testing

Thermal cycle tests were performed to compare the thermal fatigue life of enhanced SnPbCu solder bumps to eutectic SnPb solder bumps. For Tests I and II, the test vehicle was PB10-2 die on rigid ceramic substrate with no underfill. Two types of ceramic substrates were used, bare alumina (Type A) and dielectric over alumina (Type B). Eutectic SnPb and enhanced eutectic SnPb1.0Cu solder bumps were tested. Two test conditions were used, namely –40 ºC/+125 ºC (15 minute ramp and dwell) for Test I, and –50 ºC/+150 ºC (20 minute ramp and dwell) for Test II. The relative thermal fatigue life of the eutectic SnPb bump on bare ceramic substrate was normalized to 1.0 for ease of comparison. Results of the tests are shown in Tables 2 and 3, and Figures 1 and 2 below. Based on Weibull analysis using a 95% confidence bound, there is no statistical difference between the thermal fatigue lives of the four cells under either test condition. The 1% copper addition to eutectic SnPb solder therefore, does not have any measurable impact on the flip chip thermal fatigue reliability.

Table 2 - TC Test I Results (–40°C/+125°C, 60 min cycle)

Alloy	Substrate	Weibull Life (cycles)	Relative Reliability
63Sn37Pb	Type A	1561	1.00
63Sn37Pb	Type B	1559	1.00
SnPb1.0Cu	Type A	1421	0.91
SnPb1.0Cu	Type B	1616	1.04

Table 3 - TC Test II Results (–50°C/+150°C, 80 min cycle)

Alloy	Substrate	Weibull Life (cycles)	Relative Reliability
63Sn37Pb	Type A	1511	1.00
63Sn37Pb	Type B	1446	0.96
SnPb1.0Cu	Type A	1407	0.93
SnPb1.0Cu	Type B	1447	0.96

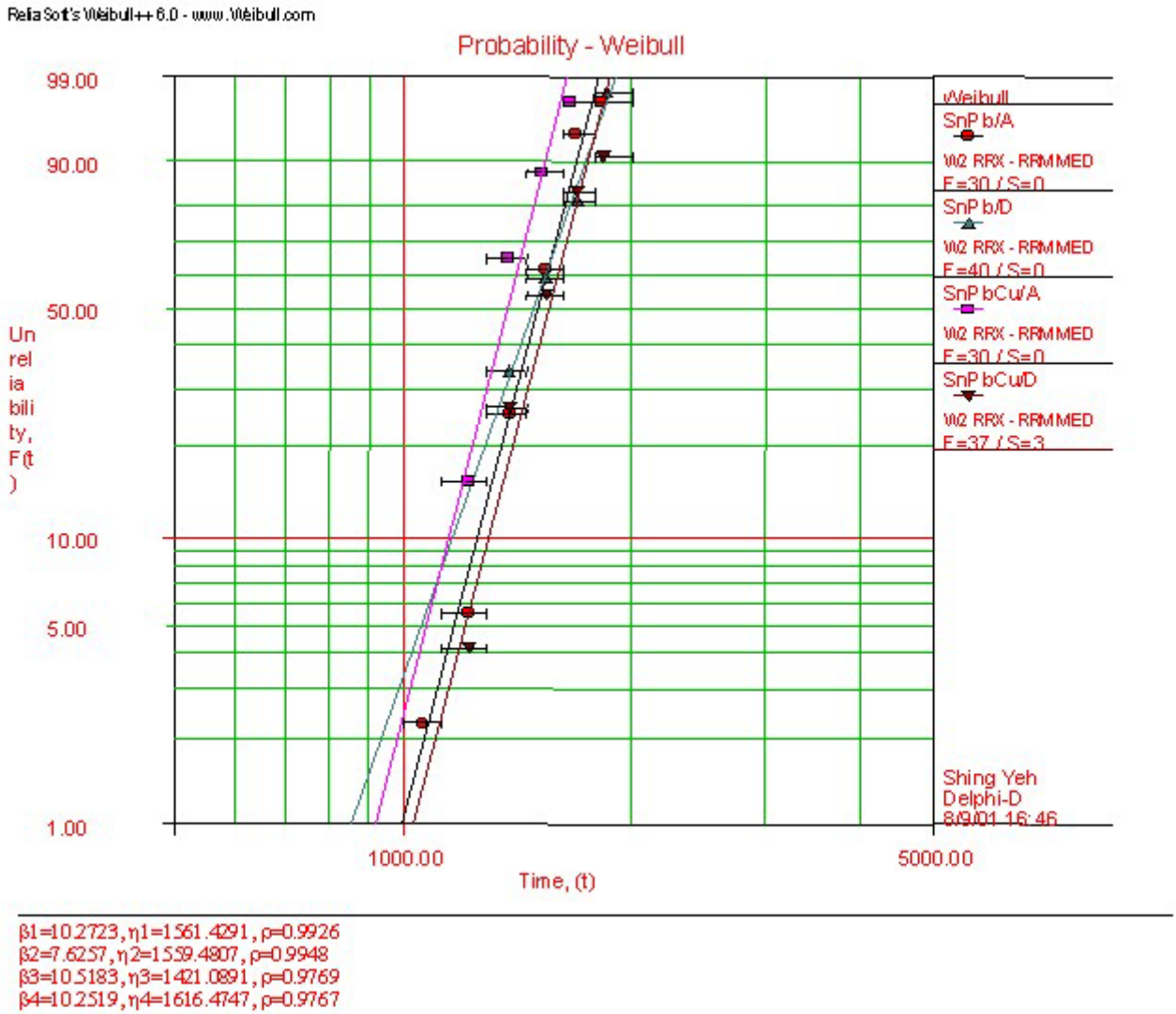

Figure 1 - Weibull Chart for –40°C/+125°C TC Test I

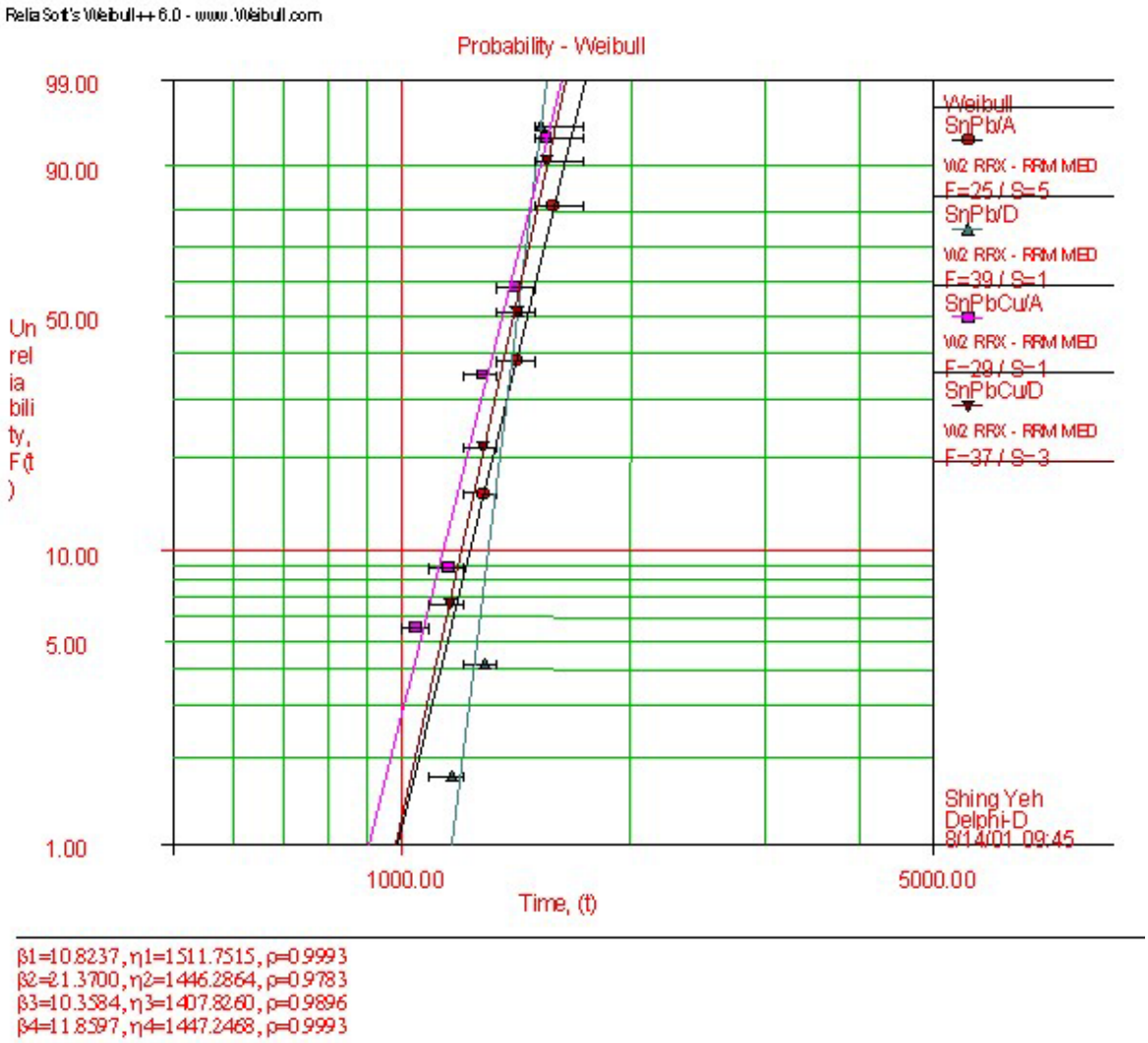

Figure 2 - Weibull Chart for –50°C/+150°C TC Test II

For TC test III the test vehicle was PB10-4a die assembled to 62 mil thick laminate boards with electroless Ni/immersion Au or immersion Ag finish. Eutectic SnPb as well as three different SnPbCu bump alloys were tested. The failure criteria for this test was a 200 milli-ohm increase in circuit resistance from the initial time zero reading. Table 4 summarizes the results of the test. As can be seen, all eutectic and enhanced eutectic cells passed 2000 cycles of testing.

For TC test IV various test vehicles were used. This test made use of 31 mil thick laminate boards with electroless Ni/immersion Au or immersion Ag finish. Each board had die sites for PB08-2, PB08-4, PB10-2, and PB10-4 die. In this test each die type was tested with standard eutectic SnPb as well as the three SnPbCu alloys. The failure criteria for this test was a 200 milli-ohm increase in circuit resistance from the initial time zero reading. Table 5 summarizes the results of the test. As can be seen, all enhanced eutectic SnPbCu cells performed equally to the eutectic SnPb cells, with all cells passing 1000 cycles of testing.

Table 4 - TC Test III Results (-50 °C/+150 °C, 80 min cycle)

Board Finish	Bump Alloy	2000 cycles - Fails/SS
Ni/Au	63Sn37Pb	0/40
	SnPb.92Cu	0/40
	SnPb1.41Cu	0/40
	SnPb2.75Cu	0/40
Ag	63Sn37Pb	0/40
	SnPb.92Cu	0/40
	SnPb1.41Cu	0/40
	SnPb2.75Cu	0/40

Table 5 – TC Test IV Results (-40 °/+150 °c, 80 min cycle)

		1000 cycles – Fails/SS			
Board Finish	**Alloy**	**PB08-2**	**PB08-4**	**PB10-2**	**PB10-4**
Ni/Au	63Sn37Pb	0/20	0/20	0/20	0/20
	SnPb.92Cu	0/20	0/20	0/20	0/20
	SnPb1.41Cu	0/19	0/20	0/20	0/20
	SnPb2.75Cu	0/20	0/20	0/20	0/20
Ag	63Sn37Pb	0/19	0/20	0/20	0/20
	SnPb.92Cu	0/19	0/20	0/20	0/20
	SnPb1.41Cu	0/20	0/20	0/20	0/20
	SnPb2.75Cu	0/20	0/20	0/20	0/20

High Temperature Storage Testing

High temperature storage testing was performed to determine the impact of bump alloy composition on UBM stability at elevated temperatures. Non-underfilled PST-2 test die on laminate boards with Ni/Au finish were used as the test vehicles. Global Au finish was used in order to introduce a large amount of gold into the solder joint to accelerate the failure mechanism. Test conditions were 150 ºC steady aging. Eutectic SnPb and enhanced eutectic SnPb1.0Cu bumps were tested. The same Al/NiV/Cu thin film UBM was used for both solder bump alloys. Read points for the test were every 250 hours for the first 2000 hours of test and every 500 hours thereafter. The failure criterion for this test was a 200 milli-ohm increase in resistance from the time zero reading for a given bump pair. In addition to the electrical test at each end point, test die were sheared off their substrates and the bump fracture surfaces inspected with SEM to determine the fracture mode. Figures 3 and 4 illustrate the results of this inspection. As can be seen, after 1500 hours of test the eutectic SnPb cells (Figure 3) show complete UBM consumption. Figure 4 shows that at 2000 hours the UBM from the SnPb1.0Cu bumps is still intact, and although UBM consumption damage has occurred by 4000 hours, the die still tested good electrically. The visual evidence showing the improved performance with SnPbCu solder bumps is clear from these images. In electrical testing, all eutectic SnPb cells passed 1000 hours but all had failed by 1500 hours. All enhanced eutectic SnPb1.0 Cu cells still tested good at 4000 hours. These results show that the addition of a small amount of Cu to the SnPb solder has effectively slowed down the UBM consumption failure mechanism.

Additional 150 ºC HTS testing with enhanced eutectic SnPb2.25Cu solder bumps is ongoing using FA10 die on 31 mil thick laminate boards with electroless Ni/immersion Au finish. The same Al/NiV/Cu thin film UBM that was used in the initial testing is being used in this test. Failure criteria for the test is a 20% increase in resistance over the initial time zero readings. Results of this ongoing test are shown in Table 6. As can be seen, at 4250 hours the enhanced eutectic SnPbCu assemblies showed zero failures.

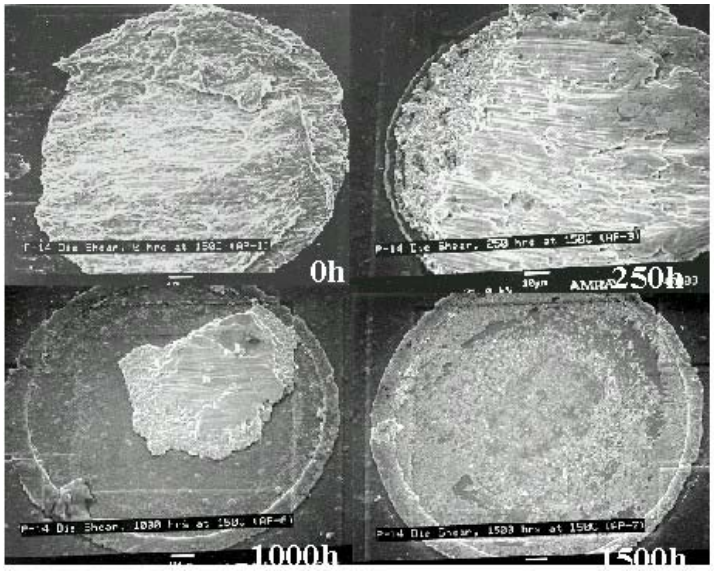

Figure 3 - Die Shear Test showing the Fracture Surface of Eutectic SnPb Bumps through 1500 Hours of 150 °C HTS Test

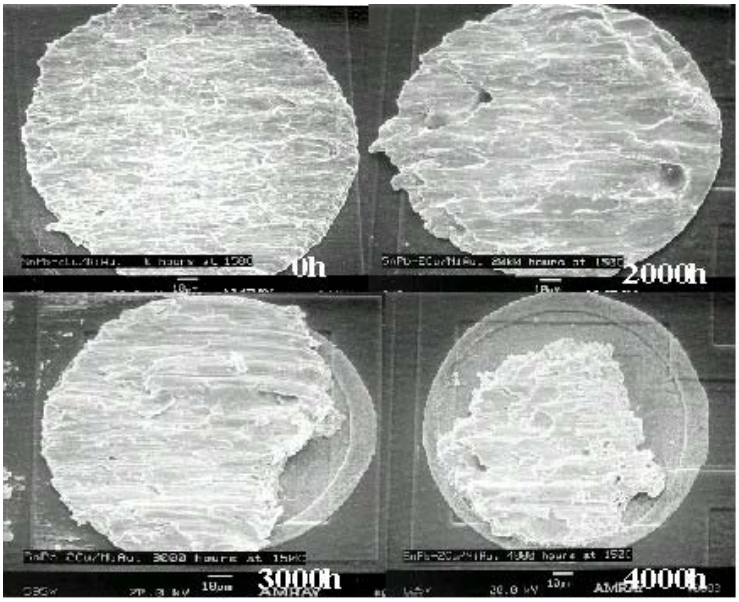

Figure 4 - Die Shear Test showing Fracture Surface of Enhanced Eutectic SnPb1.0Cu Bumps through 4000 Hours of 150 ºC HTS Test

Table 6 - HTS Test Results Summary (150 °C)

	4250 hours*
Alloy	Fails/SS
SnPb2.25Cu	0/89

*Test is ongoing

High Temperature Operating Life Tests

HTOL testing was performed to determine the electromigration resistance of the bump alloys. In HTOL Test I, eutectic SnPb and enhanced eutectic SnPb1.0Cu bumps were tested. Al/NiV/Cu thin film UBM was used. Underfilled PST-2 test die on laminate boards with Ni/Au finish were used as the test vehicles. The test conditions were 600 mA bump current, 145°C ambient temperature, and 150°C to 155°C bump temperature. The bump pad passivation openings on the PST-2 die were 127 μm in diameter. With this size opening the current density was approximately 4700 A/cm^2. In Test I, the 600 mA bump current was used as an accelerated test to determine the relative reliability of eutectic SnPb vs. enhanced eutectic SnPbCu. The failure criterion for this test was a 200 milli-ohm increase in resistance for a given bump pair. The Test I results are shown in Table 7 and the Weibull chart in Figure 5. As can be seen, for a 600 mA bump current with 150 ºC junction temperature, use of the SnPb1.0Cu bumps has increased flip chip reliability by almost 3X over the eutectic SnPb bumps.

Based on the results of Test I, the reliability of SnPb1.0Cu bumps under various test conditions was estimated based on Black's electromigration model [9, 10] and Weibull statistical analysis. Table 8 shows the prediction results. The reliability is the probability of passing 1000 hours of HTOL testing with 0/77 failures. Time To First Failure (TTFF) is also estimated. A second HTOL test (Test II) using 350 mA bump current, 147 ºC ambient temperature, and 150 ºC to 152 ºC bump temperature was then performed. Using PST-2 die with 127 μm diameter passivation openings, the current density for Test II was approximately 2700 A/cm². Results of Test II are shown in Table 9. As can be seen, the SnPb1.0Cu bumps successfully passed 1000 hours of 350 mA/150 ºC HTOL testing as predicted.

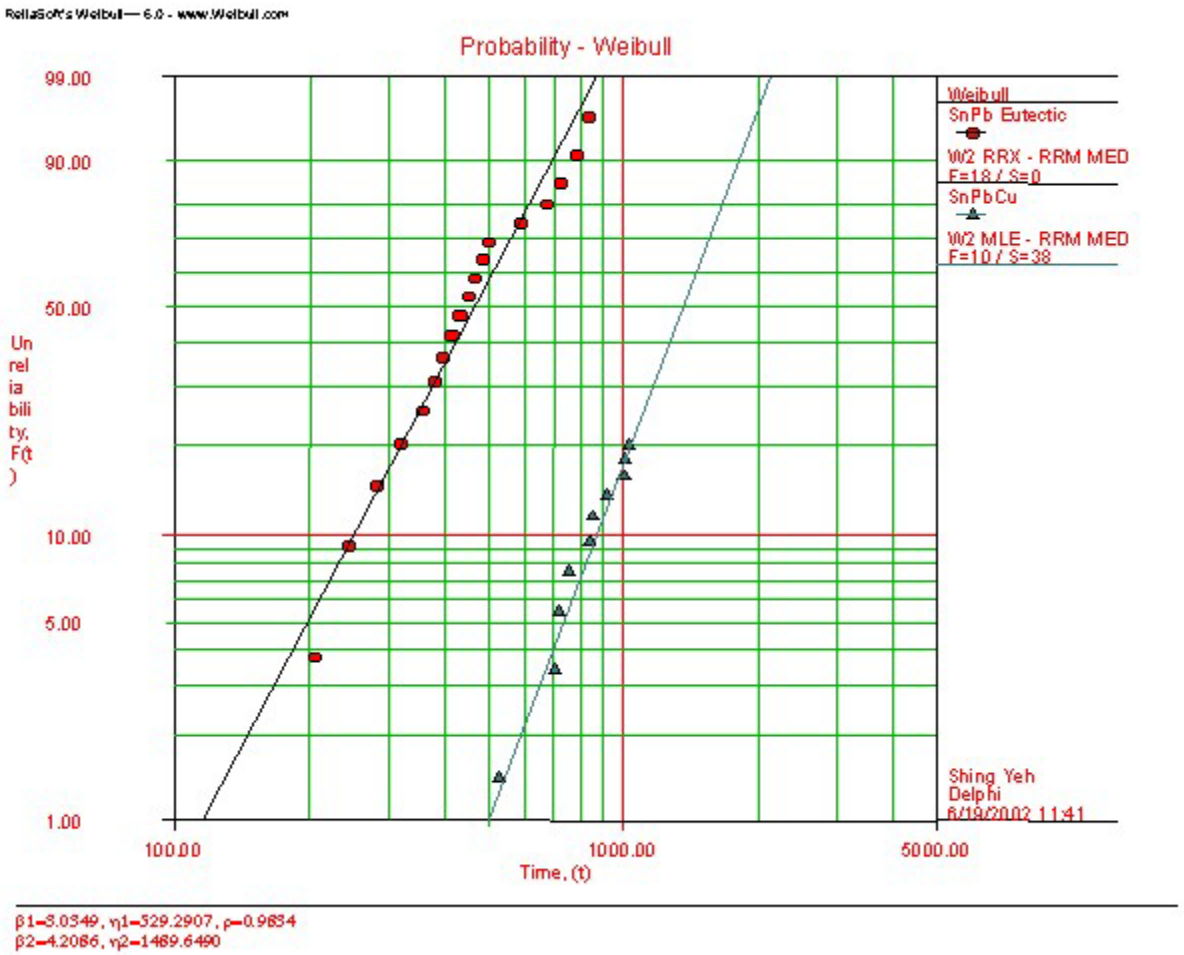

Figure 5 – Weibull Chart for 600 mA HTOL I Test - Eutectic SnPb vs. Enhanced Eutectic SnPbnCu

Table 7 - HTOL Test I Results (600 mA/150 ºC)

Alloy	Weibull Life	Relative Reliability
63Sn37Pb	529 hours	1.0
SnPb1.0Cu	1490 hours	2.8

Table 8 - Reliability Prediction For SnPb1.0Cu Bumps in 150 ºC HTOL Tests

	600mA	350mA	300mA
Weibull Life (hrs)	1490	3930	5190
Weibull Slope	4.2	4.2	4.2
Reliability	0.0%	78.2%	92.6%
TTFF	485	1281	1692

Table 9 - HTOL Test II Results (350 mA/150 ºC)

	1000 hrs	1500 hrs
Alloy	Fails/SS	
SnPb1.0Cu	0/48	1/48

Additional HTOL testing (Test III) was performed with bumps having a higher Cu %. In this test, enhanced eutectic SnPb2.25Cu solder bumps were used. The test vehicle again was the PST-2 assembly, with the same board and UBM specifications as were previously used. Test conditions were the same as for Test II. Results for Test III are shown in Table 10. As can be seen, the SnPb2.25Cu assemblies passed 1688 hours of testing.

Table 10 - HTOL Test III Results (350mA/150 ºC)

	672 hr	840 hr	1008 hr	1176 hr	1344 hr	1512 hr	1688 hr	1848 hr	2016 hr
Alloy	Fails/SS								
63Sn37Pb	1/85	13/85	34/85	47/85	51/85	78/85	-	-	-
SnPb2.25Cu	0/85	0/85	0/85	0/85	0/85	0/85	0/85	2/85	3/85

Highly Accelerated Temperature and Humidity Stress Test

The test vehicle for HAST testing was FA10 die assembled to 31 mil thick laminate boards with electroless Ni/Immersion Au finish. The failure criteria for this test was a 20% increase in resistance from the initial time zero reading. The test results are summarized in Table 11 below. As can be seen, both alloys in the test have passed the required 288 hours.

Table 11 - HAST Test Results (110 °C, 85% RH)

Alloy	288 hrs – Fails/SS
63Sn37Pb	0/90
SnPb2.25Cu	0/85

Multiple Reflow Study

The purpose of this study was to evaluate and compare the bump characteristics (i.e. bump height, bump shear, and IMC thickness) of eutectic SnPb and enhanced eutectic SnPbCu solder bumps after standard and multiple reflows. The test vehicles for this study were SAT wafers with a staggered array design, 160 micron bump pitch and 80 micron bump height target. A peak reflow temperature of approximately 220 ºC was used. Wafers with eutectic SnPb and enhanced eutectic SnPb2.0Cu solder bumps were processed through 0, 3, 6, and 9 additional reflows. Figure 6 and 7 are summaries of the bump height and bump shear data. Each data point on the graphs is an average and represents 25 measurements taken from across the wafer. All measurements for both eutectic SnPb and enhanced eutectic SnPbCu were found to be in specification for both bump height (80 +/- 15 μm) and bump shear (25 gram minimum). As can be seen in Figure 6, the enhanced eutectic solder bumps show bump height behavior similar to the eutectic SnPb under multiple reflow conditions. Figure 7 shows that the enhanced eutectic solder bumps show bump shear behavior similar to the eutectic SnPb bumps under multiple reflow conditions, although the enhanced eutectic solder bumps consistently show slightly higher bump shear values than the eutectic SnPb solder bumps. Visual inspection of the bump shear fracture surfaces for both types of solder showed that all shears were ductile and through the solder.

Both eutectic SnPb and enhanced eutectic SnPbCu have some level of copper enrichment in the solder layer adjacent to the UBM as a result of Cu UBM diffusion into the solder at bump reflow (Cu-Sn IMC's). SEM cross section studies and analysis of the UBM/solder interface region show that the enhanced eutectic bumps have a UBM/Cu enriched IMC layer that is thicker than the corresponding layer on the eutectic SnPb bumps. This difference can be attributed to the Cu in the enhanced eutectic solder alloy that precipitates out along the UBM interface during cooling after reflow. The additional Cu from the solder alloy acts to increase the functional UBM thickness. It is this increased effective UBM thickness that is the main contributor to the reliability performance increases in HTS and HTOL testing for enhanced eutectic bumps. Figure 8 illustrates the difference in effective UBM thickness between the two alloys after standard bump reflow. Figure 9 illustrates the difference in the two alloys at 9X additional reflows. Figure 9 shows that with enhanced eutectic bumps the Cu enriched layer remains continuous along the UBM/solder interface whereas in the case of eutectic SnPb bumps the corresponding layer is notably depleted.

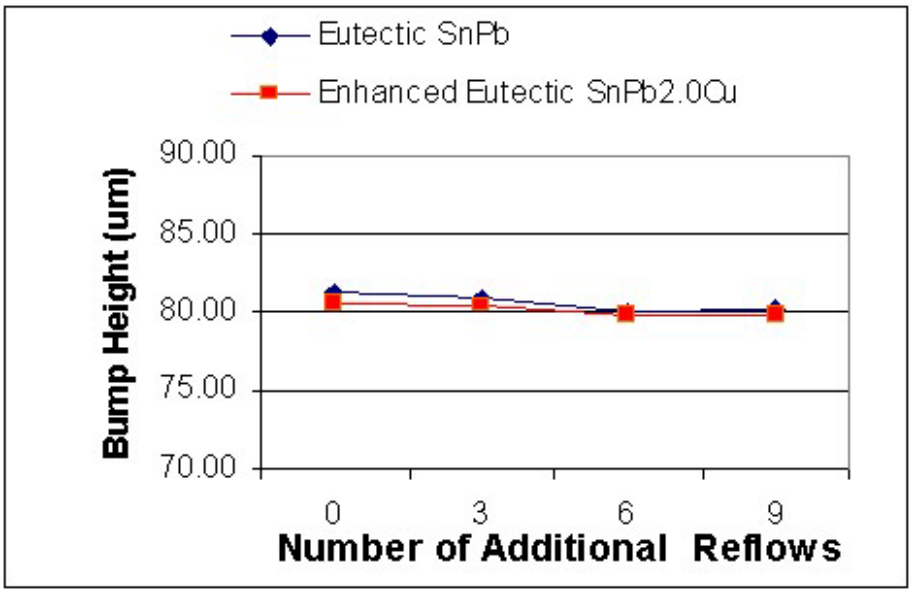

Figure 6 - Bump Height vs. Number of Reflows.

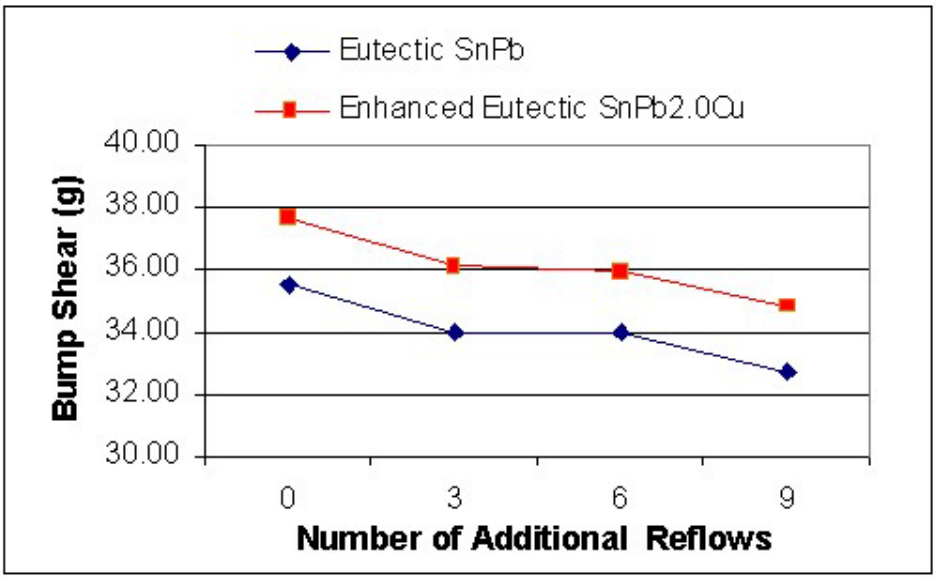

Figure 7 - Bump Shear vs. Number of Reflows.

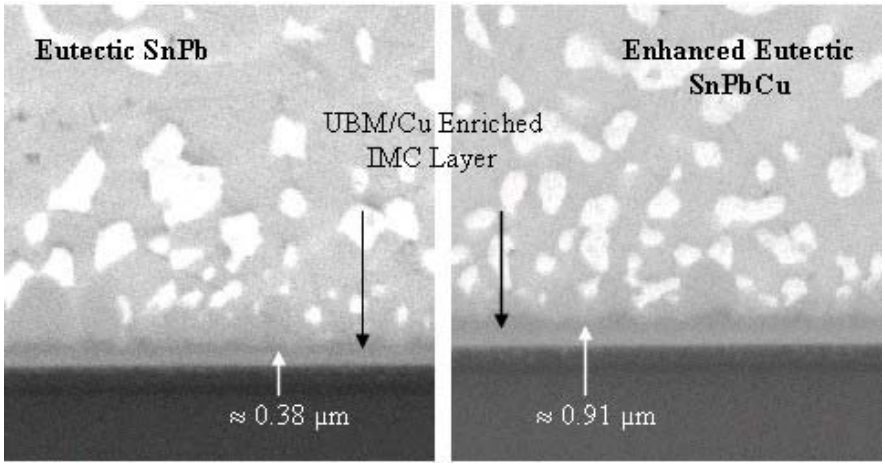

Figure 8 - Cross Section of Eutectic SnPb and Enhanced Eutectic SnPbCu Solder Bumps after 0X Additional Reflows

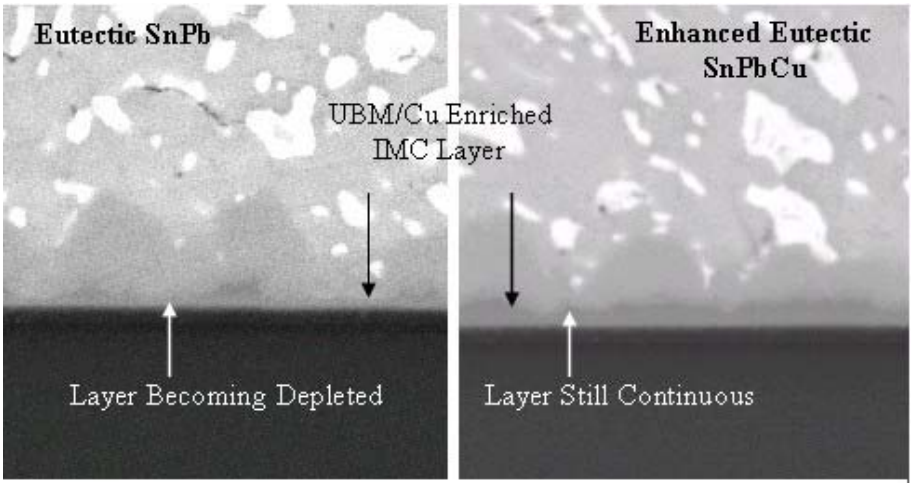

Figure 9 - Cross Section of Eutectic SnPb and Enhanced Eutectic SnPbCu Solder Bumps after 9X Additional Reflows

Bump Quality

Multiple DOE's and process characterizations using enhanced eutectic SnPbCu solder have been completed. These studies have shown that enhanced eutectic solder bumps are equal to eutectic solder bumps in regards to manufacturability and bump quality (bump shear, bump height, yield, voids, appearance). Table 12 lists various wafer bump designs and enhanced eutectic alloys that were tested. All wafers in Table 12 were processed at bump reflow using peak reflow temperatures typical of eutectic SnPb solder (215º C – 225º C). The wafers in Table 12 were analyzed and shown to meet all bump quality specifications including bump shear, bump height, voids, yield, and visual appearance. Representative shear data from enhanced eutectic SnPbCu bumps is shown in Figure 10. Typical bump shear mode representative of enhanced eutectic solder bumps is shown in Figure 11. The shear is ductile and through the bulk of the solder. Data representative of bump height and bump height coplanarity on enhanced eutectic solder bumps is shown in Figures 12 and 13.

Table 12 - Wafer Designs/Enhanced Eutectic Alloys Used in Bump Characterization and Manufacturing Studies

Design	Array	Alloy	Cap/Pitch (μm)	# of Bumps per Die	# of Wafers
PB10	peripheral	SnPb1.5Cu	120 / 254	64	2
FA10	Full	SnPb2.0Cu	102 / 254	317	5
PST2	Peripheral	SnPb2.0Cu	152 / 460	32	1
FAL	Full	SnPb2.0Cu	102 / 254	3135	29
SAT	Staggered	SnPb2.0Cu	77 / 160	851	9
FAL	Full	SnPb2.5Cu	102 / 254	3135	12
FA10	Full	SnPb2.5Cu	102 / 254	317	1
PB10	peripheral	SnPb2.75Cu	120 / 254	64	4
FAL	Full	SnPb3.0Cu	102 / 254	3135	2

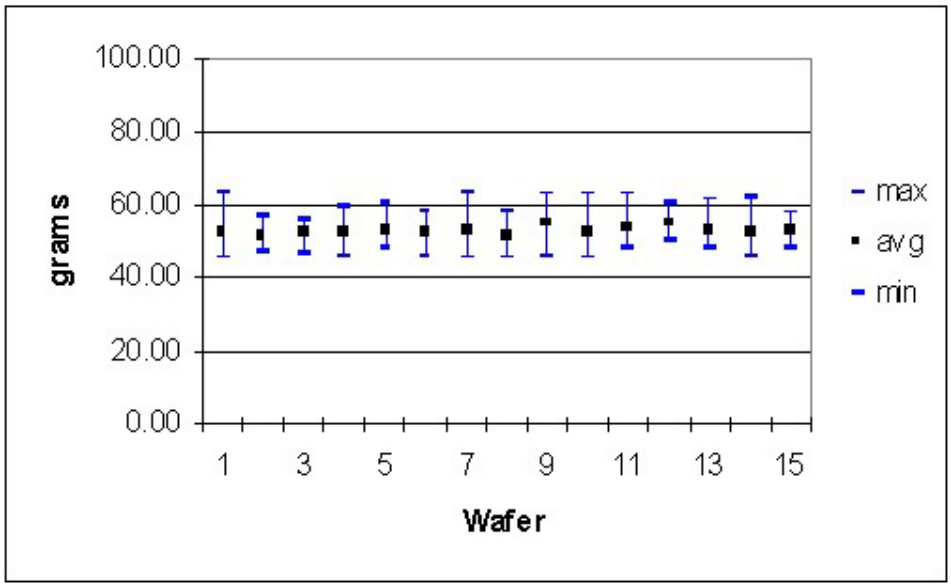

Figure 10 - Wafer Bump Shear Data, Enhanced Eutectic SnPb2.0Cu Bumps, FAL Wafers

Each Data Point is avg of 25 shears. Specification is 25 gram minimum shear.

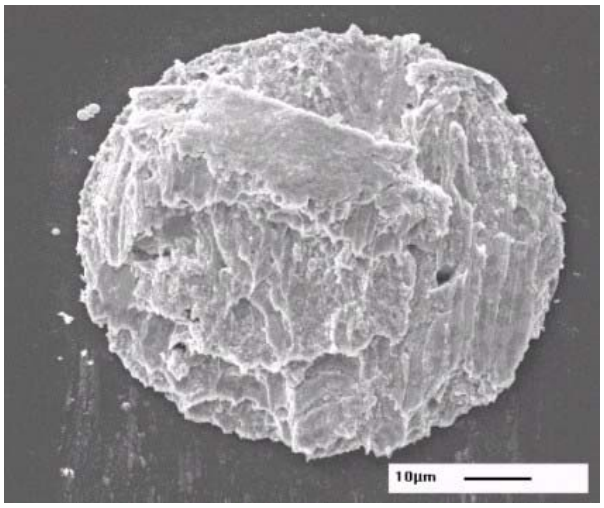

Figure 11 - Bump Shear Surface of Enhanced Eutectic SnPb2.5Cu Solder Bump

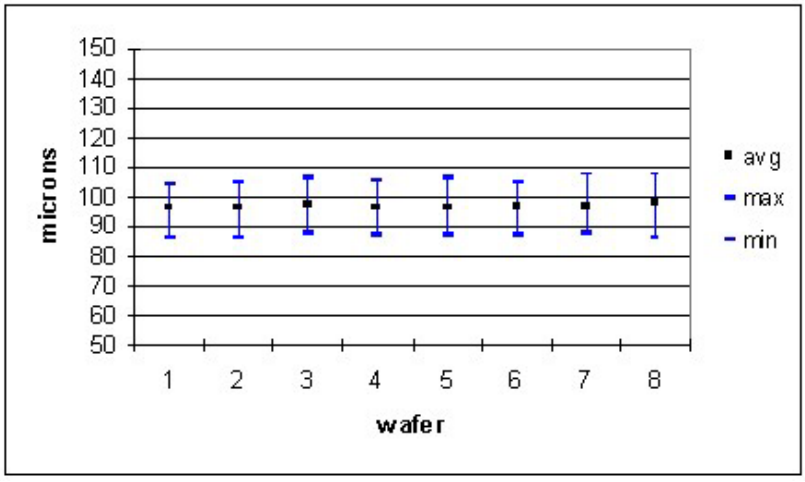

Figure 12 - Wafer Bump Height Data, Enhanced Eutectic SnPb2.5Cu Bumps, FAL Wafers

Each avg, min, max are from 15,675 bumps per wafer. All specifications were met.

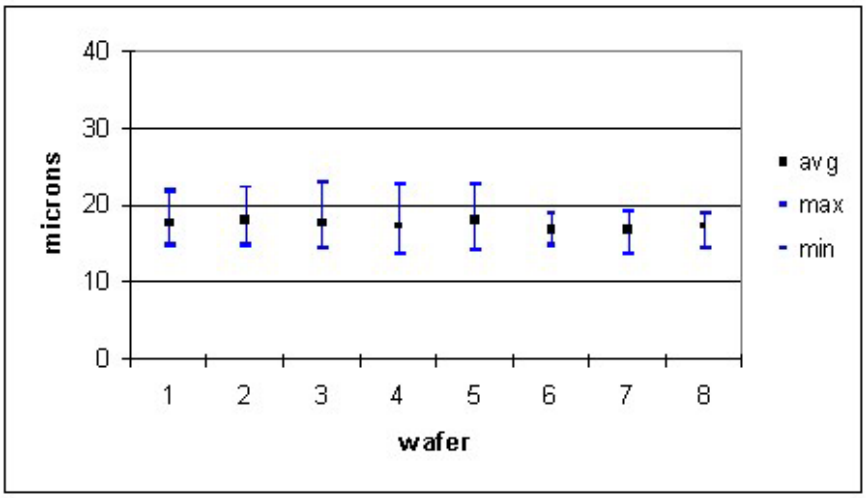

Figure 13 - Wafer Bump Height Coplanarity, Enhanced Eutectic SnPb2.5Cu Bumps, FAL Wafers

Each avg is per wafer from a total of 15,675 bumps. Min/max are die level data and are min/max die coplanarity from 5 die per wafer. All specifications were met.

Assembly

Flip chip assembly of enhanced eutectic SnPbCu bumped die to laminate circuit boards has been completed at three separate assembly locations. Various wafer/substrate designs have been used. Table 13 summarizes the assembly results. In each assembly run, eutectic SnPb bumped die were also assembled for comparison. At each assembly location, the same reflow profile was used for both the eutectic SnPb and enhanced eutectic SnPb assemblies. All assembly runs were processed using peak reflow temperatures typical of eutectic SnPb solder (215º C – 225º C) with excellent yield results.

Table 13 - Enhanced Eutectic Solder - Bumped Die Assembly Results.

Assembly Location	Design	Board Finish	Solder Alloy	# Boards	# Dice	Assembly Yield
1	PB10	Ni/Au	SnPb	6	60	100%
	PB10	Ni/Au	SnPb1.0Cu	6	60	100%
	PB10	Ni/Au	SnPb2.0Cu	12	113	100%
	PB10	Ni/Au	SnPb3.0Cu	6	60	100%
	PB10	Ag	SnPb	6	60	100%
	PB10	Ag	SnPb1.0Cu	6	60	100%
	PB10	Ag	SnPb2.0Cu	6	60	100%
	PB10	Ag	SnPb3.0Cu	6	60	100%
2	FA10	Ni/Au	SnPb	4	40	*95%
	FA10	Ni/Au	SnPB2.0Cu	4	38	*97%
	PST2	Ni/Au	SnPb	16	96	*97%
	PST2	Ni/Au	SnPb2.0Cu	16	96	*96%
3	FA10	Ni/Au	SnPb	7	70	100%
	FA10	Ni/Au	SnPb2.0Cu	19	190	100%
	FA10	Ni/Au	SnPb2.5Cu	9	90	100%

* Yield fallout not related to alloy type.

Conclusions

The results of reliability studies with enhanced eutectic SnPbCu solder have shown that the inclusion of a small amount of Cu in the 1% - 3% range into eutectic SnPb solder significantly inhibits diffusion related failure mechanisms. The new solder alloy(s) have been designated as “enhanced eutectic” due to their near eutectic SnPb composition and eutectic SnPb like behavior at bump and assembly reflow.

1. Enhanced eutectic SnPbCu solder can be used as a drop in replacement for eutectic SnPb regarding bump processing and assembly.
2. Enhanced eutectic SnPbCu solder bumps have shown a nearly 3X increase in HTOL reliability in comparison with eutectic SnPb bumps.
3. Enhanced eutectic SnPbCu solder bumps have shown very significant increases in HTS reliability in comparison with eutectic SnPb bumps.
4. The performance increase of enhanced eutectic SnPbCu solder bumps at HTS and HTOL testing is due to the increased effective UBM thickness attained with the use of the enhanced eutectic SnPbCu solder.

5. With enhanced eutectic SnPbCu, the thicker UBM is formed during the bump reflow process via precipitation of Cu from the alloy, along the UBM/solder interface.
6. Use of the enhanced eutectic SnPbCu alloy effectively increases the UBM thickness while allowing beneficial thin film UBM characteristics to be maintained.
7. Equivalence of enhanced eutectic SnPbCu solder bump thermal fatigue life as compared to eutectic SnPb has been demonstrated through thermal cycle life reliability testing.
8. Equivalence of enhanced eutectic SnPbCu solder bump quality as compared to eutectic SnPb has been demonstrated via data gathered from multiple bumping process and assembly runs.

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