Embedded Passive Technology

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Abstract— Embedded Passive Technology is a viable technology that has been reliably used in the defense and aerospace industry for over 20 years. Embedded Passive (Resistors and Capacitors) Technology have a great potential for high frequency and high density applications. It also provides better signal performance, reduced parasitic and cross talk. This paper summarizes the selection of resistor embedded materials, evaluations of resistive material (Phase 1) and duplication of a complex digital design (Phase 2). Phase 1 –resistive materials (Foil 25Ω/sq NiCr and 1kΩ/sq CrSiO) and resistive-Ply materials (25Ω/sq and 250Ω/sq NiP) were chosen for evaluation.

Phase 2 – Due to the high level of complexity and advance materials dielectric, the Digital Imaging Processor unit was chosen as an evaluation vehicle. Process Evaluation for embedded was used to determine present process gaps for laser trimming, fabrication material, raw board test and defining specifications for DFM and layout design.

Keywords – Embedded Resistors; Embedded capasitor, Materials Dielectric properties, Printed Wire Circuit, CCA Design and evaluation vehicle design.

I. INTRODUCTION

The concept of embedded passives technology (EPT) is to fabricate and bury within the layers of an interconnecting substrate passive components such as resistors and capacitors (R&C) into the substrate of Printed Board (PB) during the fabrication process of the raw board (the substrate is the electrical interconnection between the components, e.g., a printed circuit board – (PCB), [1]. EPT drivers include customers' demand for additional functionality at the same or lower price has driven the electronics industry to miniaturization, better electrical performance, higher packaging density and technologies with potential cost saving. Using the embedded passive technology, passive components (R&C) may be embedded into the substrate directly under active devices such as ASICs. The shorter distance between the embedded passives and active components reduces the parasitic losses associated with surface mounted passive components, resulting in better signal transmission and less cross talk. Lower loss and lower noise yield an improvement in electrical signal performance especially at high frequencies. Passive components account for 80 to 95% of the total number of components and cover over 40% of the surface of the substrate of Printed Board (PB). Reducing the number of surface mount passive components, will increase the PB real estate available and therefore allow for higher packaging densities to be used. There is also a potential in materials cost reduction due to fewer purchased components, manufacturing materials (Flux & Solder), reduction in Defect per Millions Opportunities DPMO, yield improvement, and reduction in production cycle time and time to market as well as reduction in Cost of Poor Quality (COPQ). EPT can simplify the assembly and test processes and reduce the actual cost especially when using 0201 packages or the Lead-Free process. EPT will reduce the overall product cost in comparison with the traditional utilization of Surface Mount technology (SMT) discrete passive components.

The Advanced Manufacturing Engineering (AME) technology group has been involved in the evaluation of embedded passive technology as part of the Game Changers technology roadmap. The game changer of the EPT was defined into three different phases; phase 0 was completed in 2009 to define the type of resistive materials that are available. Phase 1 was completed in 2010 and resistive material types were selected, a test vehicle was designed and fabricated, assembled and tested under the following conditions: ESD, Non-ESD, IST coupon testing, thermal testing at -55°C to 125°C and life cycle and mechanical vibration and displacement test. Phase 2 is in the final phases of completion, where a high complexity Circuit Card Assembly (CCA) was selected using Thermount based material for PB fabrication with 4 layers of EPT (Ticer Resist materials 25Ω and 1kΩ and 3M C-Ply Capacitance) embedded materials, in a 20 layers stackup with multiple impedance control layers.

II. DESIGN AND FUNCTIONALITY

A. Backrground

Customer demands for more increased functionality for Aerospace applications has resulted in high density Printed Board Assembly (PBA) designs that have low yield, high complexity, DFM violations, and significant hidden factory rework during assembly. EPT provides a means to reduce the number of surface mounted components which increases yields, and frees up real estate (figure 1). Although capacitors, resistors and inductors are all candidates for embedding, most current interests are focusing on capacitor and resistors since they represent the majority of passive devices used on a circuit board.

A generic single board is generally composed of 5% integrated circuits (ASICs), 4% connectors, 40% capacitors, 33% resistors and 18% miscellaneous parts [2]. Embedded resistors and capacitors can be individually fabricated, and capacitors can also be manufactured in distributed planar form.

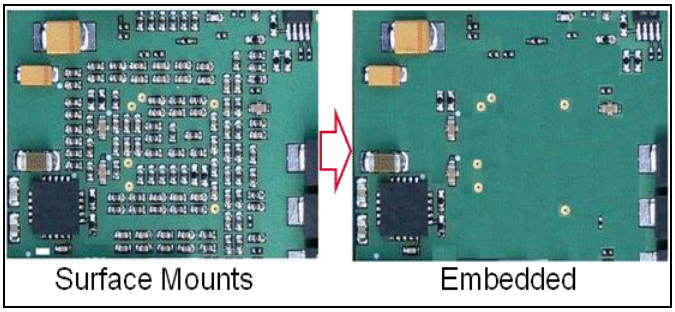

Fig 1 – Surface mounts assembly vs. embedded technology

One concern of the EPT is whether the technology is economically feasible. The advantages of embedded passives technology are the possibility to reduce the assembly costs, negate the cost of purchasing and handling discrete passive components, and reduce the required board size area. However, these advantages must be traded off against the increased cost of board fabrication and the decrease of the throughput and yield of the board fabrication process.

B. Embedded Material tests

The resistive material benchmark TICER thin film resistor foil is thermally and electrically stable after thermal cycles. The life cycle thermal testing was conducted using table 1 parameters for 300 cycles per IPC-6012 class 3 accelerated thermal shock profile. This is the profile used to qualify all Honeywell AERO FR-4 board materials and represents 20 years life reliability of the product.

Table 1 – Thermal profile for accelerated qualification test

Accelerated Thermal Shock Profile	
High Temp (°C)	+125
Low Temp (°C)	-55
Dwell Time (min.)	30
Cycles/Day	48

Rework of BGAs were done on the multiple substrates where BGAs were removed and replaced using SRT Model 1100 repair and rework station under the normal removal and replacement thermal profile. Table 2 defines the thermal parameters for removal and replacement.

Table 2 – Removal and Replacement Thermal Profile

	Top heater	Bottom Heater	Time
Preheat	180C	220C	100 sec.
Reflow	220C	230C	60 sec.

Electro Static Discharge (ESD) testing was conducted using two different lots; one lot with best in class ESD protection and the other without any ESD protection. The ESD test concluded that there is no difference in resistance percentage change between the ESD and Non ESD (figure 2) controlled boards during the assembly.

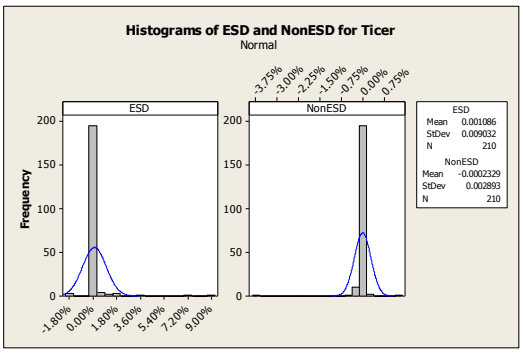

Fig 2 – No difference between ESD & Non ESD

Ticer materials also provide excellent thermal stability. NiCr, Nickel Chromium Aluminum Silicon (NCAS), and Chromium Silicon Monoxide (CrSiO) are well known for their excellent thermal stability under continuous load and thermal excursion. The materials can be subjected to multiple thermal excursions, such as lead free (RoHs) reflow, with minimal resistance change and ensured long term reliability.

C. Material Specifications[3]

TCR integrated thin Film Resistor Foil is supplied in a variety of foil widths and thickness using grade 3 copper foil. The thickness of 18 µm (0.5 oz) and 35 µm (1 oz) are commonly available. Table 3 show materials specialization and recommended etching solutions.

Table 3 – Material specification

TCR Specification Data Set: Resistive Foil Specifications			
Resistive material	NiCr	NCAS	CrSiO
Sheet resistance (Ω/sq)	25, 50, 100	25, 50, 100, 250	1000
Sheet resistivity tolerance (%)	±5	±5	±7
Temperature coefficient of resistance (ppm/°C)	<110	-20	300
Base copper foil thickness (microns)	18, 35	18, 35	18, 35
Width maximum mm (inches)	1295 (51)	1295 (51)	1295 (51)
Maximum recommended power dissipation at 40° C (watts/sq in)	25 Ω/sq: 250 50 Ω/sq: 200 100 Ω/sq: 150 —	25 Ω/sq: 250 50 Ω/sq: 200 100 Ω/sq: 150 250 Ω/sq: 75	1000 Ω/sq: 250
Recommended etching solutions 1st etch 2nd etch 3rd etch	 Cupric chloride Ammoniacal —	 Ammoniacal* Acidic permanganate Ammoniacal*	 Ammoniacal* Alkaline permanganate Ammoniacal*
For base foil properties, please refer to the appropriate product application sheet. ** For NCAS and CrSiO, cupric chloride can be used in place of ammoniacal etchant.*			

D. Fabrication

The fabrication of PB with Embedded Passive Technology (EPT) uses the same processes as the traditional fabrication where embedded resistive materials are used as part of the stack-up structure. Also, the Nickel Chromium (NiCr) resistor alloy reduces fabrication steps by eliminating the needs for a separate resistive layer etch. The NiCr can be etched first in cupric chloride followed by ammoniacal etchant, which is the same etchant used to etch the copper layers of the board. Also the use of double-treat copper can eliminate the need for laminate pre-cleaners and oxide treatments. Traditional final testing is used to determine the board integrity such as continuity, isolation and value measurements.

There are several key processes that must be in control and possibly modified to ensure properly defined resistor patterns. These processes can be properly controlled provided attention is paid to several considerations. Some of the considerations are the equipment setup for the photoresist application and subsequent exposure and development and proper process control for selective copper removal to define resistor length which can impact the value and tolerance.

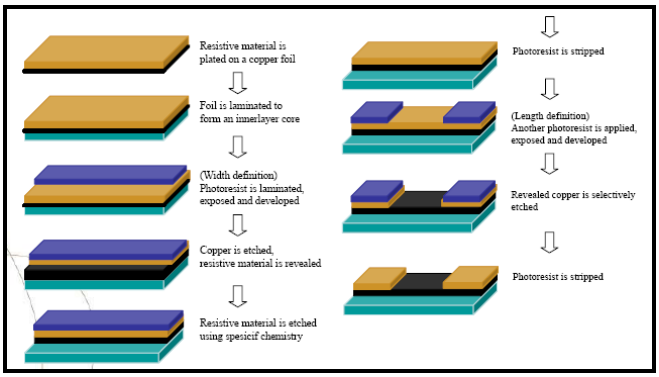

Fig 2 – Illustration of EPT fabrication process

E. Design

The design for the EPT components shape is determined based on final resistor required value and embedded resistance material value. The thin film embedded resistor is isotropic therefore the resistor patterns can be designed in any orientation required by the I/O or to optimize spacing. The basic equation for calculating resistance is:

Equation 1:
$R = s(L/W)$

R = resistance in ohms
s = sheet resistance in ohms/square
L = length of resistor
W = width of resistor
Note: the term "square" is dimensionless

The final resistance tolerance is a function of the etch precision of the copper etch processes of the PB fabricator and resistivity variation of embedded film. To minimize the impact of etching on resistor tolerance, it is recommended to use a fixed resistor width but adjust the resistor length to achieve the correct resistor value.

Another technique to improve resistor tolerance is to use larger dimensions since the line-width variation is the copper etch process is typically fixed and therefore independent of line-width. Designing with resistor widths and lengths greater

than 0.25 mm (0.010") is recommended. Consult the resistor calculator model for determining recommended sizes based on tolerance and power dissipation. This calculator [4] can be found on Honeywell Advance manufacturing Engineer (AME) website.

Thermal and mechanical spacing allowances at plated through and microvia holes can be challenging. A minimum of 0.25 mm (0.010") is recommended for copper connection between the hole and the beginning of the resistor pattern. This ensures adequate isolation from the stresses caused by assembly soldering and drilling of holes. Fig 3

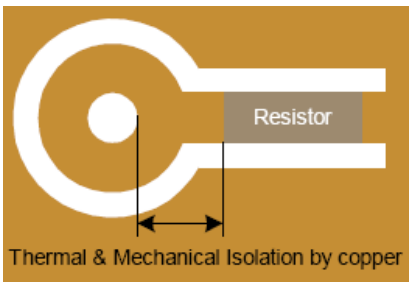

Fig 3 – Resistor in ground plane

Design for power and thermal dissipation is a function of the resistor alloy power rating (mW/mil²) and the resistor area (mil²). When higher power loading is required the resistor must be sized accordingly. The factors that effect thermal dissipation are:

- Circuit configuration
- Circuit thickness and material type
- Thermal conductivity of the dielectric
- Proximity of power or ground planes to resistor
- Ambient temperature
- Additional system cooling or heat sinking
- Resistor size (total resistor area)

All aspects of the system's thermal dissipation must be considered in the PB design. Critical thermal dissipation requirements may require thermal profile modeling or actual prototypes to ensure proper configuration is achieved.

F. Design – resistor types

Designing for EPT resistor types can be determined based on the resistor value and electrical functionality. There are two type of resistors that can be used in embedded; resistors in very basic circuits such as pull-up and pull down and precision resistors.

Pull-up and pull-down resistors are used in electronic logic circuits to ensure that inputs to logic systems settle at expected logic levels. Figure 6 shows a simple EPT design for pull-up and pull-down resistors. The typical value for pull-up/down resistors can vary in value; it ranges from 500Ω to 10kΩ depending on the circuit logic. The typical tolerance of these resistor types can be up to 20%.

EPT precision resistors are characterized by a resistance value with a low tolerance such as 1%. To achieve the required precision tolerance of 1%, laser trimming method is applied.

G. Laser trimming

Designing rules for the laser trimming [5] process requires that circuits be square or rectangular and must consist of straight lines, arcs, or combination thereof. The resistor "length" is always the dimension of the resistor in parallel to the current flow. And the resistor "square" in the corner area(s) of a bent style resistor such as "L" shape or serpentine design should be counted as one-half the value of the sheet resistance. Figure 4

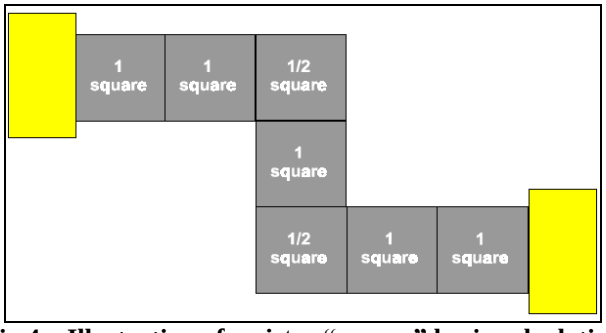

Fig 4 – Illustration of resistor "square" basic calculation

This can be demonstrated in the following equation:

Equation 2:

R = S*(Sum (Square)+Sum(Corner)/2)

R = resistance in ohms
S = sheet resistance in ohms/square
Square = number of squares
Corner = number of right corners

Based on design complexity, precision embedded resistors can be used and laser trimming is utilized. Laser trimming can achieve a tolerance of 1% utilizing several trimming methods such as plunge, double plunge, L-cut, serpentine and scan. Shown in Figure 5 and advantages and disadvantages of resistor trimming types is demonstrated in table 3

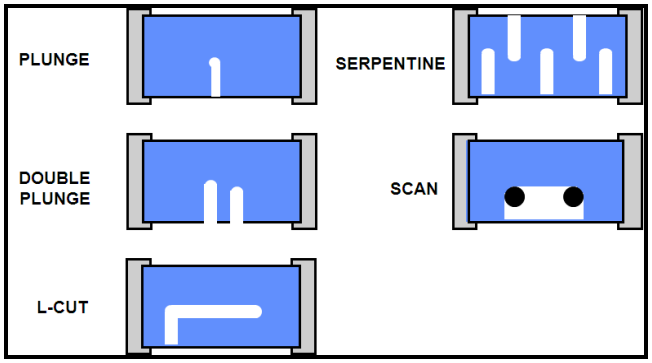

Fig 5 – Illustration of laser trimming type

Table 3 – Resistor trim types advantages and disadvantages

Resistor trim type	Recommended Application	Advantages	Disadvantages
Plunge	DC	Minimum Cost	Limited to DC only application tolerance capability
L Cut	DC	Increased accuracy lower tolerances	DC only application Slightly higher cost than plunge cut
Serpentine cut	DC – High value resistors	Increased accuracy lower tolerances. Wider final value flexibility	DC only application higher cost than plunge or L cut (depends on quantity of cuts required)
Scan Cut	All	High frequency applications. Excellent tolerance accuracy	Highest cost

Designing for laser trimming can be challenging and requires design for manufacturing and test (DFM&T). Configuration for resistor types can be designed in variety of shapes. The resistor shape will determine the method of trimming. The resistor types are:

Rectangular configuration – this is the most common type of resistor. Figure 6

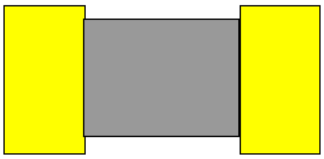

Fig 6 – Rectangular configuration

L-Bent configuration – This resistor "square" in the corner area of a bent style resistor should be counted as one-half the value of the sheet resistance. See figure 7

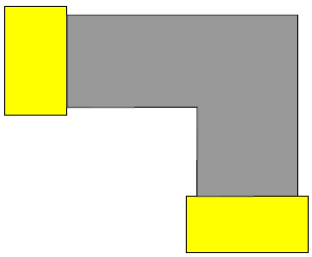

Fig 7 – L-bent configuration

Serpentine configuration – This resistor is typically used for high value resistors. The number of corners complicates calculation of the value. The resistor "square" in corner areas of a serpentine style resistor should be counted as one-half the value of the sheet resistance. See figure 8

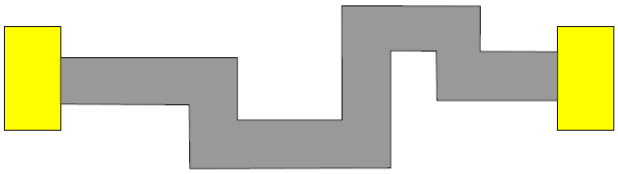

Fig 8 – Serpentine configuration

Top-hat (lobe type) configuration – The advantage of the top hat design is its wide trim range. Figure 9 shows a five square resistor. By trimming a single plunge cut of the laser, a nine square resistor can be created. The resistance can be manipulated between these values by limiting the amount of trim. Resistor with a trimmable range of more than 3x the initial value can be created using this technique. Resistor of this type must be trimmed regardless of the tolerance requirement. See figure 10

Fig 9 – Top hat configuration

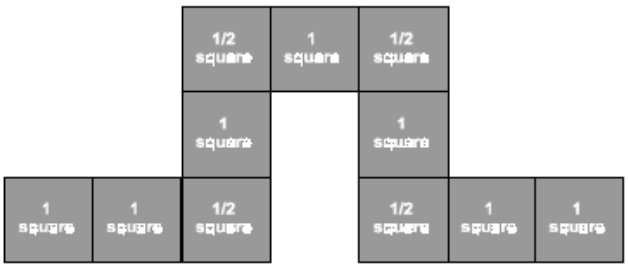

Fig. 10 – Top hat configuration after plunge cut

Tooling and trimming guidelines and requirements – Probe cards are required to measure all resistors as they are laser trimmed. It is best to design a probe card to measure 15 to 20 resistors at a time. Multiple cards would be required for designs which use more timed resistors. This will affect the circuit, tooling and set-up pricing. Resistors with values of 50 ohms or less requires Kelvin-style, 4 point, probing to insure accuracy. The quantity of probe cards can be reduced by utilization of DFM modeling and determining the resistor unique values, shapes, and geometrical positioning.

The laser (YAG) spot is approximately 35-40 µm diameter depending on the subject materials. This can be reduced to ~ 25 µm with new optics. High accuracy trims (tolerance +/- 0.5%) are best obtained for resistors larger than 0.020 x 0.020 in^2 (250 x 250 µm) and are trimmable depending on material and resistance values.

Some design driver areas for precision resistor are:

- Thermal effect during laser trimming
- Electrical current and potential during test and trim
- Thermal coefficient of resistance may significantly reduce throughput performance and final process tolerances
- Power and potential coefficient of resistance may significantly reduce throughput performance and final process tolerances
- CAD data can be used in planning and programming the process before actual parts are available.
- Final resistor tolerance may be affected by after-trim board fabrication processes

III. POWER HANDLING CAPABILITY

The power handling capability of a thin film embedded resistor is a thermal management issue; where the power handling capability is a function of the resistor's size and shape, and the PB construction. It is the relatively low degradation temperature of organics that makes thermal management important.

The steady state heat transfer conduction through board is determined by

Equation 3:

$Q = k\ A1\ (Tr - Ts) / d$

And the steady state heat transfer convection from board by

Equation 4:

$Q = U\ A2\ (Ts - To)$

Q = heat in watts Tr = resistor temperature

K = thermal conductivity A1 = resistor area

A2 = board area U = heat transfer coefficient

Ts = surface temperature at outer layer

To = environmental temperature

To avoid resistor failure:

Tr < Tmp of resistor material (e.g. NiCr ~ 1400°C)

Tr < Tg surrounding organics (e.g. FR4 ~ 170°C)

Tmp = temperature melting point

Tg = glass transition temperature

Power dissipation of thin film resistors – to understand the effect of resistor size on power dissipation [6], experiments have been done on thin film resistors to measure the burnout power and to measure the resistance change of thin film resistors under different power loads. The experiment resulted in the following Equation 5

$Pb = Ib^2\ R / A$

Where,

Pb = burnout power Ib = burnout current

R = resistance A = area of the resistor

The burnout current versus resistor size is plotted in Figure 11. It shows that the thermal dissipation ability of a thin film resistor is dependent on the width and length, and it depends on the size of the resistor. The narrower the width and the shorter the length, the higher the burnout power density will be because of the shorter heat conduction path to the surroundings. As the resistor size increases, the burnout power density drops, although the total power increases because of the larger resistor physical size, indicating that the relationship between the total power dissipation and the thin film resistor size is not linear. It was determined that the resistor should be operated at a power level of no more than 30 to 40% of the burnout power value to keep the resistor temperature low with no significant change in resistance.

The resistance change of thin film resistor under different power loads shows; as power load increased, the temperature of the thin film resistor increased, which in turn caused the resistance to change. The resistance change at different power densities calculated from the current load and the size of the resistor is shown in Figure 12 and Figure 13. Both NiCr and nickel-chromium-aluminum-silicate (NiCrAlSi) resistor materials were evaluated. For Figure 12, the resistance change is due to power load and the resulting temperature change and is a function of material Thermal Coefficient of Resistivity (TCR) this resistance change is reversible upon cooling of the resistor.

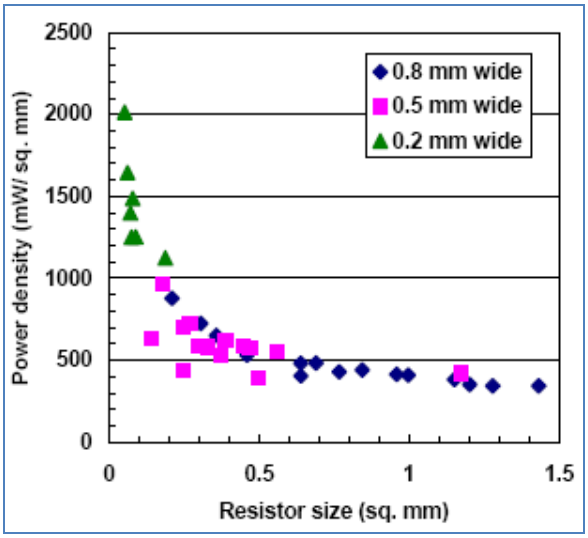

Fig 11- Burnout power of thin film NiCr resistor

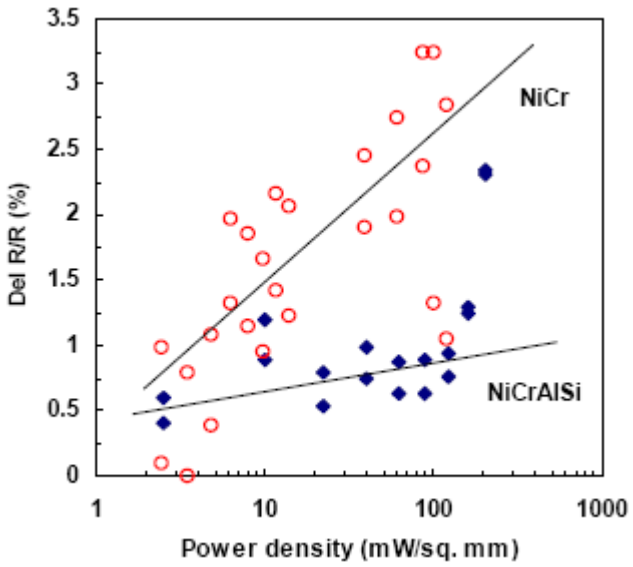

Fig -12 Resistance changes under power load, resistive foil was laminated on single side of FR4 prepreg and the resistor size is 30 mil x 30 mil.

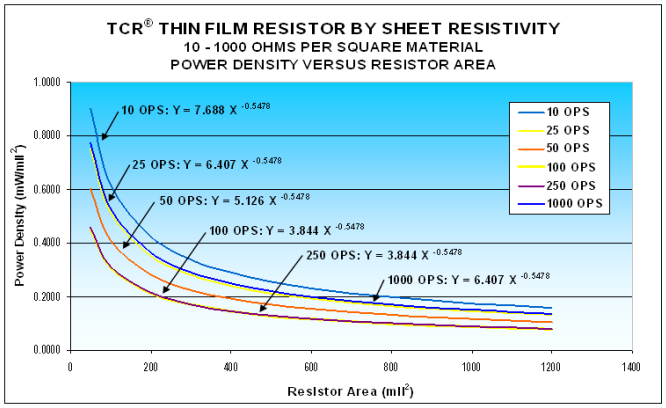

Fig. 13 – Power density vs. Resistor Area

IV. Resistor Area Calculation

The resistor value using embedded thin film resistance is calculated by sheet resistance in ohms/square times the length to width ratio of the film – the "number of squares".

Equation 6

$R = (\rho/t)\,(L/W) = Rs\ Ns$

Where

R = resistance in Ω

Rs = ρ/t = sheet resistance, Ω/square

L and W = length and width of the material strip

Ns = L/W = the number of square

The following is an example utilizing Ticer Resistor Calculator to determine the size of the resistor based on the following parameters:

Problem – Resistor value needed is 100 Ω, Power needed is 200 mW, and using thin film foil of 25Ω/square.

Solution – to achieve the 100Ω value the design requires 4 square of the 25Ω.

Power formula for the 25Ω/sq is defined as

Equation 7

$p\ (\text{mw/mil}^2) = 6.407\ A\ (\text{mil}^2)^{-0.5478}$ From Figure 13

Where

p = power density A = resistor area

Calculating for A

Equation 8

$P = p\,A = 6.407\ A^{-0.5478} = 6.407 A^{1-0.5478} = 6.407\ A^{0.4522}$

$A = (P/6.407)^{-0.4522}$

$A = (200/6.407)^{-0.4522} = 2016.9\ \text{mil}^2$

Calculation of resistor width and length is determined by

Equation 9

$A = w\ (w \times n)$

Where

w = resistor width n = number of the squares

$w = (A / n)^{0.5}$

$w = (2016.9 / 4)^{0.5} = 22.45$ mil

$l = n\ w = 22.45 \times 4 = 89.9$ mil

The Ticer calculator is generated to provide designers with guidelines to determine the size of the resistor based on variables such as resistor value, power dissipation, tolerance, and etch tolerance. It also provides resistor pattern shapes to optimize the footprint of the resistor based on sheet resistivity. This calculator is located on AME website.

V. Summary and Conclusion

The Advanced Manufacturing Engineering (AME) technology group has been involved in the evaluation of embedded passive technology as part of the Game Changers technology. The game changer of the EPT was defined into three different phases; phase 0 was completed in 2009 to define the type of resistive materials that are available. Phase 1 was completed in 2010 and resistive material types were selected, a test vehicle was designed and fabricated, assembled and tested. Phase 2 is in the final phases of completion, where a high complexity Circuit Card Assembly (CCA) was selected using Thermount based material for PB fabrication with 4 layers of EPT.

Embedded Passive Technology is a viable technology that has been reliably used in the defense and aerospace industry for over 20 years. EPT's value is creating space on a crowded PCB where more active components are needed. Embedding resistors and capacitors can increase board functionality without increasing board size. It also provides better signal

performance, reduced parasitic and cross talk. EPT can increase reliability by eliminating surface mount devices and the defects associated with assembly processes such as placement and soldering.

Multiple circuit board fabricators in the US have experience in utilizing embedded passive technology. Design aids including Ticer's Resistor Calculator are available on the AME website.

A. Abbreviations and Acronyms

The following is a list of abbreviation and acronyms that were used in this article.

EPT – Embedded Passive Technology

NiCr – Nickel-chromium

CrSiO – Chromium silicon monoxide

NCAS - Nickel-chromium Aluminum Silicon

NiCrAlSi – Nickel-chromium-aluminum-silicate

FR4 – Flame Retardant type 4

Tg – Transition glass temperature

Tmp – Temperature melting point

CCA – Circuit Card Assembly

PB – Printed Board

PBA – Printed Board Assembly

DFM – Design for manufacturing

PCB – Printed Circuit Board

R&C – Resistor & Capacitor

DPMO – Defect per millions opportunities

COPQ – Cost of poor quality

ESD – Electrical static discharge

AME – Advanced manufacturing engineering

TCR – Thermal Coefficient of resistivity

B. Authors and Affiliations

Hikmat Chammas has been engaged in manufacturing processes and technology for over 25 years. He is currently the AME Electronics Processing and Fabrication Technology Fellow at Honeywell Aerospace in Phoenix Arizona. He pioneered the Surface Mount Technology (SMT) at Hadco Corp and established 4 green fields operations during his career in Circuit Card Assembly (CCA). He spear headed the development of DFM guidelines at Northrop Grumman, and ran training programs for the Hardware & CAD Engineering organizations. He has extensive experience in technology, including, SMT (BGA, CBGA, μBGA), NPD, PTH, Press-fit compliance pins (VHDM). He has developed cost modeling and DFM tools for value engineering (VE) that resulted in achieving cost reduction of several million dollars for block III, EGI, GMLRS, EGPWS, and other systems utilizing DFx methodology. Hikmat has a Bachelors of Science in Electrical Engineering from State University College at Buffalo, New York. He also completed a manufacturing management program (MMP) studies through Honeywell. He is Design For Six Sigma (DFSS) green belt certified.

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PBA Embedded Passives

“Technologies of the Future”

Hikmat Chammas
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February, 2013

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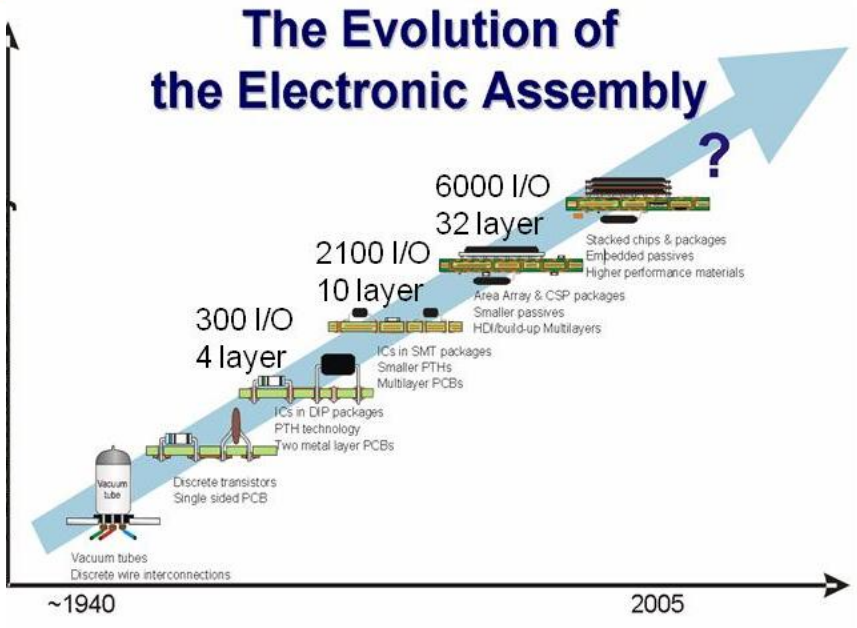
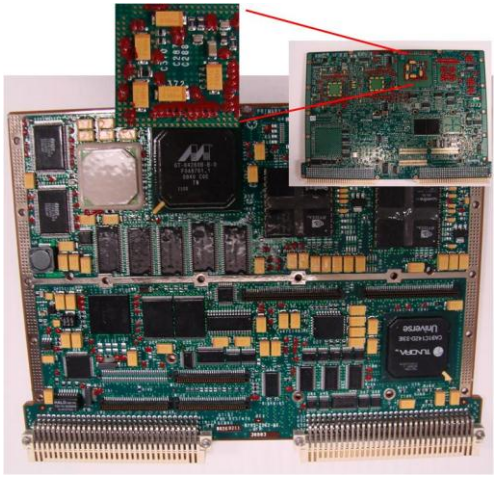
Current Design Challenges



Current Generation Design Example



- **11500 total I/O connections**
- **Miniaturized 0402 components**
- **16 layers**
- **Single digit FPY**
- **~80% real estate utilization**

Challenges

- Functionality demand is increasing while available PB real estate is decreasing.
- High I/O count devices challenge PB conventional routing practices
- High layer count designs(20+) are pushing PB manufacturers capabilities
- The DFM rules are being violated due to the high quantity of components placed on PB
- Component miniaturization challenges process capabilities

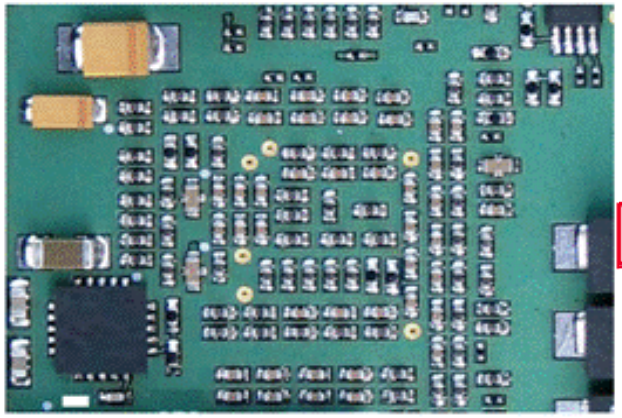
Problem Background/Motivation

- Customer demands for more increased functionality in complex PBA designs with limited real-estate has resulted in highly dense designs with low yield, DFM violations, and significant hidden factory rework during assembly
- Embedded passive technology originally emerged 20 years ago, in recent years has seen new growth driven by miniaturization of packaging, higher frequencies, and increased board density
- During the evaluation of the "Project" program, manufacturing related yield problems accounted for $2.7M in COPQ which prompted us to look for alternative technologies
- Embedded passive (R/C) technology provides a means to reduce the number of surface mounted components which increases yields, frees up real estate, lowers manufacturing costs, and reduces COPQ associated with complex designs

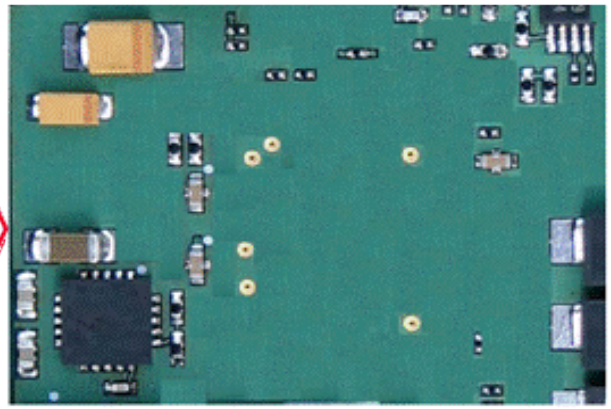
Embedded technology has potential to significantly improve yield

Embedded Passive Technology (EPT)

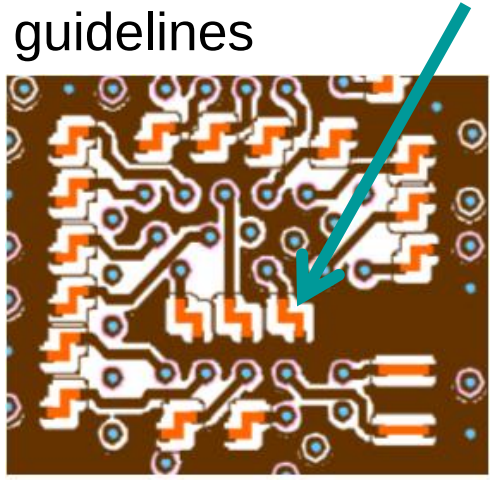
- Passive components are directly built into board substrate
  - Technology was developed in 1980's and used in telecom industry
  - Embedded components can be resistor, capacitors and inductors
- Benefits to OEM product offerings
  - Frees up real estate and improves product yield
  - Reduces product assembly cost by eliminating component placement
- Current barriers to implementation at OEM
  - Lack of internal design and manufacturing standards
  - Need to develop supplier requirements and design guidelines



Surface Mounts



Embedded

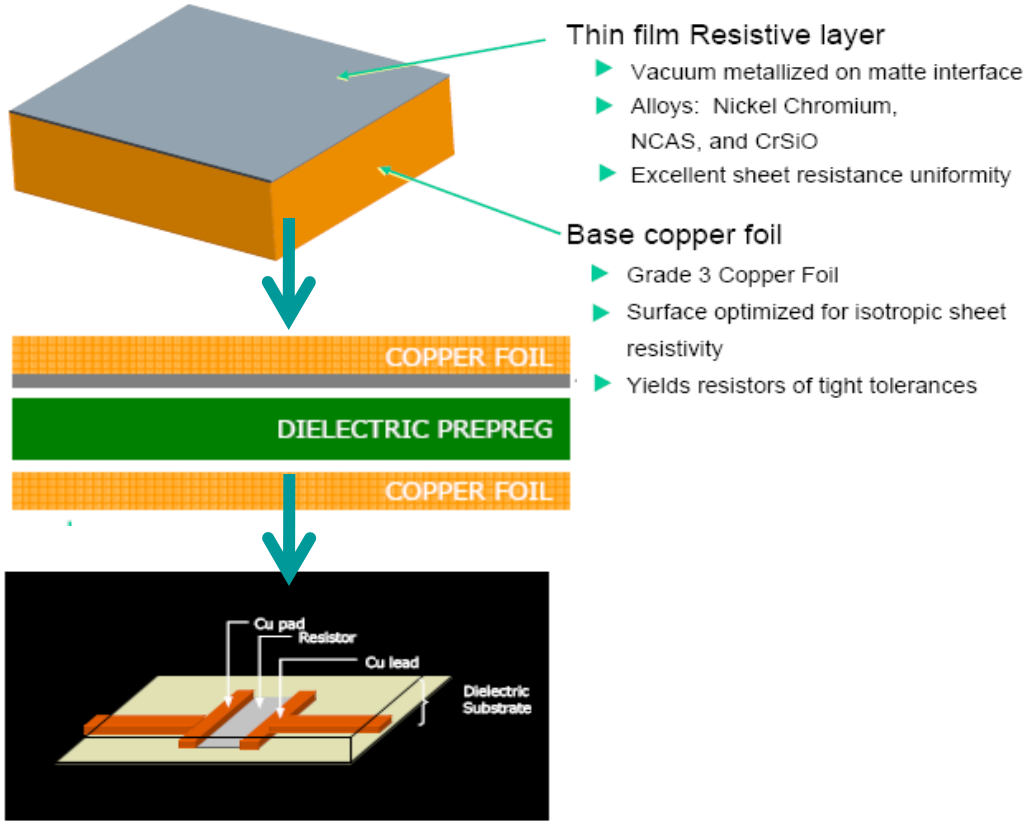


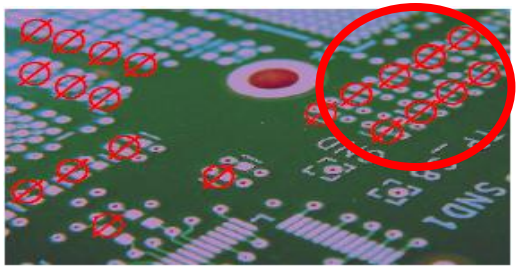
Embedded Resistor

Embedded Passive improves PBA yield and reduces cost

How Does Embedded Passive Technology works?

- Internal copper foil ply's are laser etched during board construction to create internal resistance paths (25, 50, 100, 250 and 1k Ohm) by a method of lamination
- Allows designers to replace surface mount resistors with internal ply's freeing space for additional functionality





Freeing space

BLANK

Embedded Passive Technology Game Changer

Objective, Background and Scope

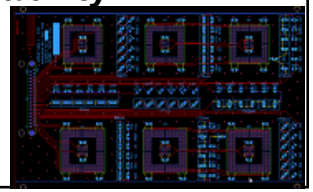
- Evaluation of Embedded Technology utilizing Ticer and OhmegaPly materials

Phase 1 – determine materials types based on resistance drift under thermal cycling (-55 C to 125C)

Phase 2 - Building an IPM (Imaging Processor Module) utilizing 2 resistive and 2 capacitance layers

Phase 1 - Highlights

- Designed and assembled 12 CCAs with 98 EP using 2 multiple resistor values & 2 different materials (Ticer & OhmegaPly)
- Testing: IST (300 cycles), HASS and HALT (50 years) were used to validate reliability
- Experiment resulted in selection of Ticer materials



Phase 2 - Highlights

- Due to complexity and yield issues IPM was selected.
- Generated 4 different layers of embedded materials
  - 2 Resistance layers – 25Ω and 1kΩ
  - 2 Capacitance layers
- Polyimide and FR4 materials were used
- Eliminated 985 surface mount components
- Laser trimming used to achieve 1% tolerance on 1kΩ

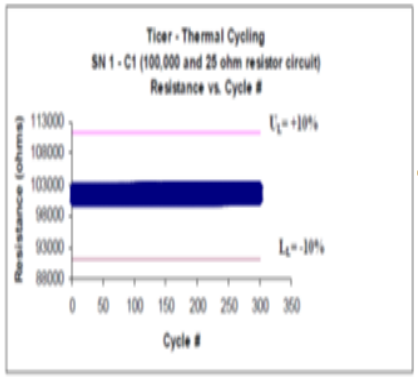
Original Design – High DFM violation

New Design – Low DFM violation

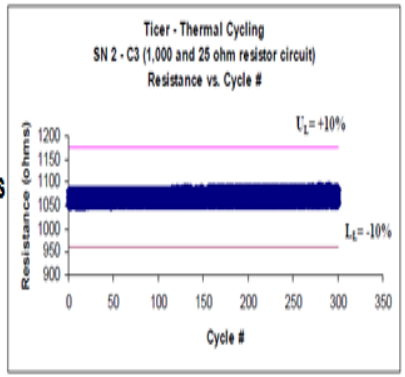
Embedded Passive Technology Phase 1

Phase 1 - Highlights

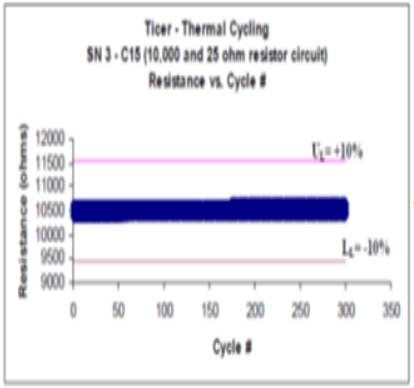
- Testing:
  - Board testing from two different suppliers
  - Coupon were defined to be ESD protected and Non ESD protected
  - 300 Thermal cycles to simulate life cycles years) were used to validate reliability
- Test Parameters:
  - Thermal Cycling -55° C to 125° C for 300 cycles simulating 20 year life cycle
  - ESD controlled test
  - No ESD controlled test
- Experiment resulted in selection of Ticer materials
- Results:
  - Supplier selection of embedded material



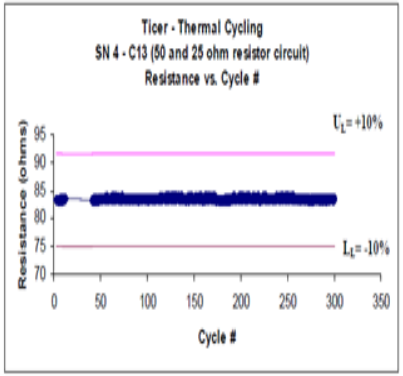
100k & 25 ohms



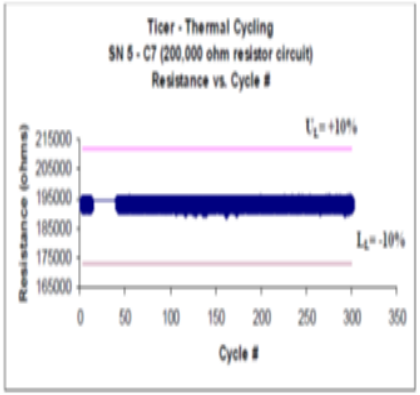
1k & 25 ohms



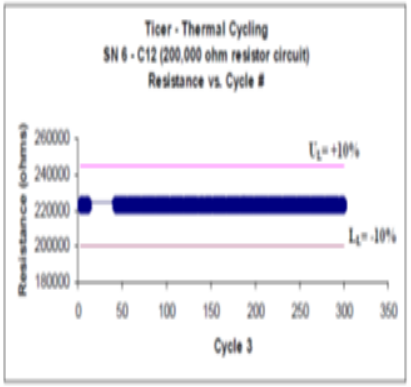
10k & 25 ohms



50 & 25 ohms



200k mixed



200k mixed

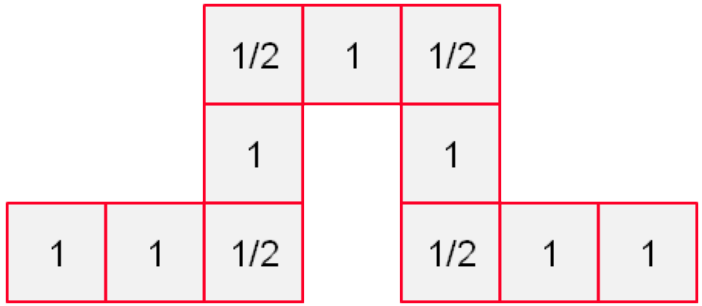
EP Resistor forming design

- The basic equation for calculating resistance value:

$$R = s(L/W)$$

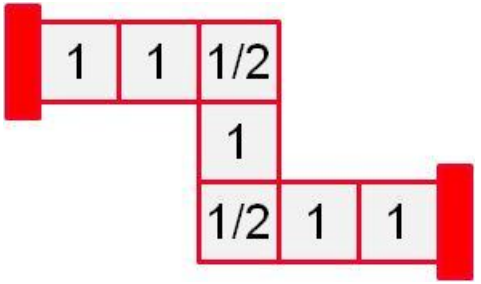
  - R – resistance in Ohms
  - L – length of resistor
  - S – sheet resistance in ohms/square
  - W – width of resistor

- Basic Shapes for EP



• **Top Hat shape**

• **Basic shape**

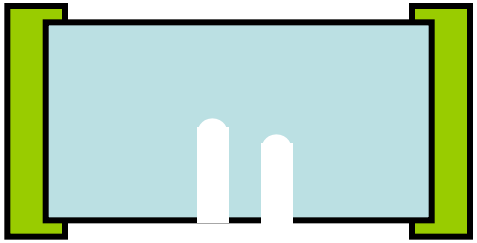


• R square in the corner area(s) of a bent R should be counted as ½ the value of sheet resistance.

Types Of Laser Trims

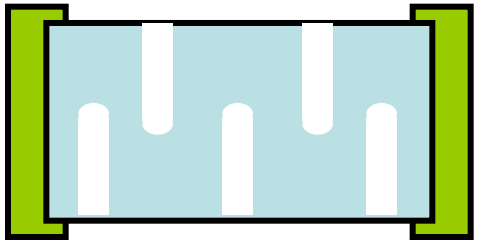
PLUNGE

DOUBLE PLUNGE

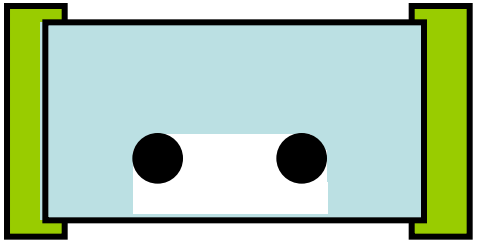


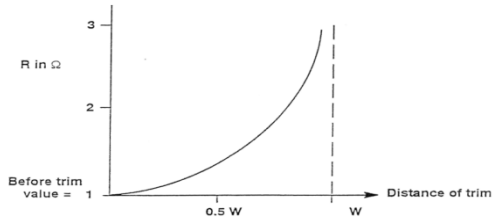
L-CUT

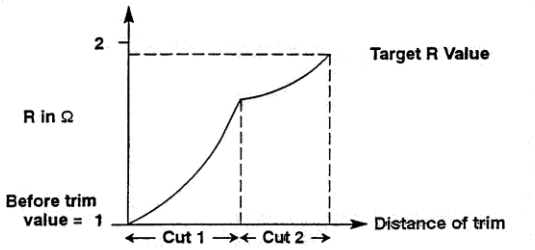
SERPENTINE

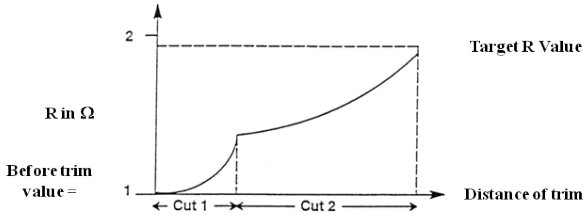


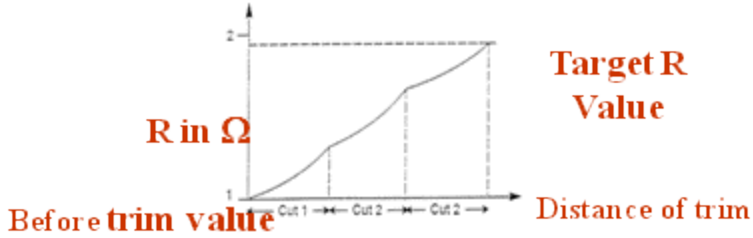
SCAN









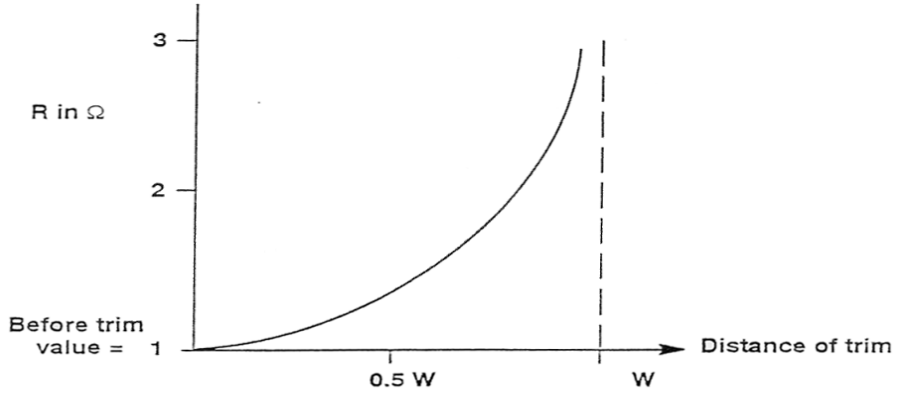


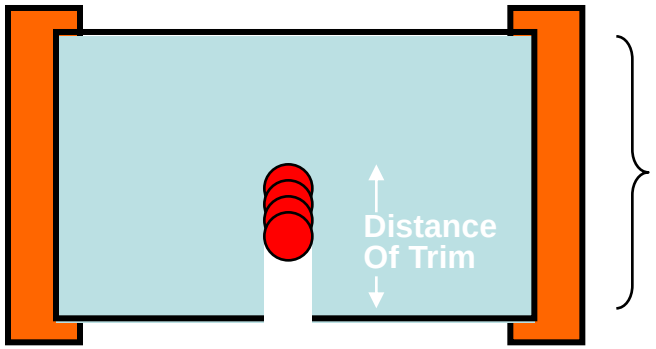
Resistor Trim Advantages & Disadvantages and Recommended Application

Resistor Trim Type	Recommended Application	Advantages	Disadvantages
Plunge Cut	DC	Min. Cost	Limited tolerance capability
L-Cut	DC	Increased accuracy – Lower tolerances	Slightly Higher cost than Plunge cut
Serpentine Cut	DC – High value R	Increased accuracy – Lower tolerances. Wider value flexibility	Higher cost
Scan Cut	All	Compatible with high RF application. Excellent tolerance accuracy	Highest cost

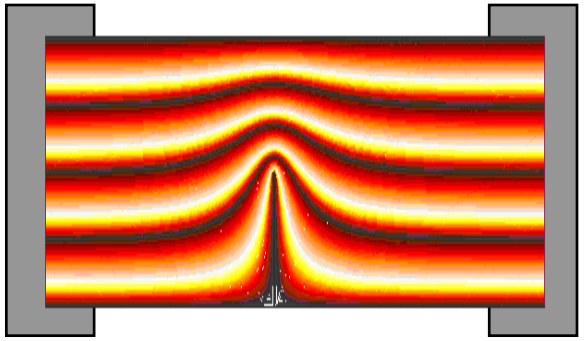
Plunge Cut Trim

- **Single directional laser trimming**
- **Less resistance materials the higher the R value**
- **The distance of laser trimming will determine the R value**

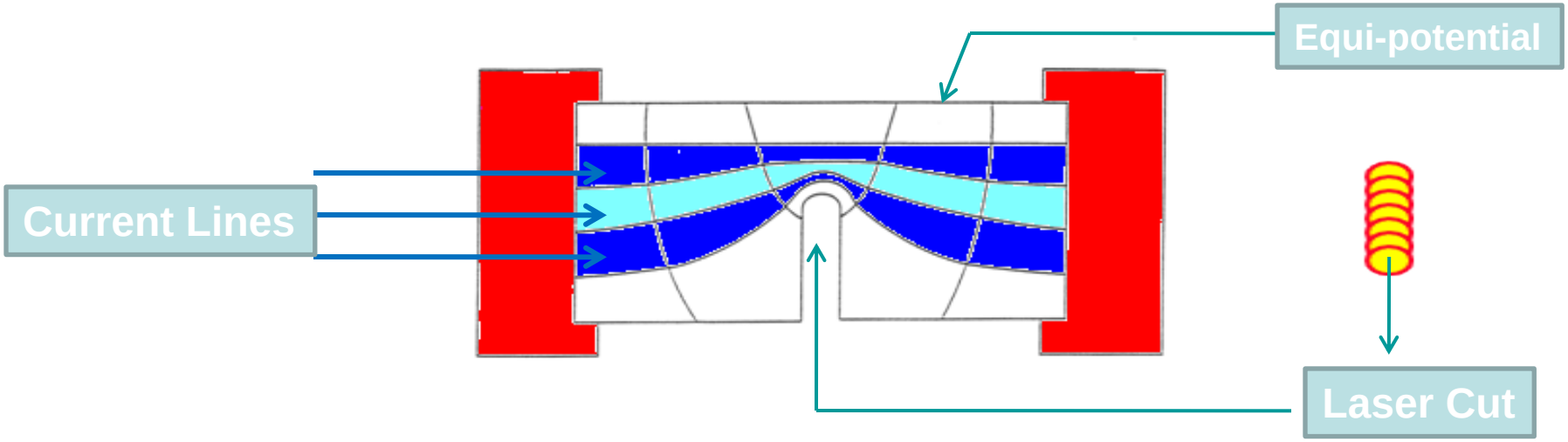




W=Width
Of Resistor



The Trimming Process



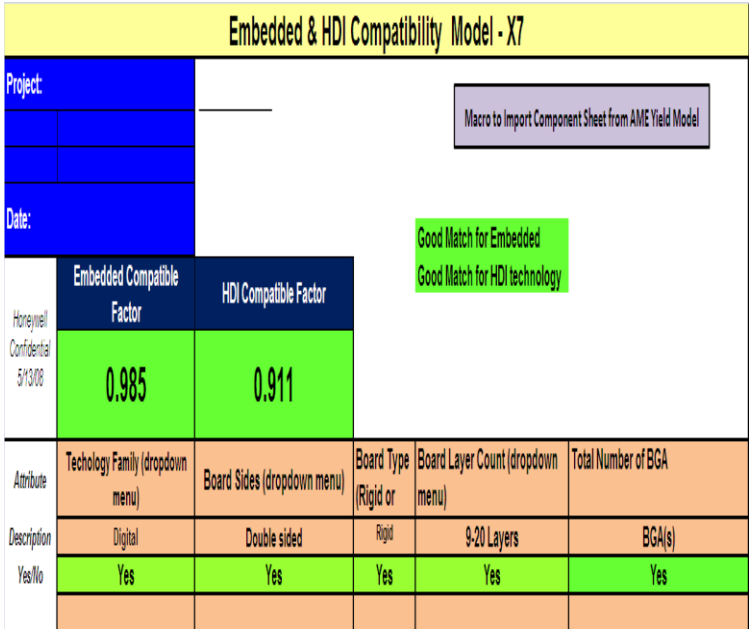
Trimmed resistor showing both current lines and equi-potential lines

- **The power dissipated in each square is still equal**
- **The top of the trim is a "hot spot"**
- **As the cut gets longer, the current density at the top of the cut gets higher**

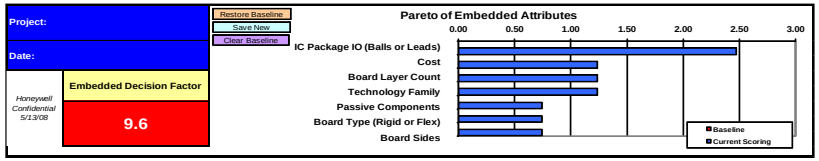
EP Technology Enabling Tool

Technology Insertion Evaluation

- Simple and easy to use enabling tool
- One Minute to determine PBA candidate
- PBA designs screened based on:
  - Board density
  - Component types
  - Layout complexity
- EP model is based on numeric score where 1 is the best match
- Processor PBA family identified as top candidate for conversion to EP and HDI technologies



Current Embedded Decision Models



Final Score is based on a 1 – 10 scale. The higher the score the better candidate for Embedded. Red = Should use Embedded; Yellow = good candidate, Green = No Embedded

Attribute #	Attribute Description	Enter X at selection
1	**Technology Family**	
	Digital	x
	Digital and Analog	
	Radio Frequency	
	Analog (Power supply)	
2	**Board Sides**	
	Single sided	
	Double sided	x
3	**Board Shape**	
	Rectangular/Square	x
	Round/Odd shape	
4	**Board Material**	

-14 different attributes with technology, Process and business elements
- 53 Attributes elements description
- Easy to use model
- Pareto attributes output chart

Cover the Design, Processes and Business Attributes

Supplier Qualification IST Coupon

- Utilization of IST coupon to determine supplier capabilities and process control
- Design IST coupons
- Test parameters utilized per IPC-TM-650 spec
  - At 150C for 500 cycles
  - Sense and capacitance testing
- Supplier selections were defined based on present capabilities and geographical locations:
  - North America
  - Emerging Regions
- Results:
  - North American supplier has more controlled fabrication process
  - Emerging market need to be develop

Summary and Conclusion

- Product miniaturization is the standard for electronics packaging
  - Drives design complexity and producibility challenges
  - Drives significant hidden cost
  - Packaging challenges (10 lb in 2 lb container)

- These technologies will provide:
  - Yield improvement and cost reduction
  - Reduce manufacturing cycle time
  - Reduction in number of components
  - Reduction in complexity and DFM violations

- Future work aimed at implementation of HDI and EP
  - These technologies are needed to meet the increased functionality demands
  - Tools have been developed to evaluate design for technology implementation
  - Guide technology insertion evaluations for HDI and EP and implement

These enablers provide the means to meet demand for miniaturization

Questions?

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Honeywell