The Coming of The MultiChip Module

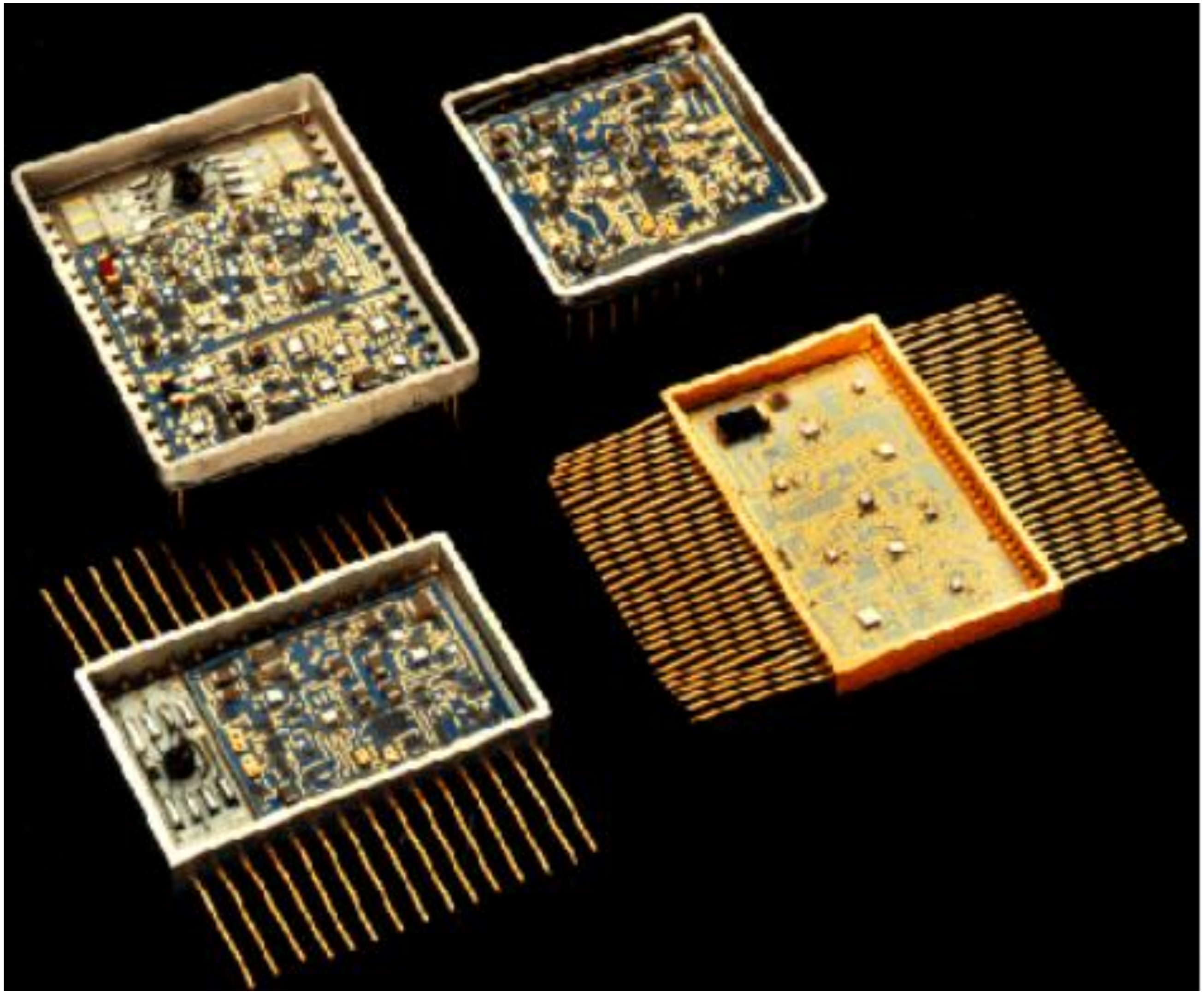
Dieter Bergman
IPC Director of Technology Transfer - Emeritus

MultiChip Module Status

- It isn't a new idea since back in the 1980's everyone was trying to combine different components into a single package
- It started with Hybrids then different forms of SMT
- Since that time many methods have been used to bring higher operating performance to electronic assemblies
- Coined phrases such as System-in-a Package, Package-on-Package, or Application Specific I/C abounded
- However with the breakthrough of being able to create a Via between wafers (Through- Silicon-Vias) other new forms are evloving

The Hybrid Microcircuit Era

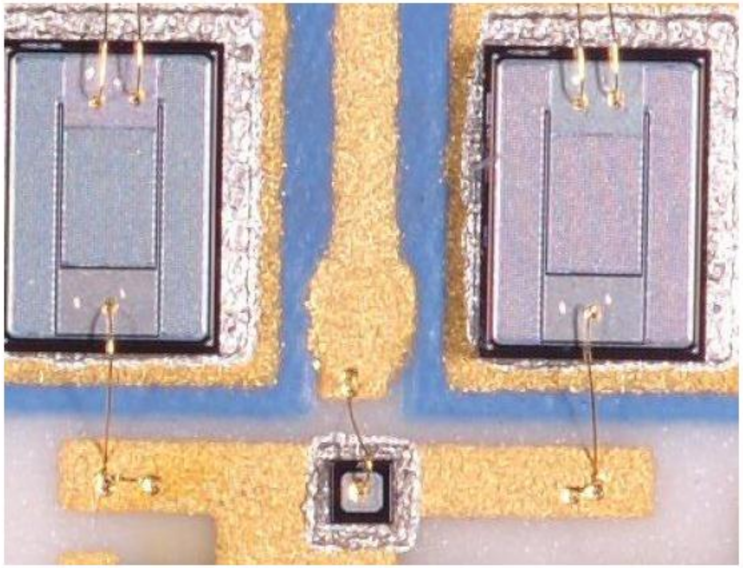
Many different packages and lead forms for input or output signals



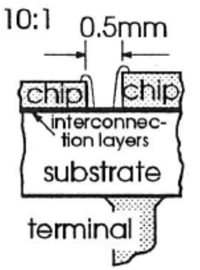
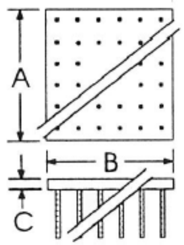
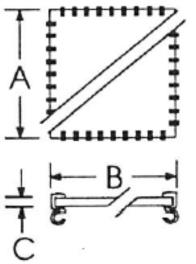
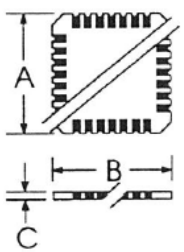
Design Services Helped

CERAMIC MULTI-CHIP MODULES

- *Signal frequencies up to 5GHZ*
- *Excellent thermal matching between chips*
- *Risk of cracks in chips eliminated*
- *Simple reliable construction*
- *Small developments costs*
- *The quality system correspond to ISO 9001*



Physical Data

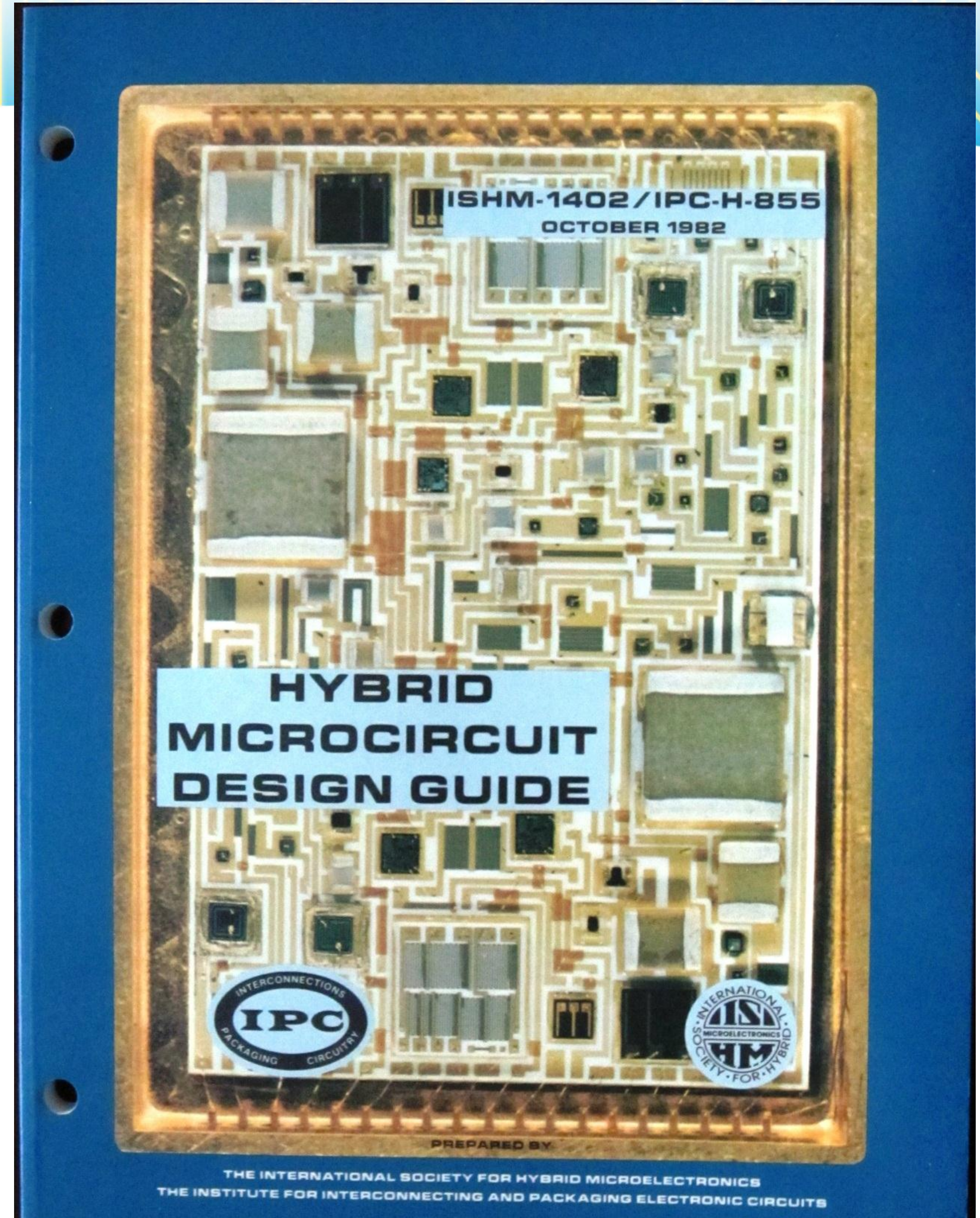
Type	Dimension (mm)					Number of terminals		Typical chip position	Terminal arrangement		
	A		B		C				PGA	PLCC	LCC
	Max	Min	Max	Min	Nom	Max	Min				
PGA	50.8	12.7	50.8	12.7	1.0	400	16				
PLCC	30.5	7.6	30.5	7.6	0.8	84	20				
LCC	30.5	7.6	30.5	7.6	0.6	84	20				

Working Together to Establish Ceramic Reliability

- In 1980 IPC had a Hybrid Circuits Committee made contact with the ISHM board of directors to see if ISHM and IPC would work together.
- Their Board of directors approved the idea
- As a result 5 workshops were held hosted by ISHM and IPC.
- IPC’s technical editor created the review drafts from the meetings
- The results were published in 1982

APEX EXPO IPC 2013

One Publication effort with quantities split between IPC and ISHM with either Organization to sell to their members



Standards with Application in Today's and Future Technology

IPC

The Institute for Interconnecting and Packaging Electronic Circuits

IPC-D-859

Design Standard for Thick Film Multilayer Hybrid Circuits

ANSI/IPC-D-859
Original Publication
December 1989

A standard developed by the Institute for Interconnecting and Packaging Electronic Circuits

2215 Sanders Road
Northbrook, Illinois
60062-6135

Tel 847 509.9700
Fax 847 509.9798
URL: http://www.ipc.org

Design standard published in 1989

IPC

The Institute for Interconnecting and Packaging Electronic Circuits

IPC-HM-860

Specification for Multilayer Hybrid Circuits

Performance standard published in 1987

IPC

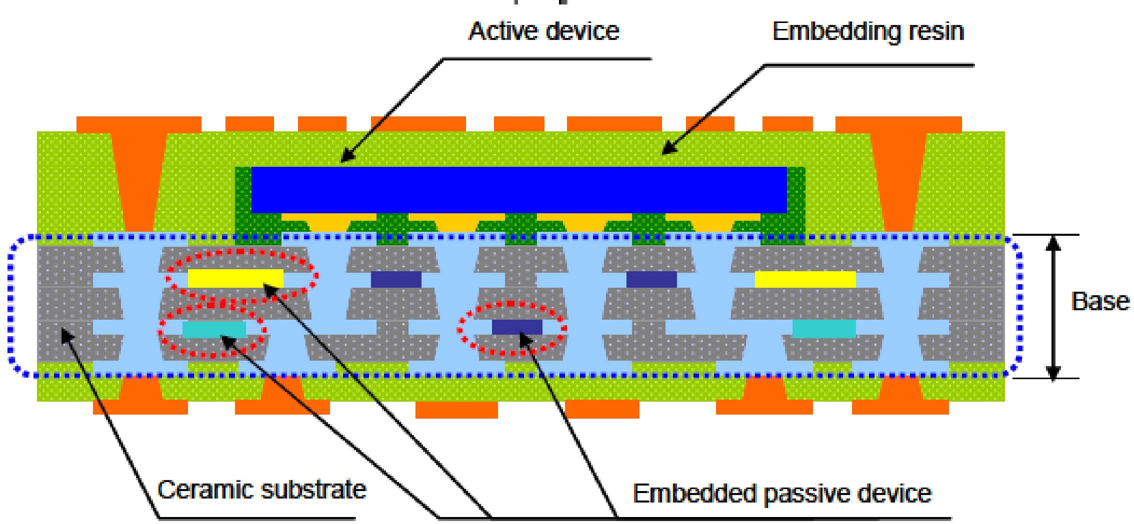
The Institute for Interconnecting and Packaging Electronic Circuits

IPC-TF-870

Qualification and Performance of Polymer Thick Film Printed Boards

Qualification standard published in 1987

Embedded Board Application



Surface Mounting Reliability

- 1985 ; US Secretary of Defense indicates "Surface Mounting is a technology at risk"
- EIA, IPC & SMTA form the Surface Mount Council made up of about 35 individuals.
- The Council never wrote standards but brought focus on what was needed.
- They published their first status and Action Plan in 1987

Council Membership

- The Surface Mount Council is made up of key industry representatives dedicated to promoting the use of surface mount and advanced electronic packaging technology in the design and production of electronic hardware.
- Council Members represent user, supplier and equipment manufacturing companies engaged in surface mount implementation for automotive, telecommunication, computer, instrument, government, consumer, and medical electronics.

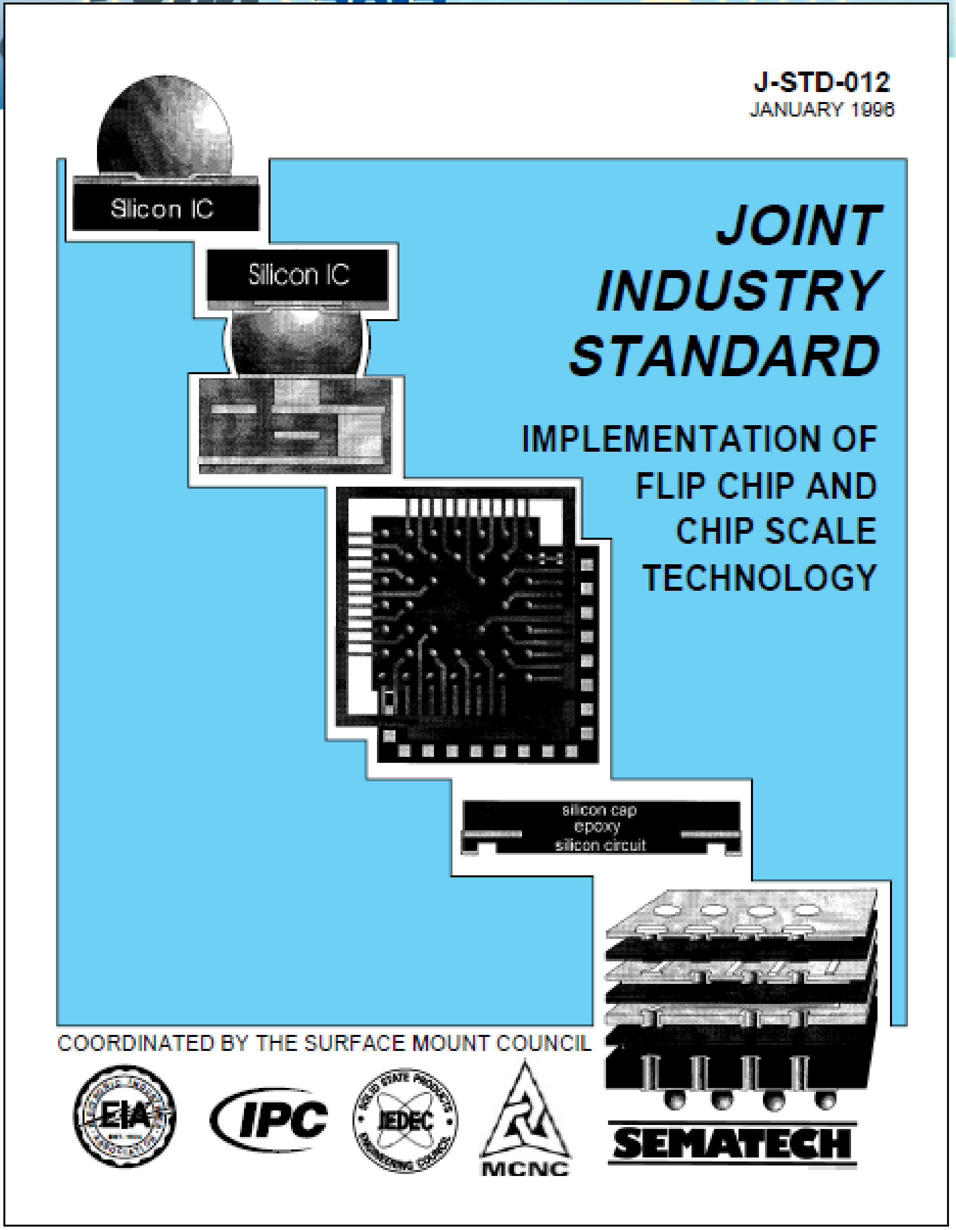
Council Mission Statement

The mission of the council is to facilitate, coordinate, and promote the orderly implementation of surface mount and advanced electronic packaging technology through standardization, the development of technical documents, and other means.

1985 -1999 Council Accomplishments

Reliability Matrix For SMT Solder Joints

Worst-case use environment							
Use category	Tmin °C	Tmax °C	ΔT°C	t_D hrs	Cycles/ year	Typical years of service	Approx. accept. failure risk %
1) Consumer	0	+60	35	12	365	1-3	1
2) Computers	+15	+60	20	2	1 460	5	0.1
3) Telecom	-40	+85	35	12	365	7-20	0.01
4) Commercial aircraft	-55	+95	20	12	365	20	0,001
5) Industrial & automotive Passenger Compartment	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	10	0.1
6)Military Ground & ship	-55	+95	40 &60	12 12	100 265	10	0.1
7) Space leo geo	-55	+95	3 to 100	1 12	8 760 365	5-30	0.001
8)Military avionics a b c	-55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	10	0.01
9)Automotive under hood	-55	+125	60 &100 &140	1 1 2	1 000 300 40	5	0.1



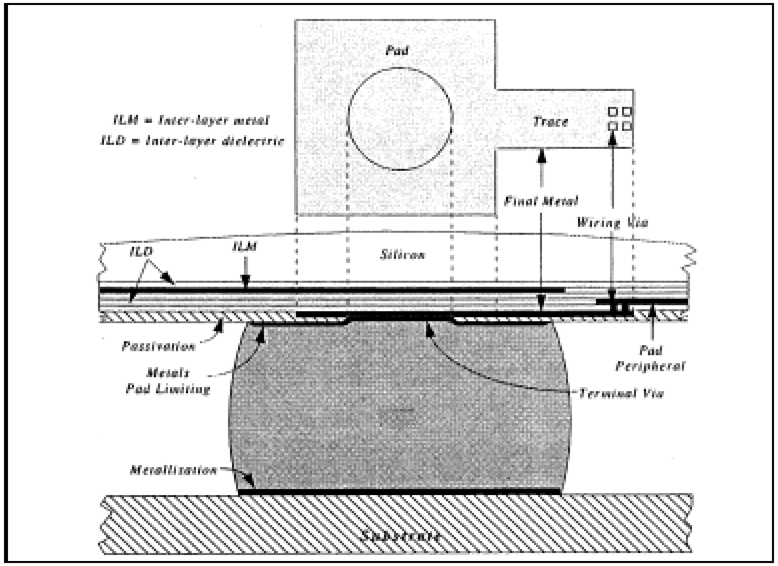


Figure 4–30 Bump Electrical Path (Redistributed Chip)

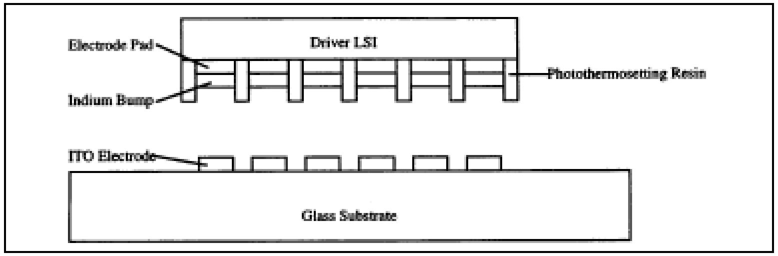


Figure 5–5 Newly Developed Chip on Glass Technology

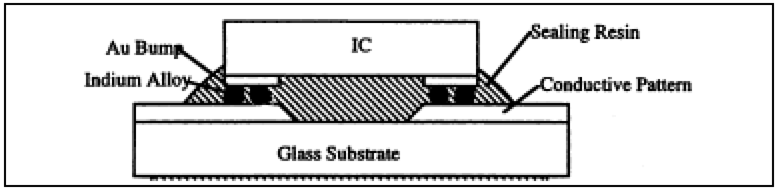


Figure 5–6 Schematic Cross-Sectional View of Connection for Chip on Glass

Fostered and Coordinated by the Council

J-STD-012 Illustrations

Early examples of MCMs

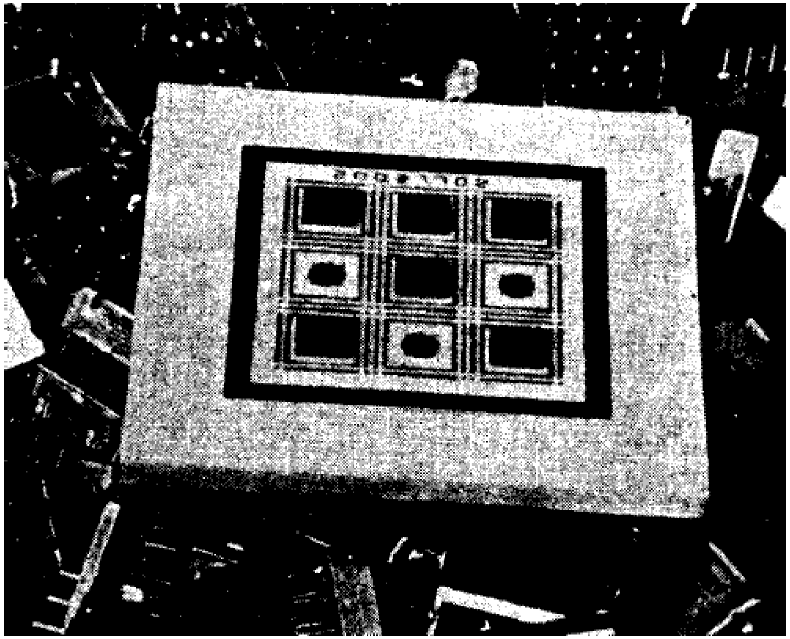


Figure 2−12 Uncapped 50 mm Multi-Chip Module (MCM)

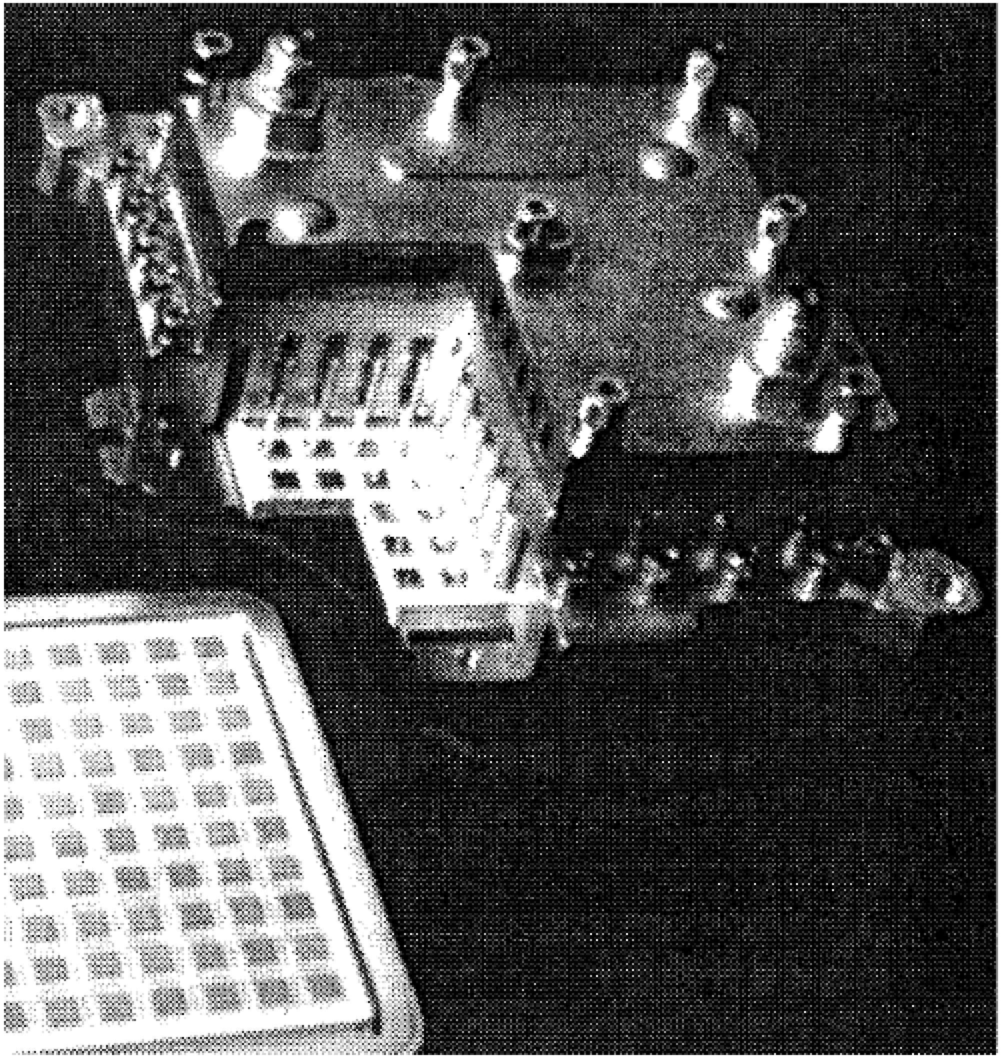
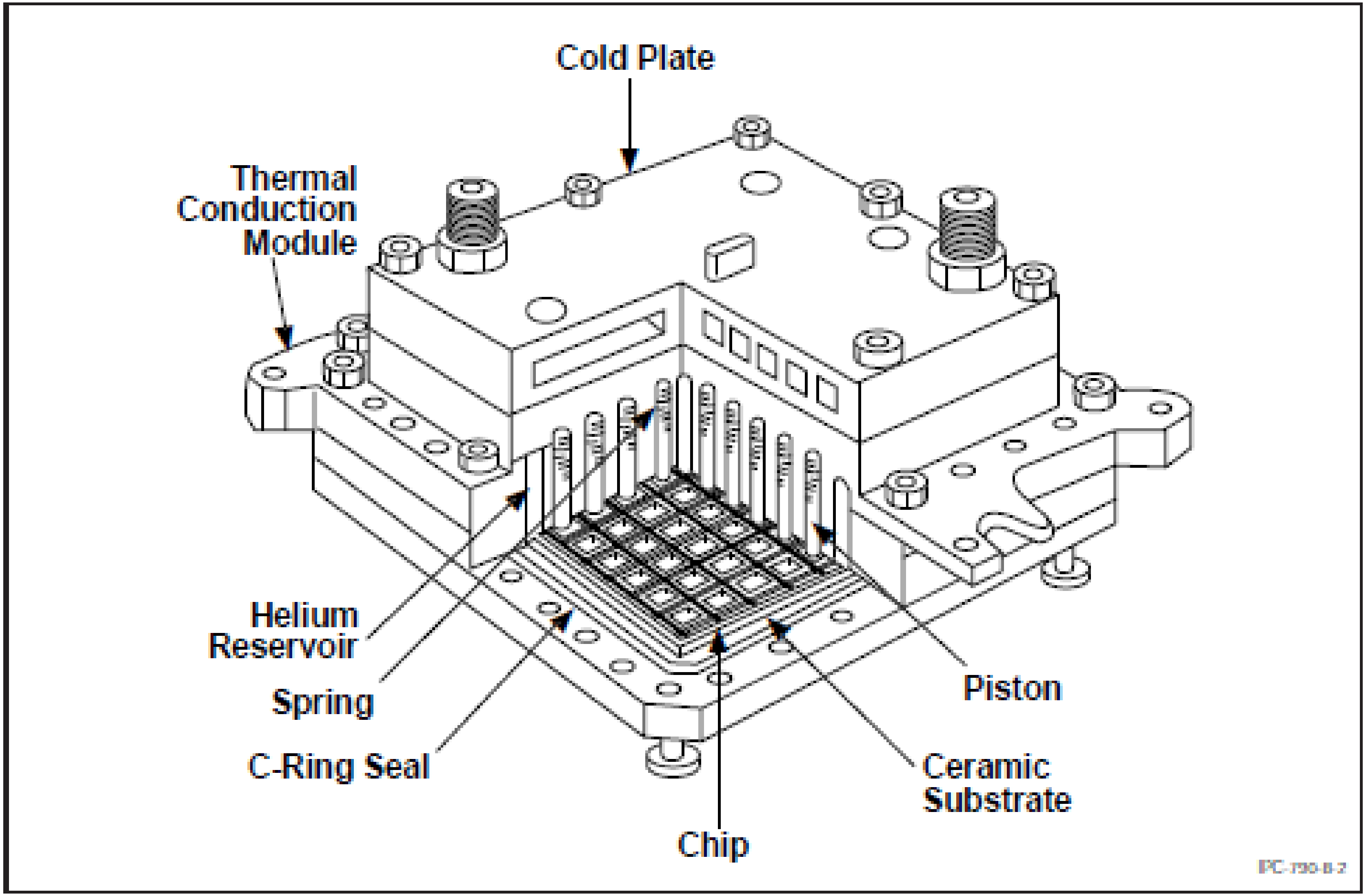


Figure 2−13 IBM Thermal Conduction Module with 100-130 Flip Chips and Hat with Piston Assemblies

Detail Attention to Cooling



Published 1992

Section 3 MCM-C Design Considerations (Ceramic/Glass Based Materials)

3.0 INTRODUCTION
3.1 Layout
3.2 Conductor Pattern
3.3 Conductor Routing
3.4 Land Patterns
3.5 Wire Bonds
3.6 Vias
3.7 Resistors
3.8 Substrate Requirements

Section 4 MCM-L Design Considerations (Organic Based Materials)

4.0 INTRODUCTION
4.1 Design Layout
4.2 Conductor Pattern
4.3 Land Pattern
4.4 Holes
4.5 Resistors
4.6 Substrate Materials

Section 5 MCM-D Design Considerations (Deposited Dielectric Films)

5.0 INTRODUCTION
5.1 Layout
5.2 Conductor Pattern
5.3 Conductor Routing
5.4 Land Patterns
5.5 Vias
5.6 Resistors
5.7 Integrated Circuit Die (Chips)
5.8 Dielectrics .
5.9 Substrates

IPC
ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES

IPC-MC-790

Guidelines for Multichip Module Technology Utilization

"LOGICAL FUNCTIONAL BLOCKS GROUPED TO MAXIMIZE INTERCONNECT WITHIN A COMPACT ASSEMBLY, YET MINIMIZE INTERCONNECT TO THE NEXT LEVEL"

IPC-MC-790
July 1992 A standard developed by IPC

2215 Sanders Road, Northbrook, IL 60062-6135
Tel. 847.509.9700 Fax 847.509.9798
www.ipc.org

MCM Characteristics

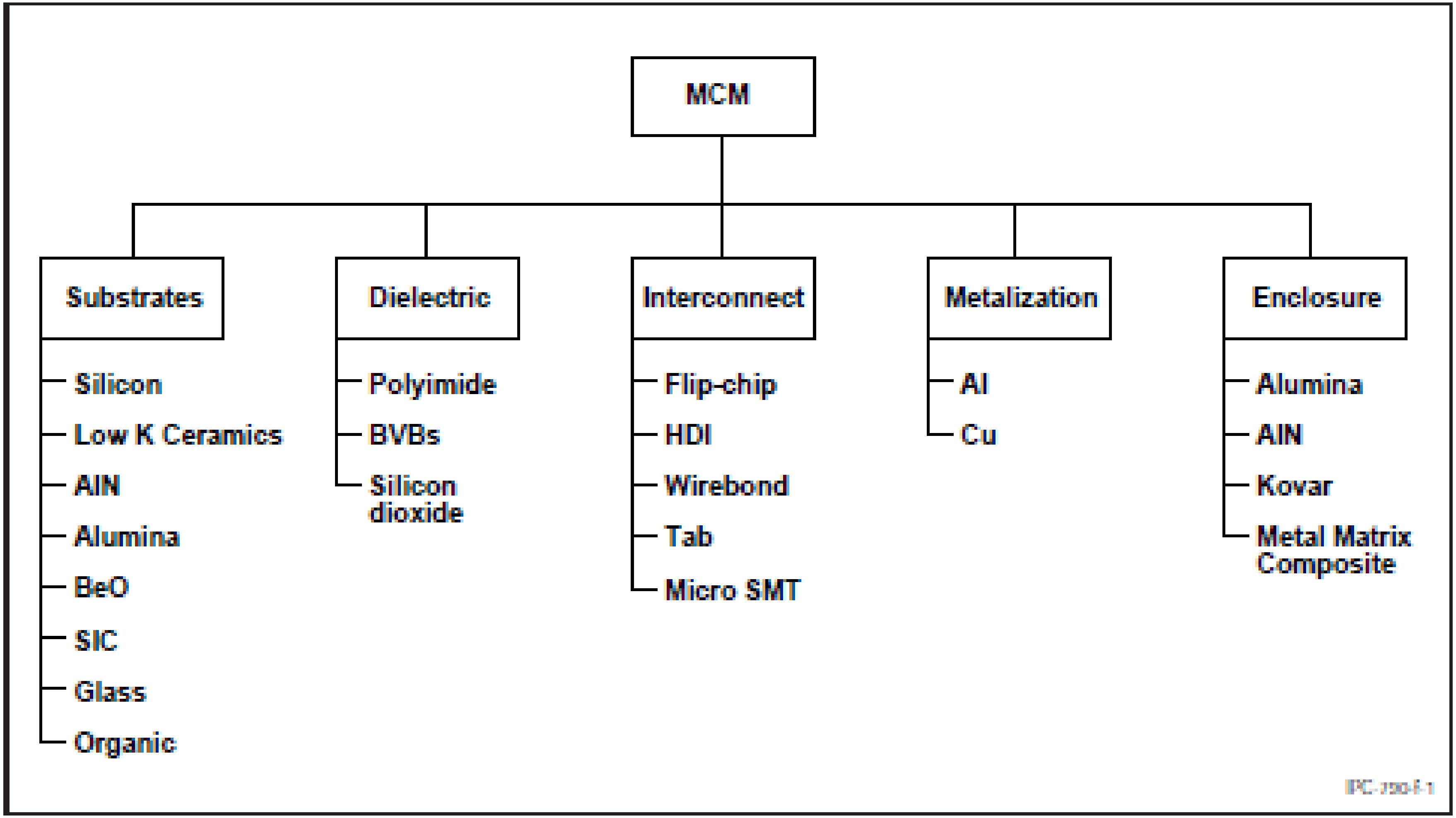


Figure F-1 MCM options

Multichip Module C

- Multichip modules identified by the letter C normally are constructed of ceramic or glass ceramic alternatives. These materials have a dielectric constant that is 5.
- Performance of the MCM-C considers the dielectric properties between single planes or between single planes and ground planes.
- The materials act as both the dielectric and the supporting plane for the components.
- Conductors are usually a fireable metal material such as tungsten, molybdenum, and the screenable frit metal thick film conductors of gold, silver, palladium and copper.
- When these materials are used to form the conductors, the conductor width is <0.15 mm Vias necessary during the interconnecting process are formed during the conductor screen printing,
- The vias are usually the same materials as the conductor.
- For most Multichip C applications, the number of active devices is greater than the passive components

Multichip Module D

- Multichip Modules identified by the letter D are normally constructed using unreinforced dielectric materials that are adjacent to the signal plane.
- The dimensional stability of this type of module is determined by the underlying substrate which is usually made of ceramic, silicon, copper, glass-reinforced laminate, or other metal or metal composites.
- The dielectric materials normally have a dielectric constant of <5.
- The additive dielectrics may be deposited on the substrate or may be deposited on a metal platen and peeled off to be reapplied elsewhere in fresh situations.
- Conductors are sputtered or plated. The materials may be aluminum, copper, or gold. Photolithography is used to provide the imaging of the conductor patterns.
- Vias may be formed during the conductor deposition/ plating processes. When deposition and plating are used in combination, the vias are plated after conductor deposition

Multichip Module L

- Multichip Modules identified by the letter L use laminated printed board fabrication technology.
- Laminated layers may be reinforced or unreinforced and consist of such resin materials as epoxies, polyimides, or acrylics, reinforced with fiberglass, quartz, Kevlar, etc.
- The dielectric materials normally have a dielectric constant of <5.
- Conductors are almost always copper. These are deposited additively or are generated as part of the printed board subtractive process. Vias are copper, electrolessly plated initially, followed by additional electrodeposition.
- When the MCM-L requires control of the coefficient of thermal expansion, lamination techniques use materials that have low CTE such as copper-invar-copper.
- MCM-L were usually the lowest cost solution

Out of the Ashes

- In 2000 the SMC had completed most of their work, and decided to adjourn the council.
- Japan had just complete what they called a Jisso Technology Roadmap.
- At an IEC meeting in Japan, Kisao Kusuga, NEC, a key developer of the Jisso concept requested that US and Europe join Japan in the effort.
- IPC hosted the first meeting of the JIC in Chicago.
- The JIC has 3 subgroups JEA (Jisso East Asia), JNAC (Jisso North America), JEC, (Jisso European Council)
- The council meets yearly; JIC 14 scheduled for Seoul, Korea in April 2013

Mission Statement for the Jisso International Council (JIC) by IPC,JEDEC and EIAJ in May, 2000

The purpose of this council is to promote a strategic partnership among global organizations interested in the total solution for interconnecting, assembling, packaging, mounting, and integrating system design.

To accomplish these objectives, members will cooperatively work:

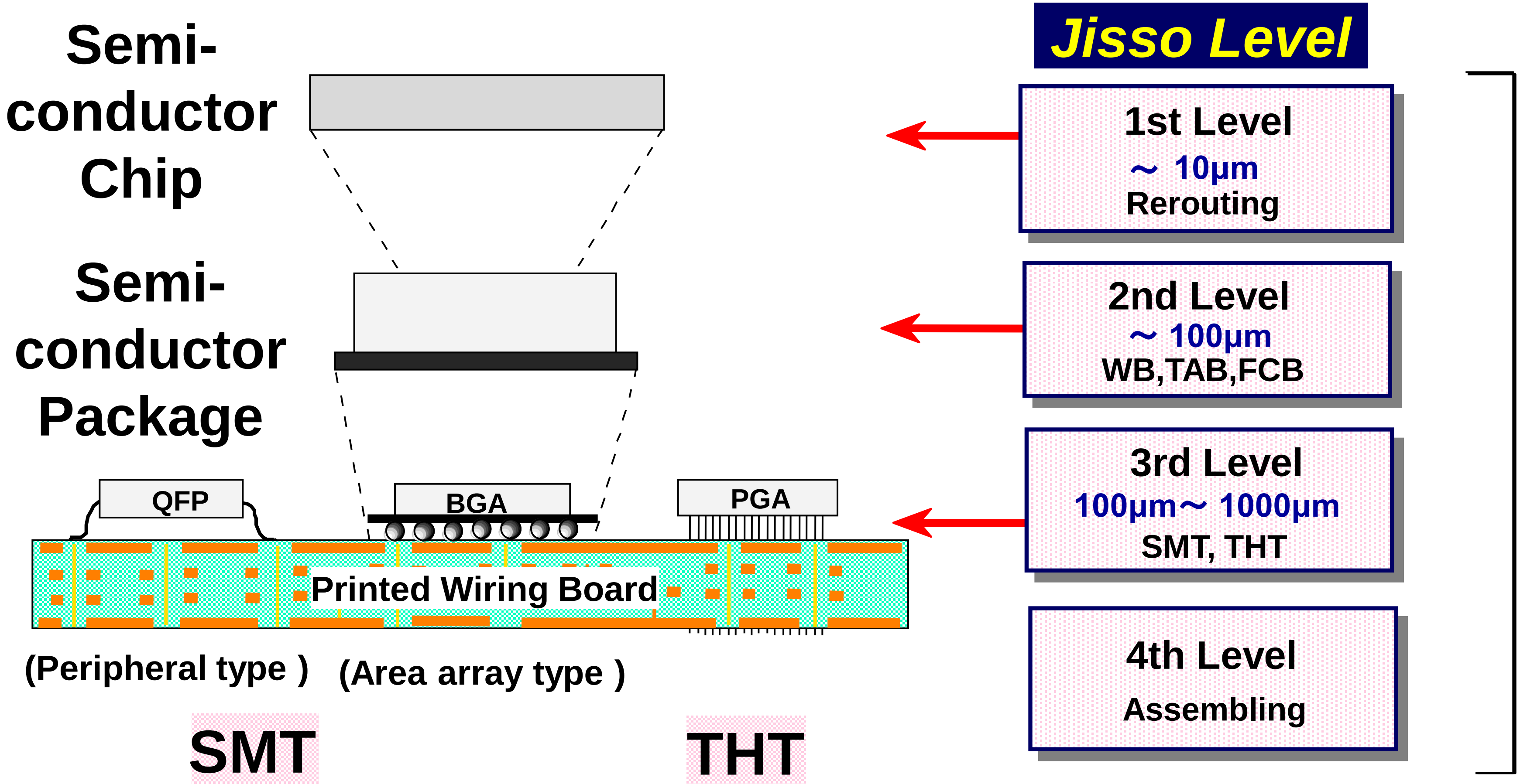
to support and encourage standards development at a national or international level, to encourage the development of technology roadmaps, to address environmental issues, and to monitor market trends.

These activities will be based on the principles of free enterprise, cooperation, and will be undertaken in a spirit of responsibility to the worldwide electronics industry.

Jisso International Council, May 2000

The Concept of Jisso

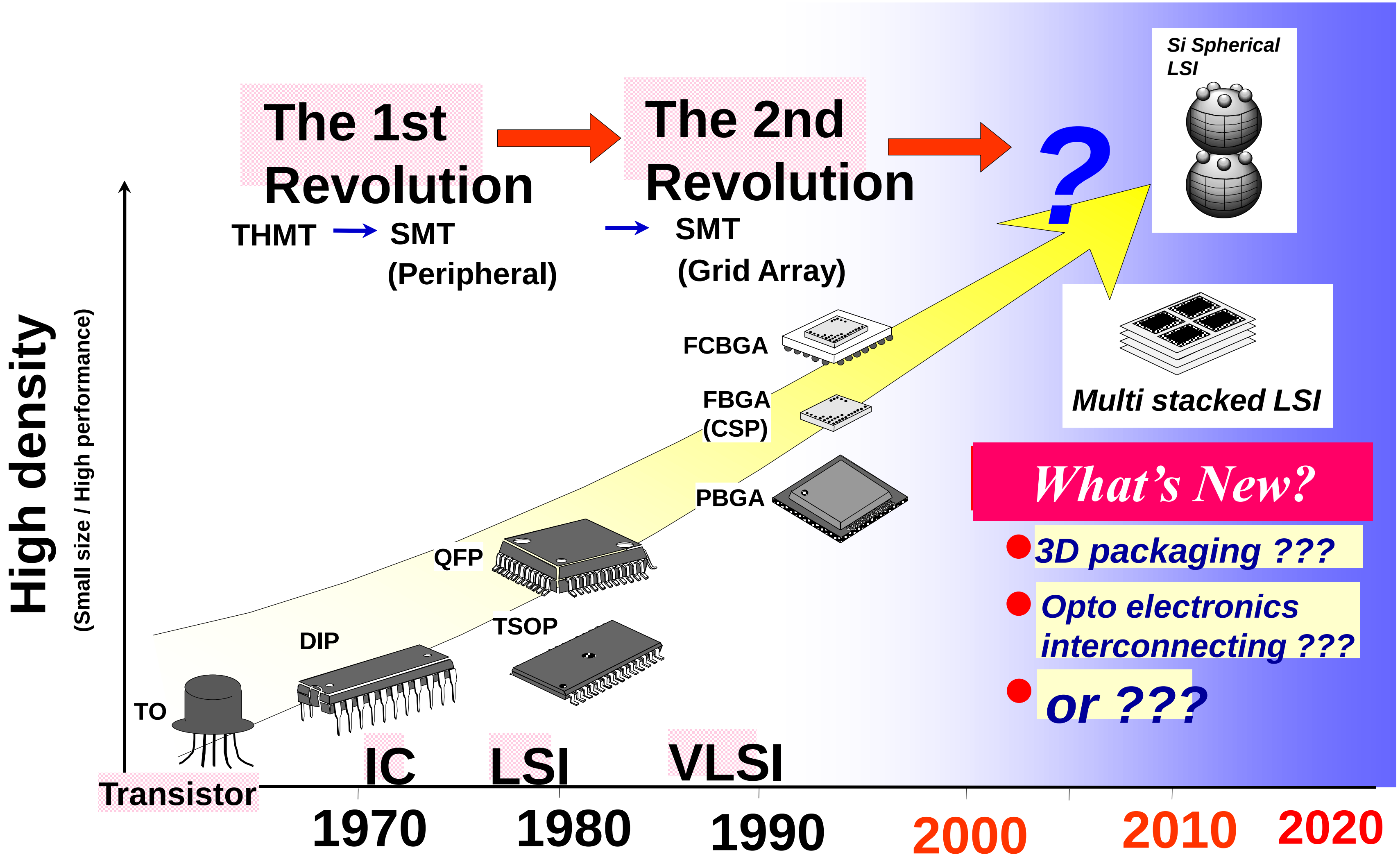
A Total Packaging solution for Interconnecting, Assembling, Packaging, Mounting and Integrating system design.



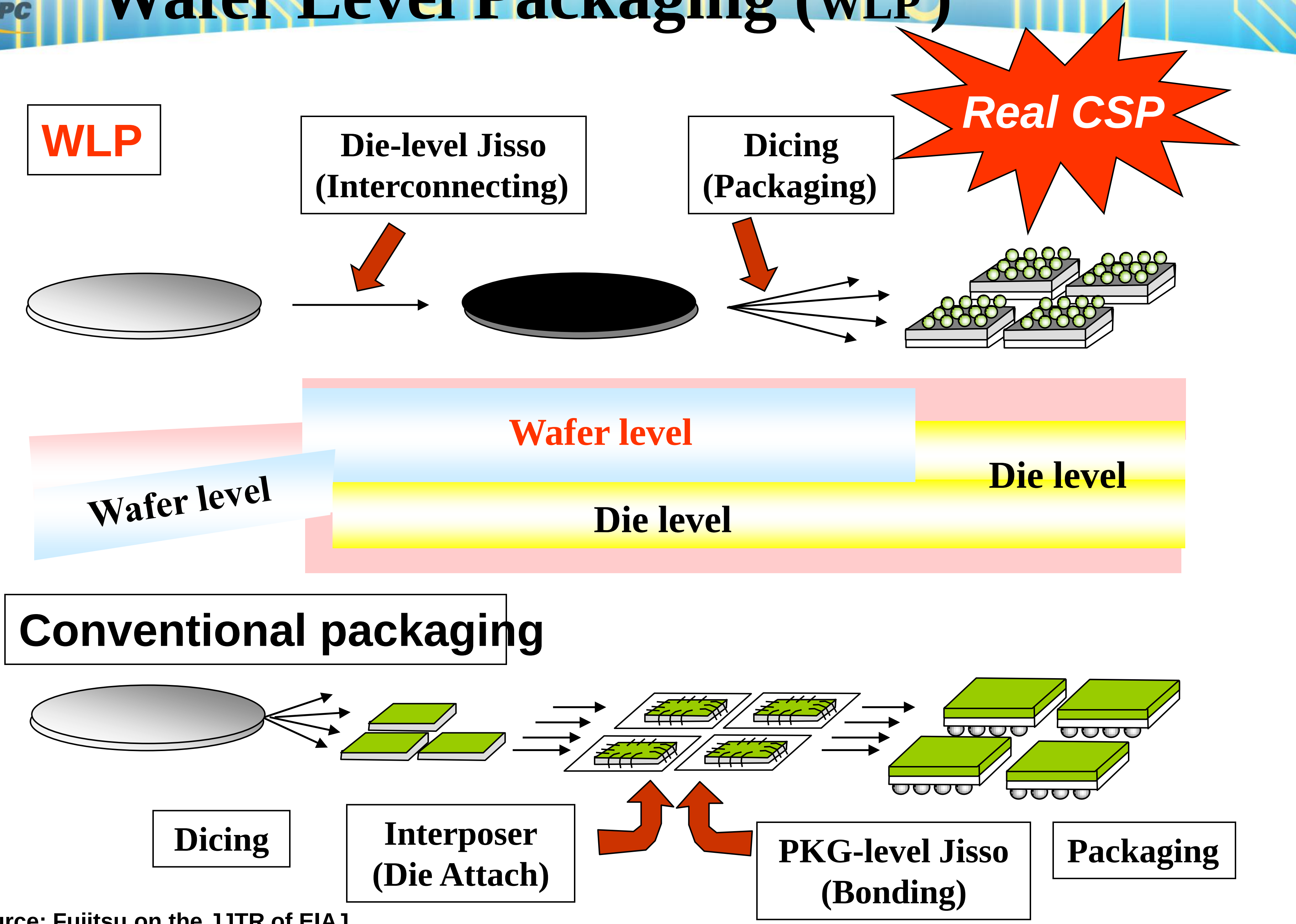
SMT : Surface Mounting Technology

THT : Through Hole Mounting Technology

Jisso Technology Revolution on High Density Mounting toward the 21st century

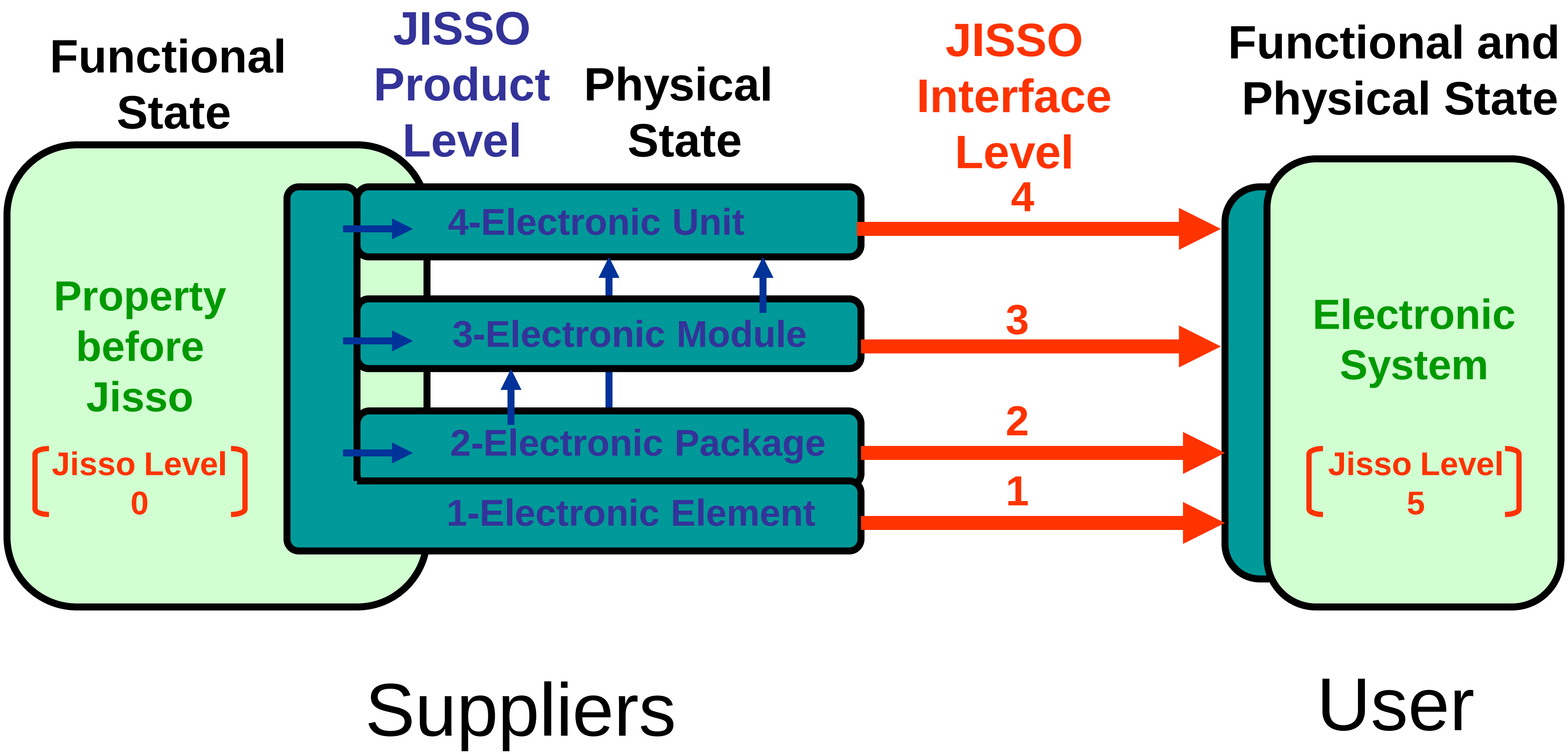


Wafer Level Packaging (WLP)



Source: Fujitsu on the JJTR of EIAJ

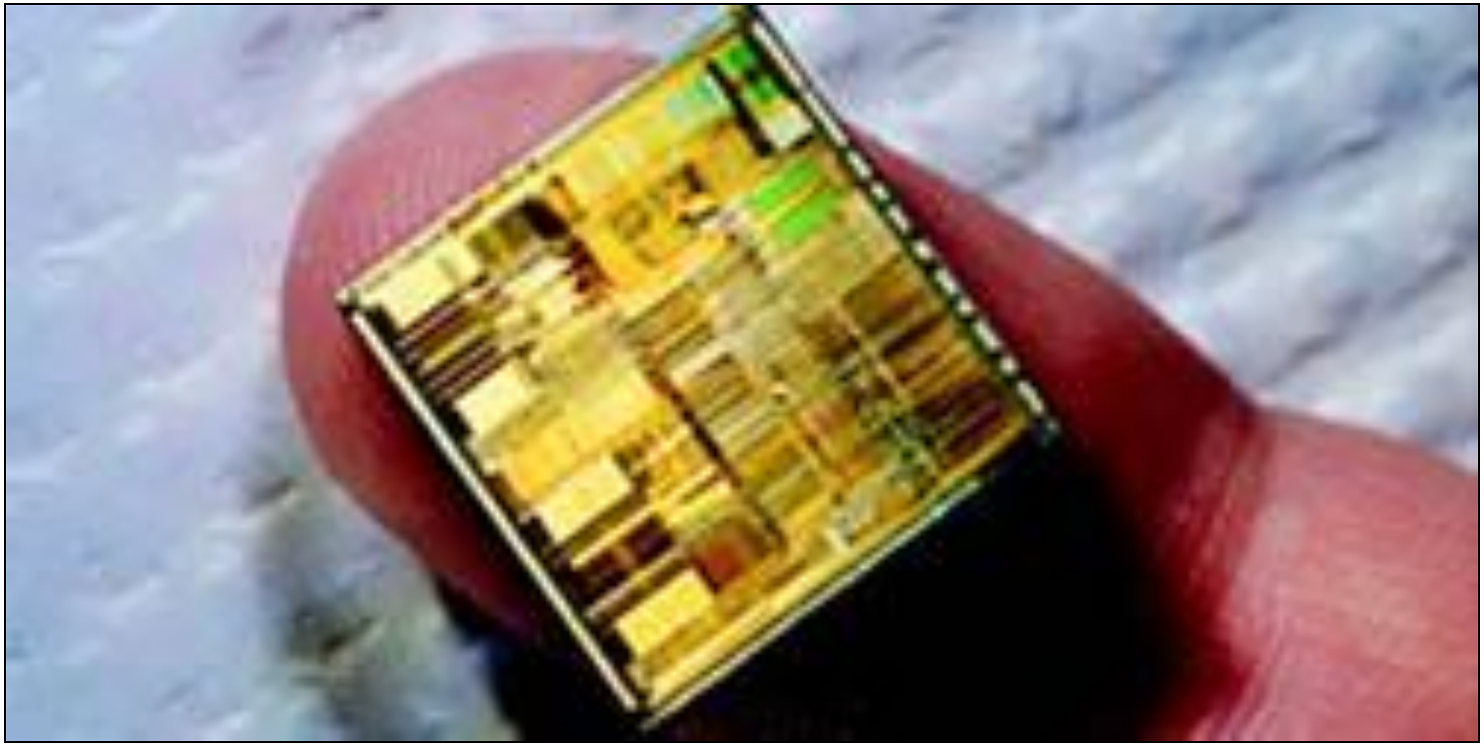
JISSO Levels Concept



Definition of Basic Jisso Levels

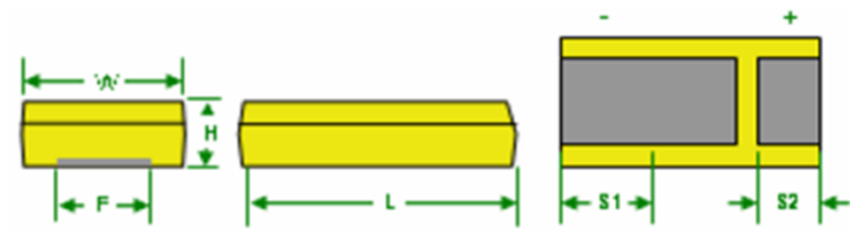
- **Level 0 - Property before Jisso**
  - Includes standards, patents and proprietary methodology
- **Jisso Product Level 1 – Electronic Element**
  - Bare die/Wafer ready to be mounted, semi-finished component
- **Jisso Product Level 2 – Electronic Package**
  - Electronic, Optoelectronic, Mechanical MEMS, Includes finished components
- **Jisso Product Level 3 – Electronic Module**
  - Electronic, Optoelectronic, Mechanical MEMS
- **Jisso Product Level 4 – Electronic Unit**
  - Electronic, Optoelectronic, Mechanical MEMS
- **Level 5 – Electronic System**
  - Electronic, Optoelectronic, Mechanical, Backplane, Housing or Cabling

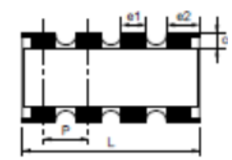
Individual Electronic Element Example

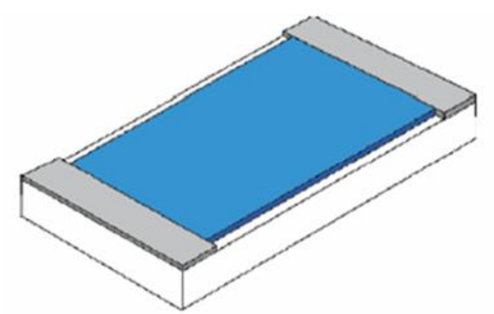


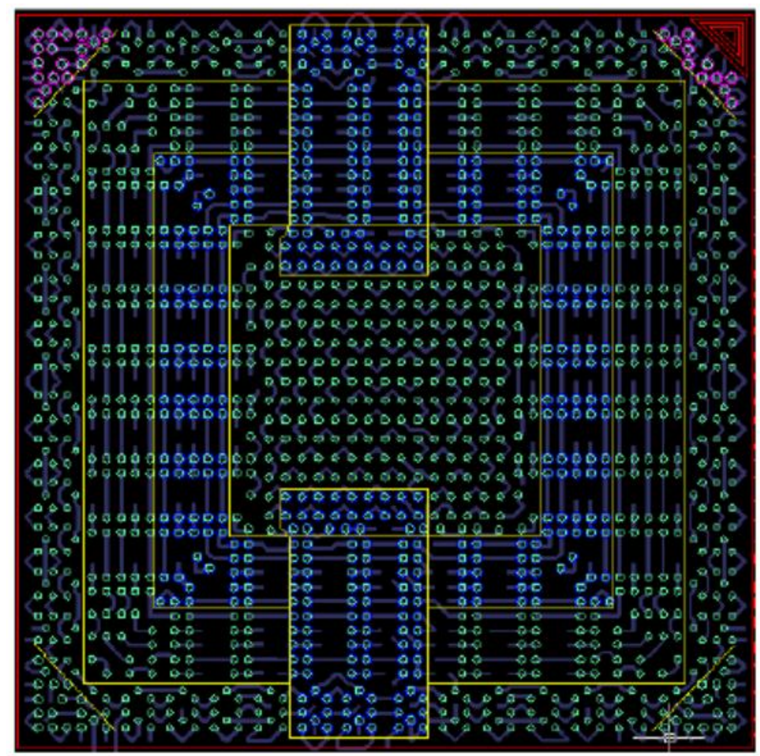
Example courtesy of Intel

Individual Electronic Package Example



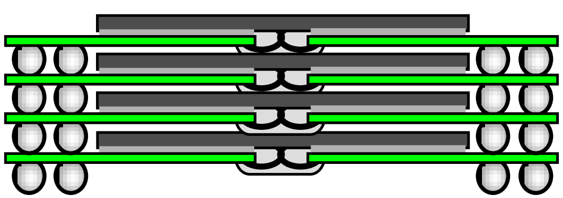


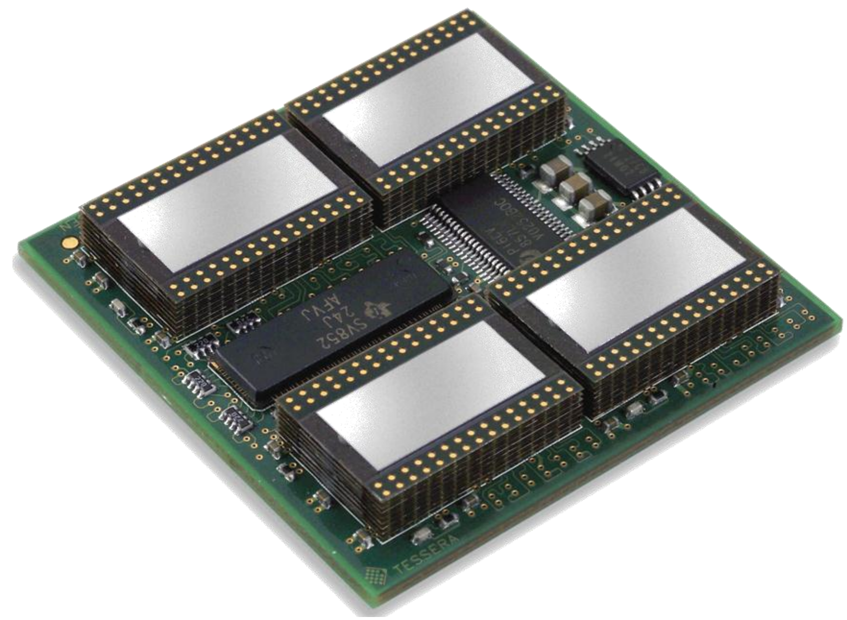




Electronic Module Examples

4 Layer Ball Stack Module





High Density Memory Module

Examples courtesy of Tessera

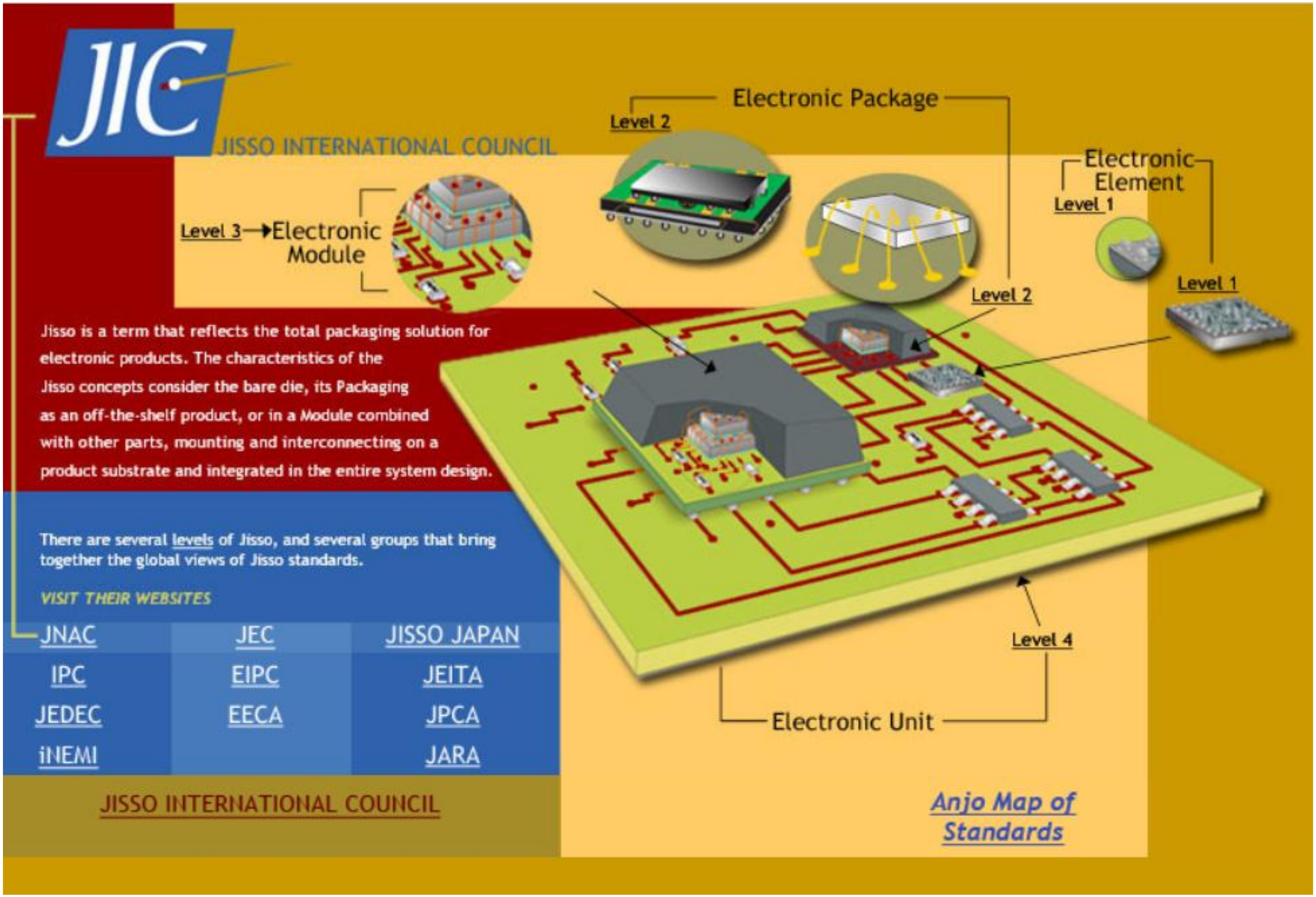
Electronic Unit Example

20GB Ruggedized Solid State
2.5 inch Flash Drive Assembly

Example courtesy of Tessera

Electronic System Examples

http://jisso.ipc.org/ on the IPC website



JISSO Council Proposal

1. New Terminology Proposal
   1) Needs of New Terminology
   2) Definition
   3) Objective(Needs for Standardization)
2. Classification

Current Understanding of MCM

MCM Concept in Japanese Companies (JEITA Survey results, 2001)

Sub-system

Module 8
Package 15

for

Multi - ICs 22
- Include Packages 8
- Not include Packages 16

Multi – components (Include passive comp.) 7

(Allow single chip?) 2

Semiconductor suppliers	11
Components suppliers	9
Set makers	13

Indefinite Concept

(a narrow sense - a wide sense)
- SiP,MCP also indefinite
- Other term(FCM,Hybrid IC, , ,) in a narrow sense

↓

Need a new generic term

New Terminology Proposal

Terminology:

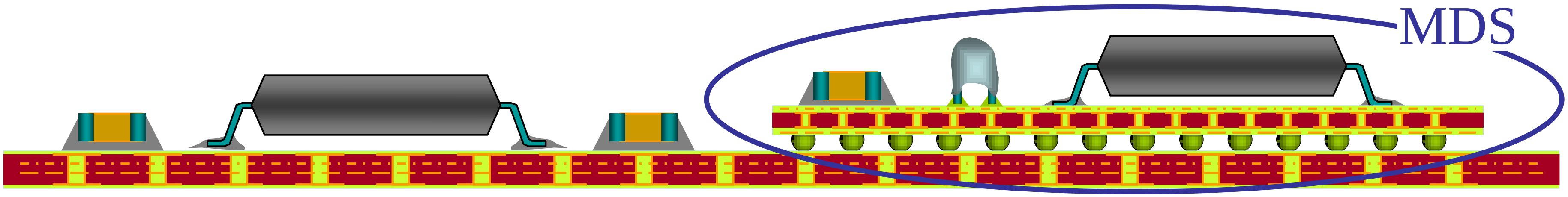
Multi Device Sub-assembly(MDS)

Definition:

The MDS is a sub-system which consists of multiple electronics devices including at least one integrated circuit. It is connected to a motherboard which functionally integrates it into a system. (A generic term which includes Hybrid IC/MCM/MCP/FCM/ FCP/SiP/SIMM/DIMM)

Objective:

Jisso Level 3 common standard between users and suppliers

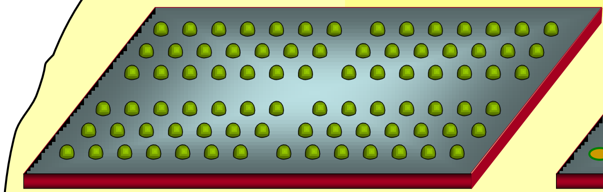


Classification of MDS

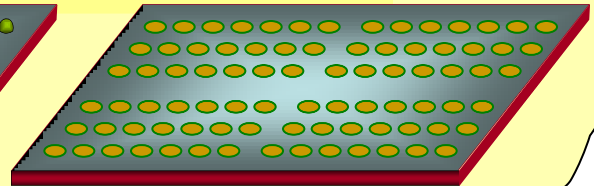
Prioritization	Category
1st	Terminal B(Ball) / L(Land) / Le(Lead) / C(Connector Pad) / P(Pin) / O(Others: Optic,Electromagnetic)
2nd	Terminal Connect Technology 1:Chemical(Solder/Conductive resin) 3:Contactless(Optic/Electromagnetic) 2:Mechanical(Connector/Socket)
3rd	Substrate Material C(Ceramic) / L(Laminate) / D(Deposit) / Si / O(others) + E(Embedded Passive)
4th	Devices 1(Same IC) / 2(Various IC) / 3(IC+Discrete and/or Passive)
5th	Devices Configuration P(on Plane) / S(Stacked) / F(Folded) / E(Embedded in Substrate)
6th	Interconnect Technology for IC Assembly W(Wire) / FC(Flip-chip) / Le(Lead) / B(Ball) / L(Land) / P(Plating) / M(Mixed)

1st-2nd Priority : Terminal / Connect Technology

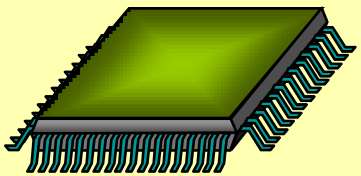
1. Chemical Contact



B(Ball)

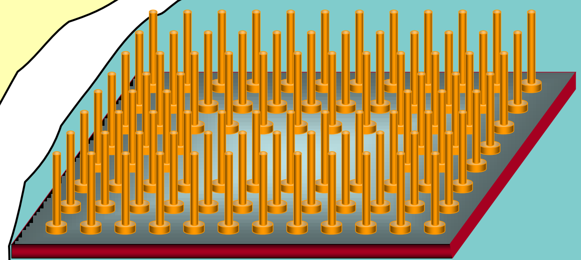


L(Land)

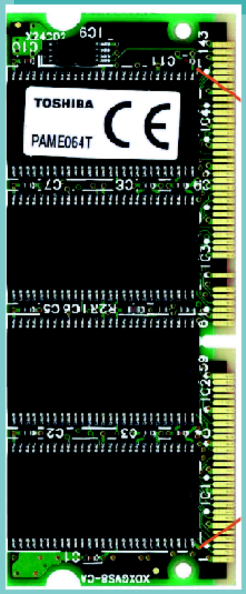


Le(Lead)

2. Mechanical Contact

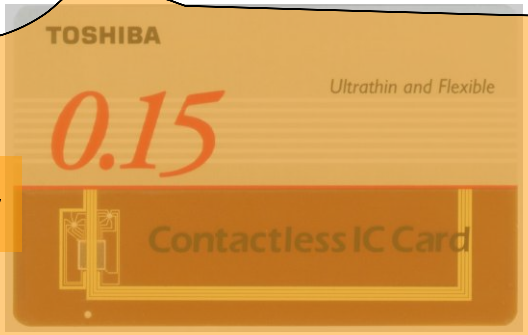


P(Pin)

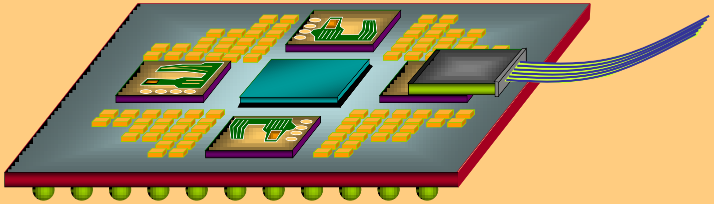


C(Connector Pad)

3. Contactless

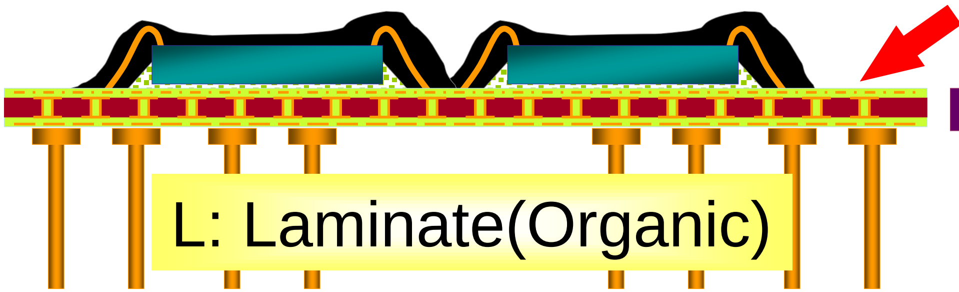


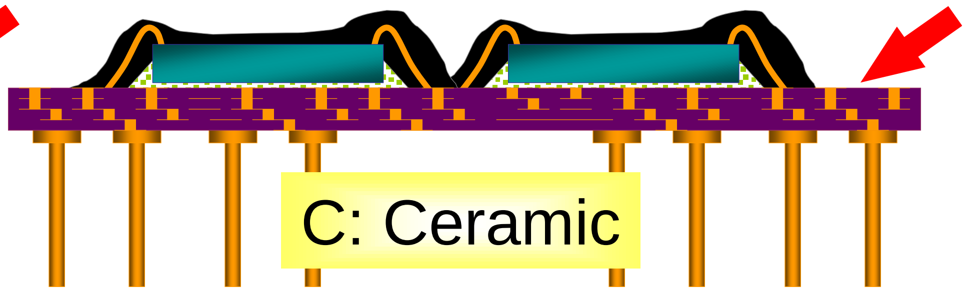
O(Others/Electromagnetic)

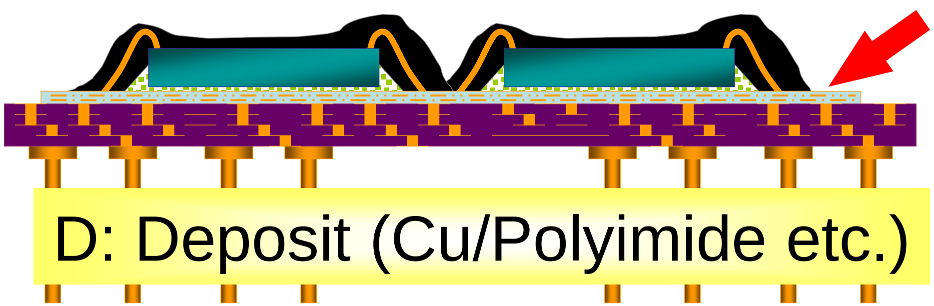


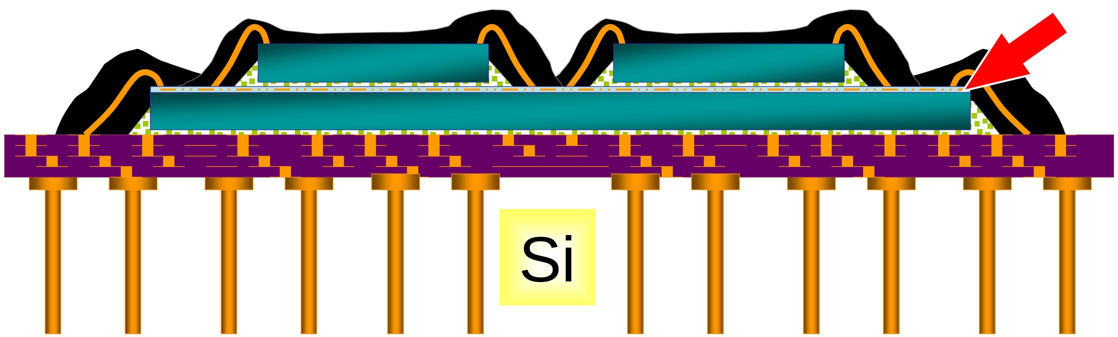
O(Others/Optical)

3rd Priority : Substrate Material





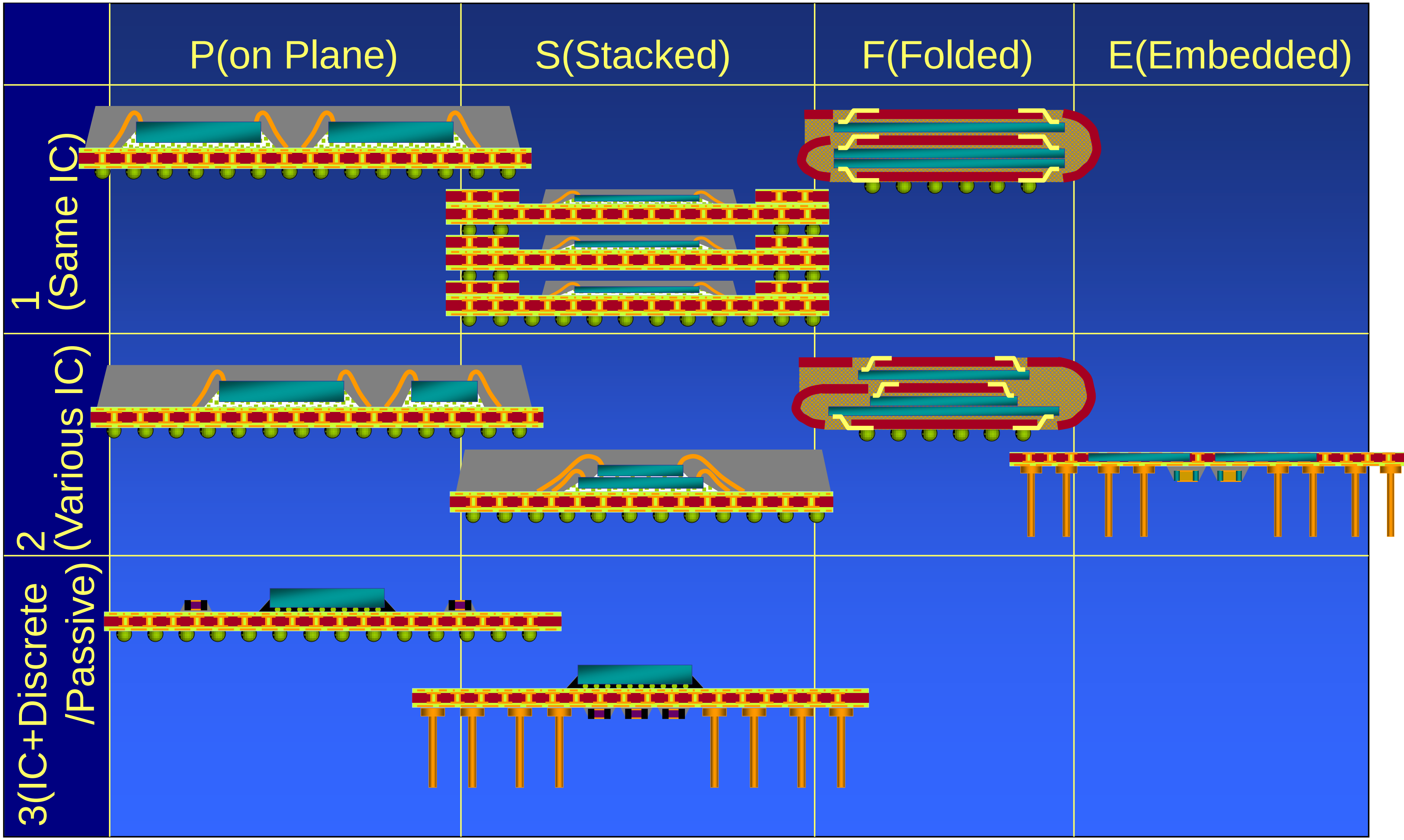




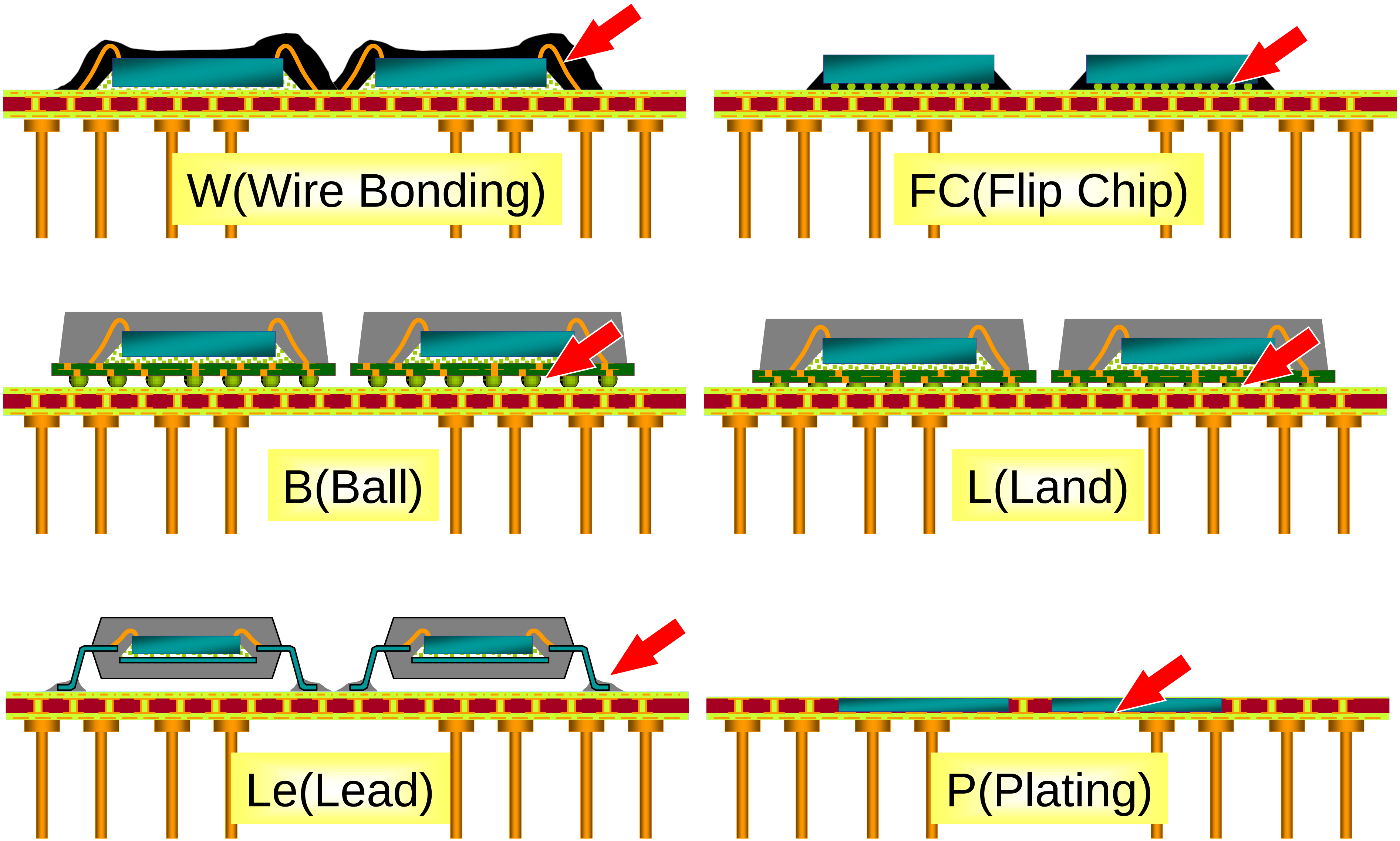
+E: Embedded Passive

e.g.
- Organic substrate w/ partial laminated high-k → LE
- Multi layered ceramic substrate w/ high-k layer → CE
- Si interposer w/ MIM Cap. → SiE
-
-

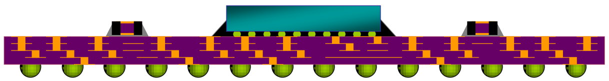
4th-5th Priority : Devices / Configuration



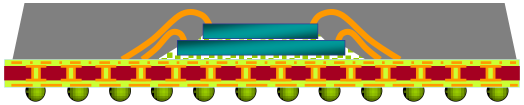
6th Priority : Interconnect Technology



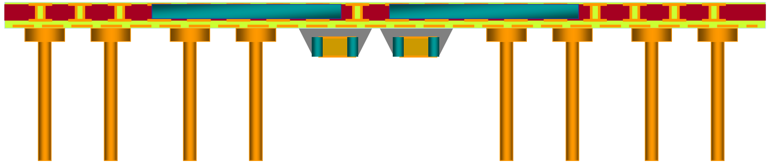
Typical Examples of MDS Classification



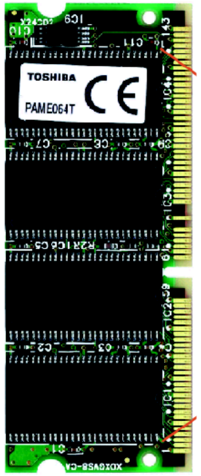
Transmeta Crusoe
"MDS-B1-C-3P-FC"



Stacked MCP for Mobile Phones
"MDS-B1-L-2S-W"

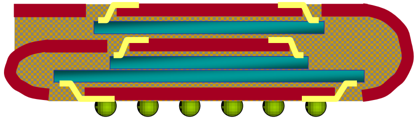


CPU+Chipset in Intel BBUL w/ decap
"MDS-P2-L-2E(3S)-P"



DIMM/SIMM

"MDS-C2-L-1P-Le"



Flash+SRAM in Tessera Folded Stacked
"MDS-B1-L-2F-Le"

Can Define/Classify Current/Published Products, but Hard to Understand.

Involvement through ISO and IEC

- The JIC promoted the concept of working with IEC and ISO standards in order to accomplish their mission.
- The mapping of standards to the "Total Packaging Solution" was an attempt to have all the building blocks in place in order to have technology become main stream
- Several JIC meetings were hosted by the IEC, however JIC is not an official group
- Countries submit resource documents and the are turned into International standards supported by COUNTRIES.
- In some instances these may become international Law due to cooperative effort.
- The IEC National committees just adopted the IPC-A-610 as the global Workmanship standard

Major Committees of Interest

- TC47 - Semiconductor Devices [JEDEC]
- TC91- Electronics assembly technology
  - Electronic Assembly Physical Characteristics
  - Design Automation for Electronic Assembly
- TC111 - Environmental standardization for electrical and electronic products and systems
- TC119 – Printed Electronics

IEC IPC JEDEC

IEC/PAS 62588

Edition 1.0 2008-09

PUBLICLY AVAILABLE SPECIFICATION

Marking and labeling of components, PCBs and PCBAs to identify lead(Pb), Pb-free and other attributes

INTERNATIONAL ELECTROTECHNICAL COMMISSION

Marking and Labeling of Components, PCBs and PCBAs to Identify Lead(Pb), Pb-Free and Other Attributes

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A PAS is a technical specification not fulfilling the requirements for a standard but made available to the public.

IEC-PAS 62588 was submitted by IPC/JEDEC and has been processed by IEC technical committee 91: Electronics assembly technology.

The text of this PAS is based on the following document: This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document

Draft PAS	Report on voting
91/767/PAS	91/783/RVD

Following publication of this PAS, the technical committee or subcommittee concerned will investigate the possibility of transforming the PAS into an International Standard.

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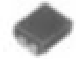
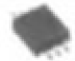
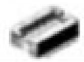
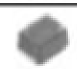
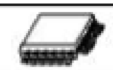
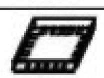
This PAS shall remain valid for an initial maximum period of 3 years starting from the publication date. The validity may be extended for a single 3-year period, following which it shall be revised to become another type of normative document, or shall be withdrawn.

IPC JEDEC

test methods suitability

	Types and terminals of device				Rapid temperature change test					Cyclic bending test	Cyclic drop test	Mechanical shear fatigue test
	Terminals		Number of terminals	Examples	Pull test	Shear strength test	Torque shear test	Resistance measurement	Monotonic bending limit			
General electronics components	Electrodes on 2 sides (bent leads)		2	Tantalum capacitor, inductor	-	A,B	-	-	-	-	C	-
	Electrodes on 3 sides		2	Rectangular chip resistor/film capacitor	-	A,B	-	-	-	-	C	-
	Electrodes on 5 sides (including cap)		2	Laminated capacitor, thermistor, laminated inductor, fuse	-	A,B	-	-	-	-	C	-
	Multi terminals (terminals on sides)		4 or more	Resistor array, capacitor array	-	A,B	-	-	-	C	C	-
	Gull wing – 1		4 or more	Transformer	A,B	C	-	-	C	-	C	-
	Gull wing – 2		Up to 6	Switch	-	B	A,B	-	-	-	C	-
	Gull wing – 3		4 or more	Connector	-	A,B	A,B	-	C	-	C	-
	Electrodes on bottom		2	Inductor, tantalum capacitor	-	A,B	B	-	-	-	C	-
	Round electrode (including cap)		2	MELF capacitor/resistor /fuse	-	A,B	B	-	-	-	C	-
Semiconductor devices	Leads on two sides (bent lead)		2	Diode	-	A,B	C	-	-	-	C	-
	Gull wing leads		3 to 6	Small transistor	C	B	C	-	-	-	C	-
	Gull wing leads J-lead packages		6 or more	QFP, SOP J-lead	A,B	-	-	C	C	C	B	B
	Non-lead		6 or more	QFN, SON	-	-	-	A,B	C	B	B	B
	Ball electrodes on bottom		Multiple	BGA, FBGA	-	-	-	A,B	C	B	B	B
	Electrodes on bottom without ball		Multiple	LGA, FLGA	-	-	-	A,B	C	B	B	B

APEX EXPO IPC 2013

FR4
IPC- 4101 slash sheet to SolderTemps

FR4 Material Properties					
Laminate Properties	Exposure Level A	Exposure Level B	Exposure Level C	Exposure Level D	Comments
Standard Nomenclature	4101/126 4101/130	4101/99 4101/128	4101/101 4101/127	4101/124 41010/125	Brominated Un-Bromin.
Tg	170	150	110	150	
Td	340	325	310	NA	
Solder float extremes 260ºC 288ºC 300ºC	30 15 2	30 5 NA	30 5 NA	NA	
CTE in X&Y	14 – 18 PPM/ºC	14 – 18 PPM/ºC	14 – 18 PPM/ºC	14 – 18 PPM/ºC	
CTE in Z A alpha1 B alpha2 C 50-260ºC	60 max 300 max 3.0% max	60 max 300 max 3.5% max	60 max 300 max 4.0% max	NA	
Copper Adhesion	0.7 Newton/MM	0.7 Newton/MM	0.7 Newton/MM	0.7 Newton/MM	
Copper Ductility	17µm 5% min	17µm 5% min	17µm 5% min	17µm 5% min	
Moisture Content	0.5% max	0.5% max	0.5% max	0.8% max	
End Usage					
Benign end use	OK for use	OK for use	OK for use	OK for use + durability	
Median end use	OK for use	OK for use Plus test	OK for use + durability	OK for use + durability	
Severe end use	OK for use + quality	OK for use + durability	OK for use + durability	NA	

What Have We Learned ?

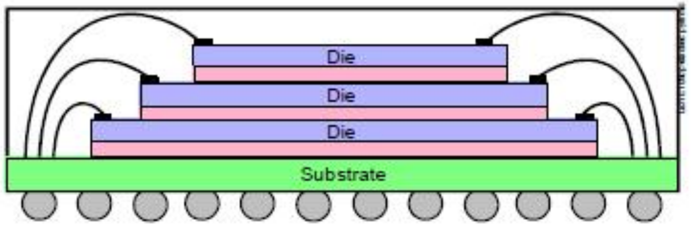
- Cooperative effort can make a difference
- Communication is key
- Good marketing helps sell ideas
- Publish or perish
- Users feel comfortable with choices to meet their needs and application
- There needs to be a focus group supported by organizations ready to set direction and to create a mission and Status and Action Plan.

Present Day Technology and Implementation

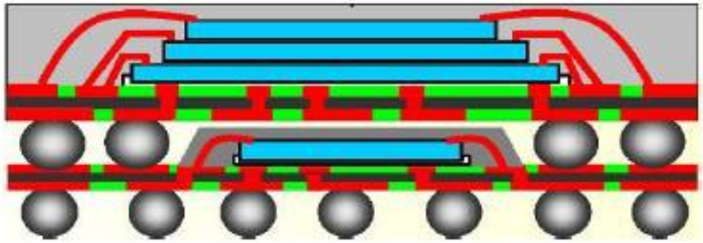
- Lots of activity in the last few years
- Much of it was driven by the visionary leaders
- Of all the end-use environments , the main drivers have been the Commercial products
- The supply chain becomes more convoluted and more difficult to manage
- The printed board mounting platform has become very complex and OEMs want assurance of reliability
- Trade associations work to help develop new test methods and techniques for product life

3D Package Technology

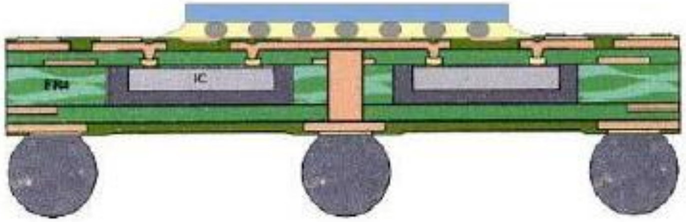
- **Stacked Die in Package**
  – Standard wire bond assembly process
  – Billions of packages shipped annually (memory)
  – Represents > 15% of semiconductor die area



- **Package-on-Package**
  – Hundreds of millions ship annually (logic and memory)
  – Advantage in logic/memory test separation

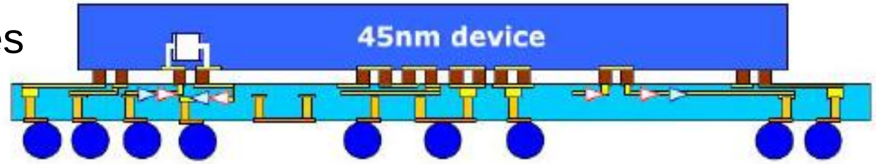


- **Embedded Die in PCB**
  – Limited production since 2005
  – Recent renewed interest (PCB and wafer-based)



Source: Imbera

- **Die/Wafer Interconnection Using TSV**
  – Ultimate SiP in size and performance
  – TSV production to date only with non-3D structures
  – Face-to-face production without TSV in 2007

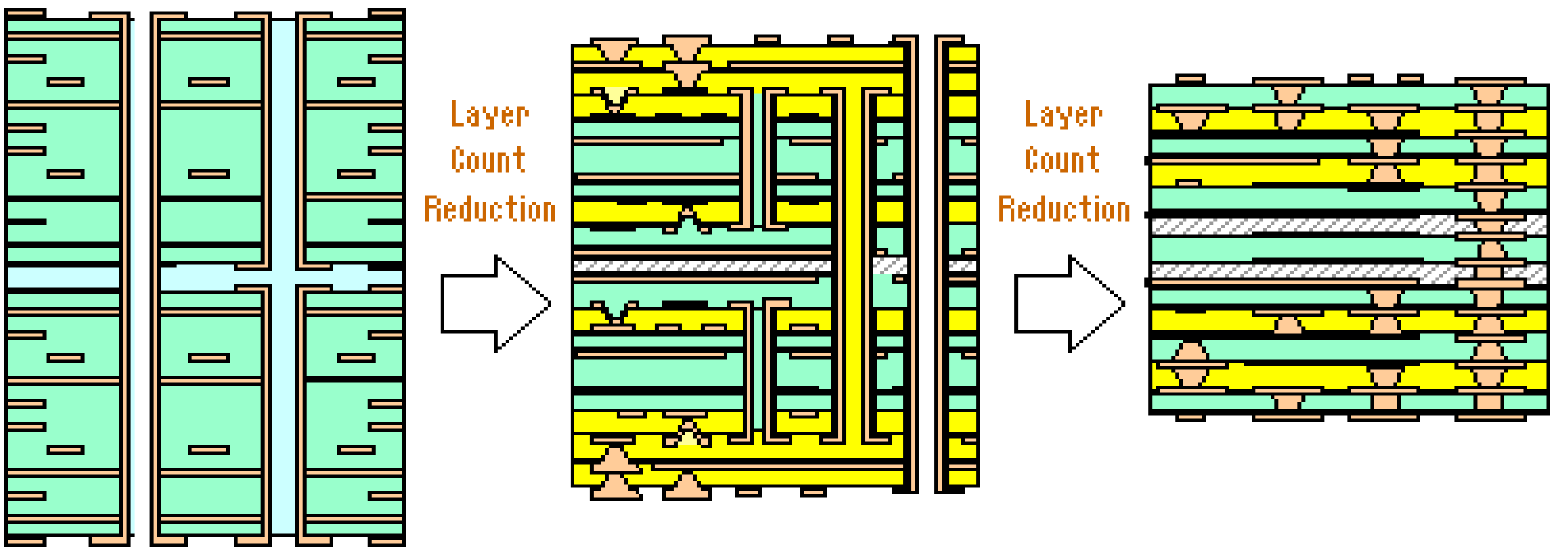


Source: ST

Complements of Prismark

Substrate Technology Evolution

MV1 Sequential lamination structure	MV3 Sequential build-up structure	MV5 Full stacked via structure



	MV1	MV3	MV5
Wiring Density	1	2	3
Wiring Length Ratio	1	0.70	0.60
	1000pin BGA mounting	2500pin BGA mounting	4000pin BGA mounting

Establishing Focus

- **Reliability** is the ability to function as expected under the expected operating conditions for an expected time period without exceeding expected failure levels
- **Proof of Performance**
- ***End item reliability can only be determined by the OEM.***
- ***PWB Fabricators often have little or no visibility to end item requirements.***

- **Quality** is the ability to produce the product in the manner specified by the customer in the documentation package provided including any test or legal requirements
- **Meets Requirements**
- ***OEM's define PWB quality requirements necessary to meet their reliability needs***.

Issues to Consider

- ***Die***

  Electrical load: voltage, current, power, surge,

  Environmental load, die itself and interaction within package

- ***Package***

  Environmental and mechanical load Internal die interconnection
  Package type: Leaded/leadless, BGA, CSP, WLP, Flip chip

- ***PWB***

  Materials (FR-4, Polyimide), Lay up (copper, HDI), Finish PTH, Microvia, Via in pad, Embedded Components

- ***Assembly***

  Electrical, environmental (thermal, mechanical, chemical, etc)

- ***System***

  Product specific

All of these are OEM design considerations.

Collision of Quality and Reliability Requirements

- OEM products must survive 2 primary environments:
  1. Product Assembly (Reflow/wave & rework)
  2. Field Service (thermal cycles & shock/vibration)

- Traditional PWB Quality Requirements are primarily measurements used for PWB fabrication process validation but have limited use for determining reliability.

Modern Reliability Challenges

- Components are much smaller than they were a few years ago.
- Components are placed more densely on PWBs.
- PWBs go through more severe reflow processes, and often multiple times.
- Lead-Free solder increases processing temperatures
- As a result PWB designs have changed
  - PWB features are very small
    - High aspect ratio vias
      - (old designs seldom higher than 5:1, today can be 10:1)
    - *Many* more vias per pwb than in the past
  - Laminate materials must be more robust
    - Assembly temperatures are higher
    - Must have low z-axis expansion for greater via life.

New Evaluation Methods

- **Reliability**
  - A- Thermal shock
  - B- Vibration
  - C- Thermal Cycle
  - D- HAST
  - E- IST
  - F- Pressure Vessel
  - G - CAF
  - H - Whisker Growth
  - J – Assembly Simulation
  - X – System Specific
- **Quality**
  - **Visual Inspection**
    - Visual 10X 40X
    - Dimensional
    - Microsection
    - Continuity/ In-Circuit
    - Customer Specific
    - PCQRR
  - **Durability -New**
    - HATS
    - IST
    - Solder Float
    - Solder Reflow

Test PWBs 150˚ C

Microvias 190˚ C

Polyimide 210˚ C

Mounting Substrate

The product is as strong as the weakest link – Have lower requirements for sub assemblies makes no sense.

Product Application per end use					
End-use Environment	A-Interposer	B-Module	C-Portable	D-Product	E-Back Plane
1-Consumer	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150
2-Computers and Peripherals	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150	100 cycles @ 150
3-Telecomm	250 cycles @ 150	250 cycles @ 150	250 cycles @ 150	250 cycles @ 150	250 cycles @ 150
4-Commercial Aircraft	350 cycles @ 150	350 cycles @ 150	350 cycles @ 150	350 cycles @ 150	350 cycles @ 150
5-Industrial and Automotive Passenger Compartment	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150
6-Military (ground and shipboard)	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150
7-Space	1400 cycles @ 150	1400 cycles @ 150	1400 cycles @ 150	1400 cycles @ 150	1400 cycles @ 150
8-Military Aircraft	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150
9-Automotive (under hood)	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150
10- Bio Medical & Life support	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150	500 cycles @ 150

RoHS = 260° C

Tin/Lead = 230° C

Assembly Process Simulation

Product Application per end use					
End-use Environment	A-Interposer	B-Module	C-Portable	D-Product	E-Back Plane
1-Consumer	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
2-Computers and Peripherals	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
3-Telecomm	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
4-Commercial Aircraft	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
5-Industrial and Automotive Passenger Compartment	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
6-Military (ground and shipboard)	6X230°C	6X230°C	6X230°C	6X230°C	6X230°C
7-Space	6X230°C	6X230°C	6X230°C	6X230°C	6X230°C
8-Military Aircraft	6X230°C	6X230°C	6X230°C	6X230°C	6X230°C
9-Automotive (under hood)	6X260°C	6X260°C	6X260°C	6X260°C	6X260°C
10- Bio Medical & Life support	6X230°C	6X230°C	6X230°C	6X230°C	6X230°C

Issues Facing Designers

Complex Technologies

- Different materials & technologies mounted on the same board.

➢ **Embedded Active Devices**

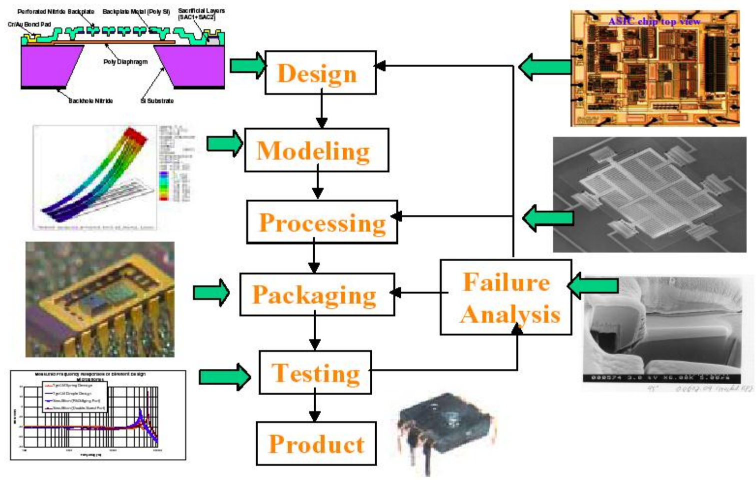
➢ **Embedded Passive Devices**

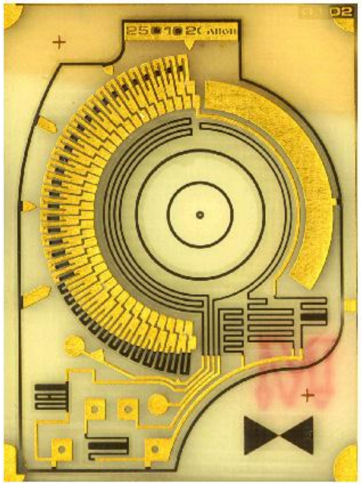
➢ **MEMS**

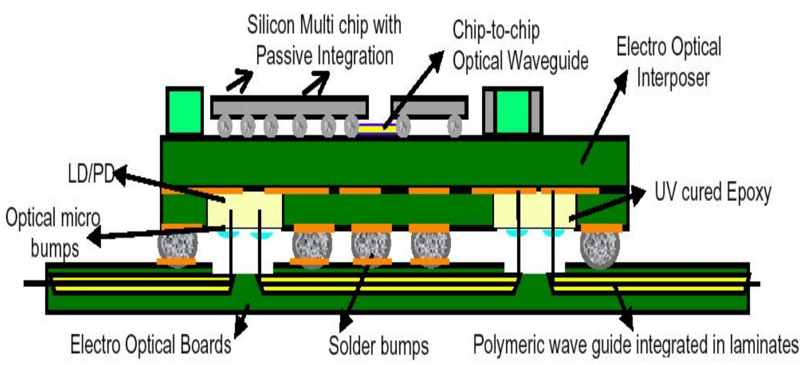
➢ **Optoelectronics**

➢ **SiP**

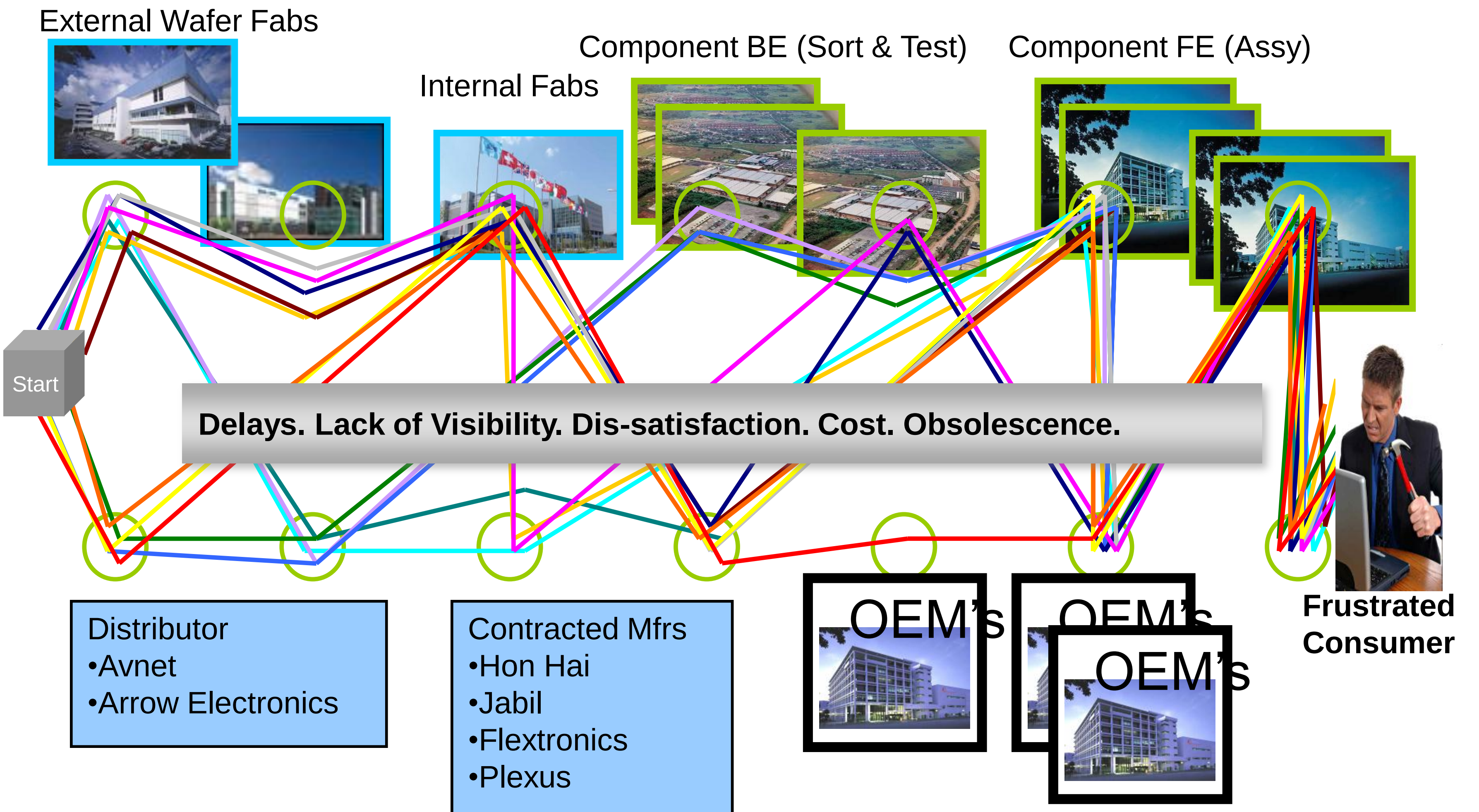
➢ **Sensors, Others**





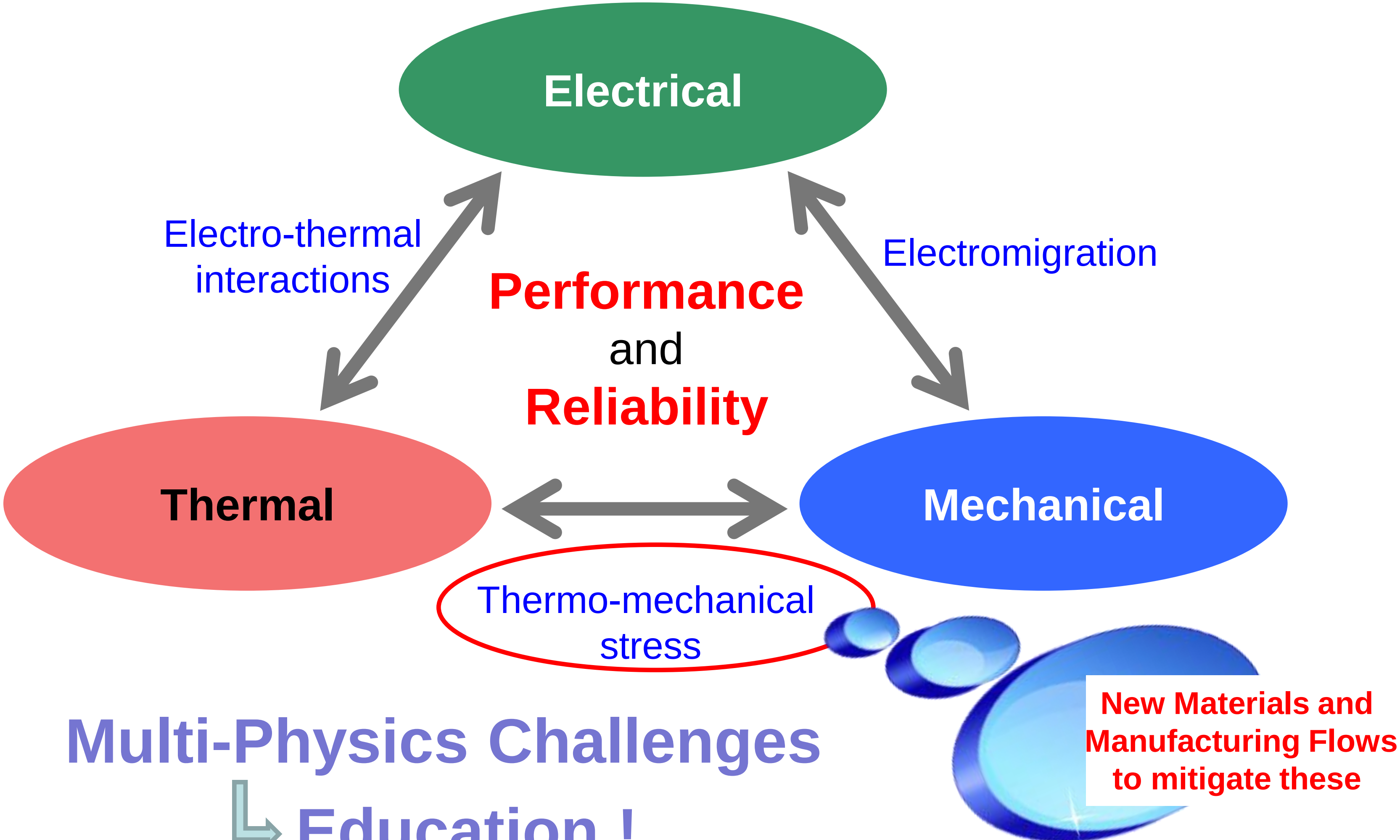


Tech Supply Chain: A Complex Ecosystem



Source: Avnet and UBS

3D Integration Challenges



Multi-Physics Challenges

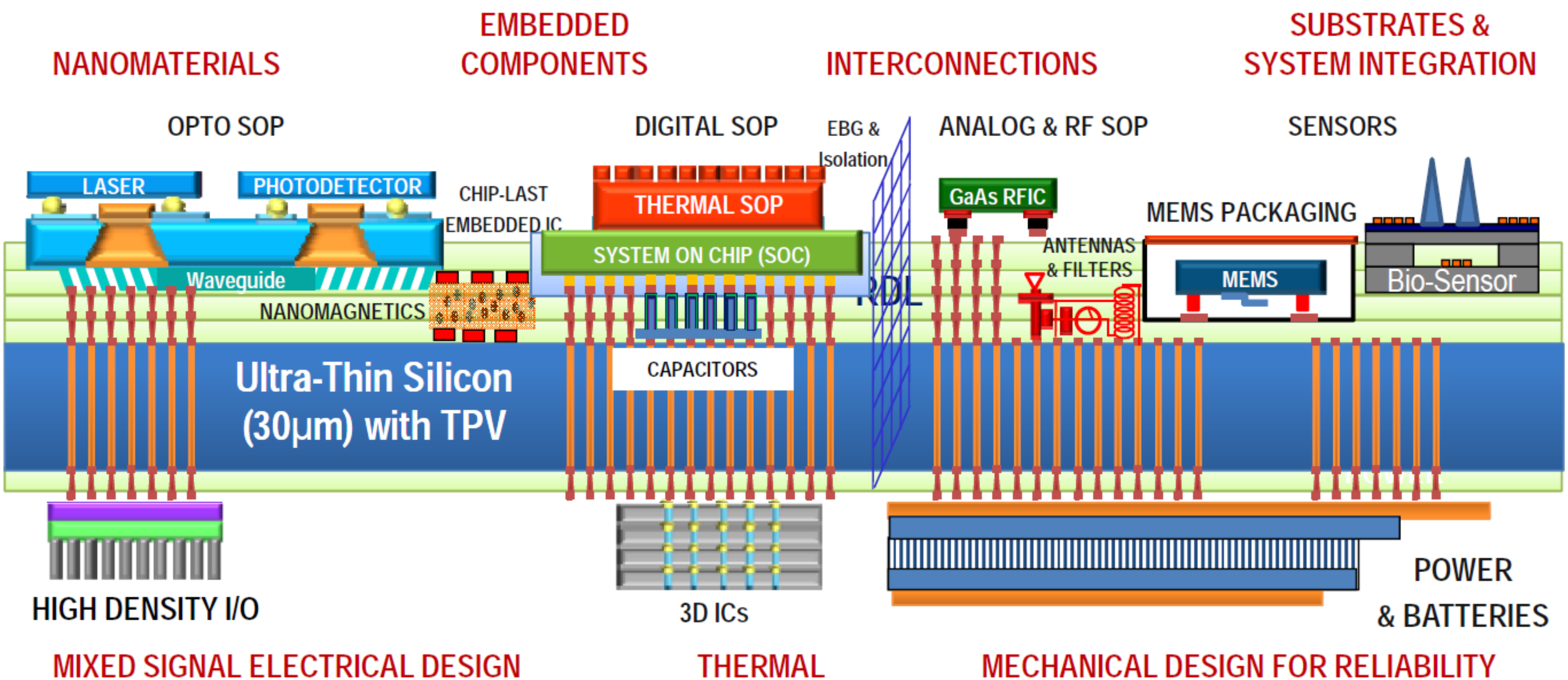
↳ **Education !**

↳ **EDA, IC Designers**

Ongoing Efforts to Accelerate 3D Rollout

- 3D development efforts at industry consortia
- SEMI & Si2 drive manuf./design standards
- GSA’s 3D IC Working Group ongoing since 2009
- JEDEC: Wide I/O Standard, rev 1 released in Jan
- HMCC released first interface spec issued in Aug
- Many technical books
- **Little or no coordination**

Tomorrow's 5.5D System Integration



Source: Rao Tummala, Georgia Institute of Technology,
3D Systems Packaging Research Center,

Conclusions

- Get involved and let your needs be heard
- Study implementation standards
- Identify reliability issues with case studies
- Participate in email forums with colleagues
- Understand the needs of the customer whose requirements are in the contract.
- Comprehend the meaning of manufacturing instructions (notes) on documentation
- Know the methods and techniques of Data Transfer from Design to Manufacturer