Reliability Performance of Very Thin Printed Circuit Boards with regard to Different any-Layer Manufacturing Technologies

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Abstract
The next generation of smart phones will demand very thin multi-layer boards to reduce the product thickness again. This paper shows three different manufacturing approaches, which can be used for very thin any-layer build-ups. The technological approaches are compared on reliability level – the any-layer copper filled micro-via technology which is to be considered as state of the art technology for high end phones and the ALIVH-C/G technology that is well established in Japan. A test vehicle design featuring test coupons for comprehensive reliability test series has been defined as target application for investigation. The applied test vehicle build-ups comprise an 8 layers build-up with total board thickness below 500 µm. The first test vehicle is based on an any-layer HDI build-up including copper filled stacked micro via structures, the second test vehicle features an 1+6+1 ALIVH-C build-up comprising an outer HDI prepreg layer while the third test vehicle is built in ALIVH-G technology featuring a full ALIVH build-up.

The influence of the applied manufacturing technology on the reliability performance of thin PCBs is evaluated based on these three test vehicle build-ups.

To cover the behavior during SMD component assembly the produced samples are subjected to reflow sensitivity testing applying a lead free reflow profile with a peak temperature of +260ºC. Failure occurrence and the observed failure modes are evaluated and compared.

In parallel a temperature cycling test is conducted on the test vehicles in a temperature range between -40 ºC and +125 ºC in order to evaluate the thermo mechanical reliability of the test vehicles with regard to the manufacturing technology.

In order to characterize the reliability aspects influenced by electrochemical migration phenomenon the different samples are subjected to a HAST test at +130 ºC with 85 % humidity level.

The results obtained from reliability testing are summarized and compared within this paper. The identified relations between manufacturing technology and the reliability performance of the test vehicles are shown; strengths as well as weaknesses of the applied any-layer technologies are identified and summarized.

Introduction

When IBM introduced the IBM Simon device this marks the beginning of the smart phone area [1]. Combining phone functions with the functionality of a PDA is a remarkable milestone for our communication age. However while being very innovative the device was not really suitable for one's waistcoat pocket. With a total weight of 510 g and a thickness of 38 mm it was confined to a live in the briefcases of business executives. Since that time the smart phone OEMS have quite clearly recognized that next to functionality the handling behavior and the ergonomics of the smart phone device belong to the decisive criteria for the customers. Based on selected examples the subsequent Figure 1 shows how the smartphone dimensions evolved since Simon appeared. While the basic length and width of the devices just changed with regard to functional and aesthetic trends the reduction of the thickness of a smart phone device became a kind of race with the OEMs as competitors. As the figure shows the thickness of a smart phone device has been reduced by a factor of almost 6, with the October 2012 champion, the Finder X907 device of Chinese OEM Oppo. This Android driven device claims to have a nominal thickness of only 6.65 mm. However there will not be much time to enjoy the position at the cutting edge since another Chinese OEM, company ZTE, already announced to introduce a device with 6.2 mm within the next months.

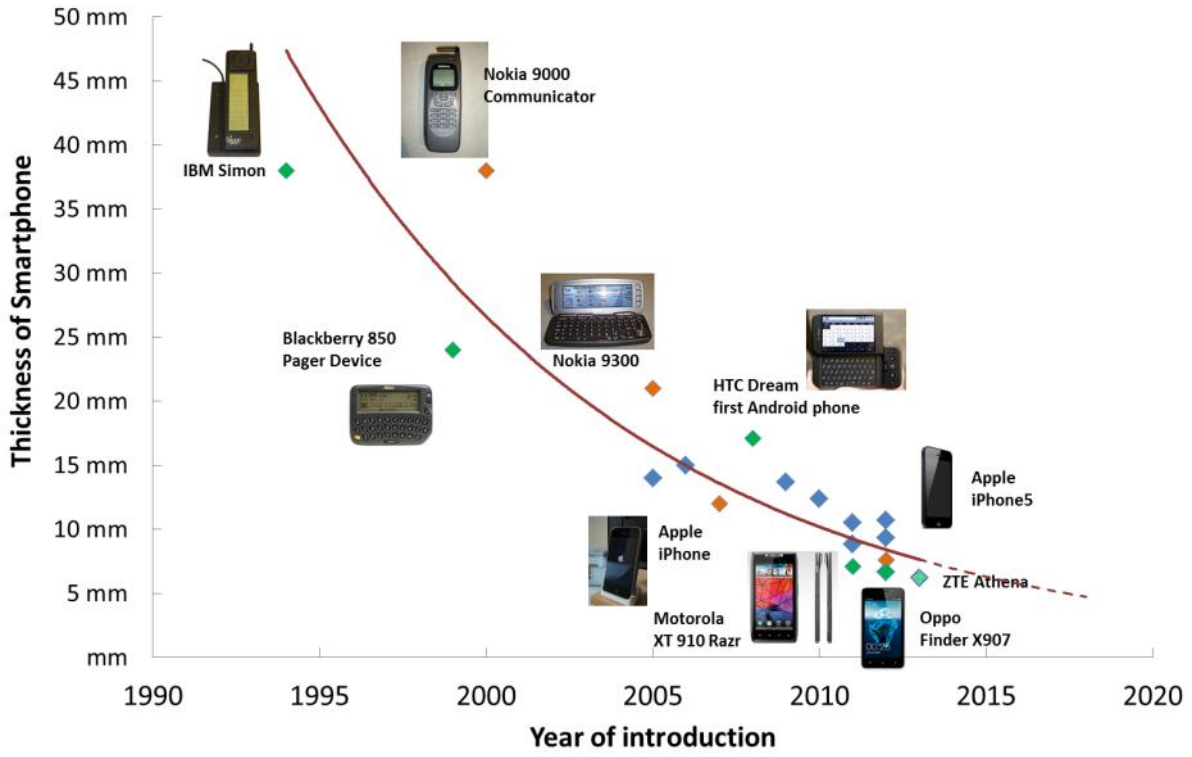

Figure 1: Thickness of smart phone devices with regard to the year of introduction

In order to achieve this reduction the smart phone designers quite neatly used all the possibilities that the always ongoing miniaturization trend in industries offered to them. It is obvious that for the producers of printed circuit boards (PCBs) for smart phone devices it has been necessary to adopt for that demand and to reduce the thickness of their PCBs significantly.

The period around the introduction of the first smartphones coincides with the breakthrough of the HDI technology in PCB making [2]. The first smartphones often featured 8 layer rigid boards, with a stack up made of 1080 fabric style prepregs and 25 µm copper layers. While the layer count is similar for the boards of today's high end phone, again the thickness changed significantly: From more than 1,2 mm in the year 2000 to approx. to approximately 600 µm in 2011, while the target for a rigid 8 layer board in 2013 has been set to 400 µm.

Experimental set up

In order to evaluate the production process and performance of very thin rigid PCBs within this study test vehicles in three different technological approaches have been build. The test vehicles then were subjected to a reliability test program comprising a MSL Level 3 reflow test, a thermo cycling test with lower temperature level of -40ºC and an upper temperature level of +125ºC at 2 cycles per hour and a Highly Accelerated Stress Test (HAST) at a temperature level of +130ºC with a humidity level of 85 %.

Processing technologies ALIVH and HDI/FV

To build the rigid 8 layer board with a total thickness below 500 µm two PCB production technology have been considered. On the one hand the High density Interface (HDI) technology combined with micro via filling has been chosen in order to be able to realize the implementation of stacked via designs (HDI/FV) [3], on the other hand the proprietary Any-layer Interstitial Vias Hole (ALIVH) technology that was introduced in 1996 by Panasonic/Matsushita and which is well established in Japan. The HDI/FV process features the traditional process flow with lamination steps, mechanical and laser drilling and subsequently establishing the contacts between the layers by electroless copper deposition and electrochemical plating. Also the filling of vias is done in an electrochemical plating process, while the ALIVH process is based on printing a conductive copper paste into pre-drilled holes of the prepreg layers to achieve the required electrical connection from one copper layer to the other. A more detailed description of the process has been given by Holden in the HDI Handbook [4]. A schematic view of the ALIVH process (Any-layer Interstitial Via Hole) is shown in Figure 2. ALIVH is a registered trademark of Panasonic Industrial devices.

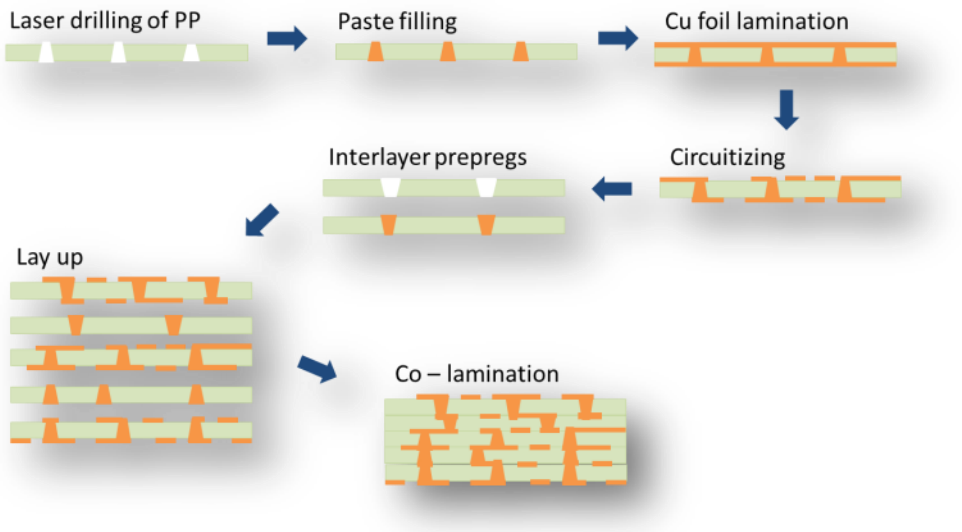

Figure 2: Schematic description of process flow at ALIVH PCB production process

Design and Stackup of test Vehicles

For the targeted rigid 8 layer PCB test vehicle a test design used regularly for reliability tests and material qualification issues at AT&S was selected. The test vehicle comprises several coupons for electrical and reliability tests with an 8 layer build-up. With regard to the defined production technologies slight modification within the design of the single part numbers had to be made, however great care was taken to assure the comparability of the HDI and ALIVH test vehicles. Figure 3 shows the built test board and the corresponding test coupons used for the further tests within the reported work.

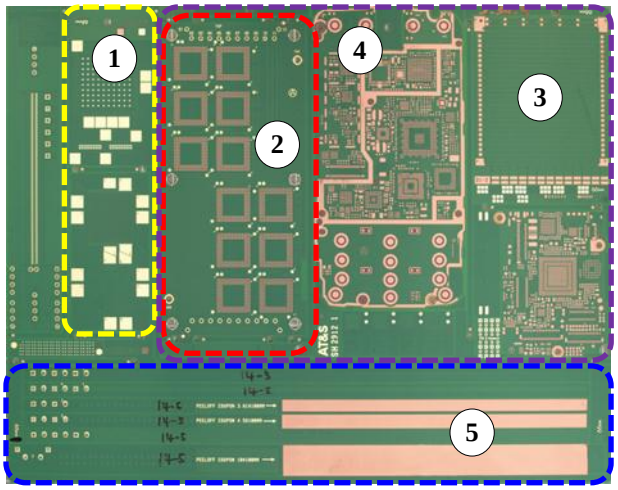

Figure 3: Test vehicle design and corresponding test coupons

Stack up and applied material

For the reported work three different test vehicles with different build-up approaches have been defined. As Table 1 shows there is one HDI build-up, one full AILIVH-build-up (ALIVH-G) and an ALIVH-C build-up where layer 2 to layer 7 are manufactured in ALIVH technology and the two outer layers are then in a subsequent process step add in HDI technology. The Expected Thickness column shows that thickness value for the board as it is calculated during the PCB design stage.

Since the target applications this study is based on are from the mobile devices segment all used dielectric materials have been chosen from the standard materials which are well introduced in PCB mass production. It was mandatory for all selected materials to be halogen free (HF).

Table 1: Built test vehicles and expected total board thickness

Test Vehicle	Technology	Build-up	Dielectric Material	Expected thickness [µm]
TV1	HDI/FV	3-2-3	HF FR4	471
TV2	ALIVH-C	1-A6-1	Low Flow HF FR4	459
TV3	ALIVH-G	A8	HF FR4 Low Flow HF FR4	448

Relevant material and build-up properties of the applied dielectric materials are given in Table 2. For copper layers standard 12µm copper foil with single sided, standard treatment has been applied.

Table 2: Properties of applied Dielectric material

Property	Low Flow FR4 PP	FR4 standard PP	FR4 standard CCL
Halogen free	yes	Yes	yes
Cloth style	1037	1037	1x1067
Resin content [%]	73	70	65
Thickness [µm]	40	45	50
Copper thickness [µm]	-	-	12
D_k	4,3	4,1	4,2

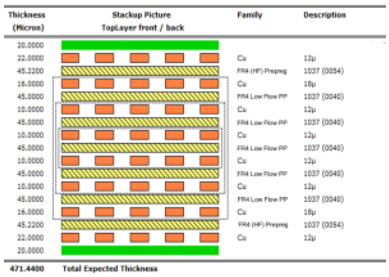

Figure 4: Build-up TV1

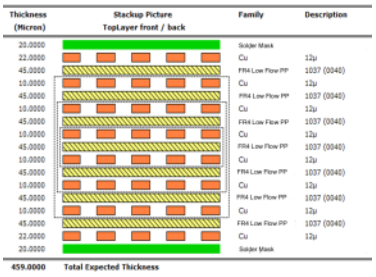

Figure 5: Build-up TV2

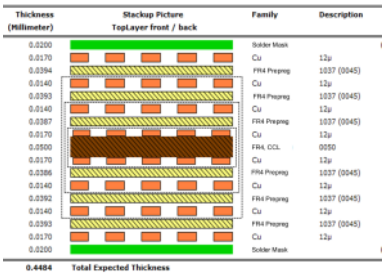

Figure 6: Build-up TV3

Experimental Procedures

Board Thickness measurement

The thickness of the board was measured at two positions of the board as shown in Figure 7. The measurement was done manually with a digital micrometer gauge with a precision level of 0.001 mm at ambient conditions. The measurement was done for a random sample of 15 TVs from the production lot. While position A represents an area with lower overall copper content in the build-up, position B correspond to an area of the built test vehicle which features a relatively high copper content in the stack-up structure.

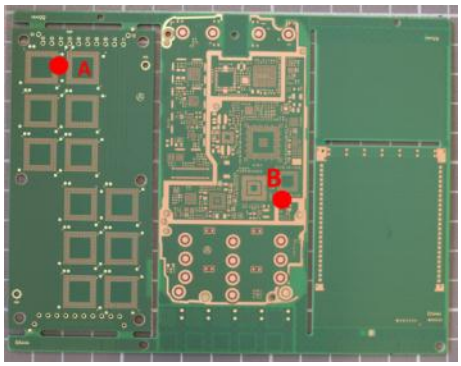

Figure 7: Positions for board thickness measurements

Reflow performance

The reflow testing was done in accordance with IPC/JEDEC J-STD-020D1T [5]. Applied moisture sensitivity level was level 3. The sample size was 10 test vehicles of each test vehicle type. Conditions for preconditioning are given in Table 3. The applied lead free reflow profile is shown in Figure 8.

Table 3: Preconditioning for IPC/JEDEC J-STD-020D1 MSL3acc level reflow testing

Moisture sensitivity level	MSL3
Conditioning/Drying	24 h / 125ºC
Pretreatment MSL3	
Temperature	60ºC
Moisture duration	60%
Reflow Cycles	40 h

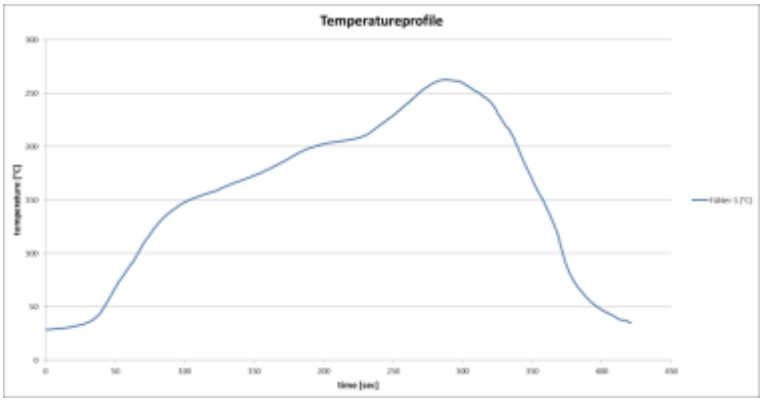

Figure 8: Lead free reflow profile applied for reflow sensitivity testing

Thermo cycle test

The thermo cycling of the samples has been done in accordance with JEDEC JESD 22-A104D [6], Test Condition G,2,C . Parameters are given in Table 4. The test on bareboard level has been carried with a designated daisy chain coupon for all three test vehicles TV1, TV2 and TV3. Resistivity of the daisy chain structure at each sample was checked at defined checkpoints during the test duration. For the bareboard configuration in total 8 coupons of each test vehicle type have been tested. The test is considered as passed if after 1000 temperature cycles the change of resistivity of the daisy chain structure is within the limits of 10%.

Additionally 4 populated samples each have been tested for TV2 and TV3. The populated sample was assembled with 12 CTBGA288 dummy components (see Figure 10). Each of the components during the test was monitored online by an event detector device. Test is considered as passed if no failure at a monitored structure is identified.

Table 4: Temperature cycling test parameter setting

Parameter	Level
Temperature low	-40 ºC
Soaking time at low	5 min
Temperature High	+125 ºC
Soaking time at high	5 min
Cycles per hour	2
Total cycle count	1000

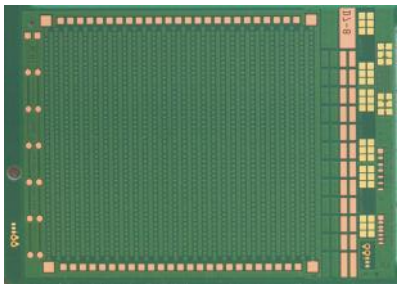

Figure 9: Bareboard daisy chain coupon for thermo cycling

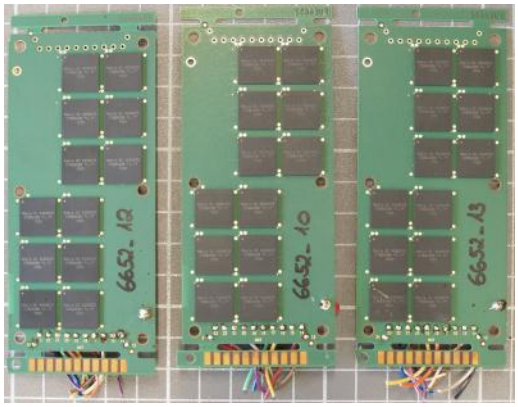

Figure 10: Assembled coupons (TV1) for thermo cycle testing

Highly Accelerated Stress Test (HAST)

HAST testing was done in accordance with JEDEC JESD 22-A110C [7]. The HAST test provides four process parameter, which are temperature, humidity level, applied bias and duration. For the current test the following parameter set was applied. For pre-treatment the samples have been thermo cycled for 5 times between -40ºC to +125ºC, then stored for 48 hours at 60ºC and 60% humidity level. Last step of preconditioning for the HAST test have been 5 lead free reflow cycles with +260ºC peak temperature.

For the actual HAST test then the parameter set given in Table 5 has been applied.

Table 5: Parameter set applied for HAST testing

Parameter	level
Temperature	130ºC
Humiditiy	85% r.h.
Bias	3,5 VDC
Test duration	120 hrs

The used test coupons provide structures for via to via testing (1 structure per coupon), via to plane testing (1 structure per coupon) and comb structures (1 comb structure per layer) as shown in Figure 11 and Figure 12 respectively. In total 8 coupons per part number were tested. All test structures have been monitored continuously during the test period, the results have been recorded. As failure criterion at each of the tested structures a drop of resistivity below a value of 10^6 Ohm was considered.

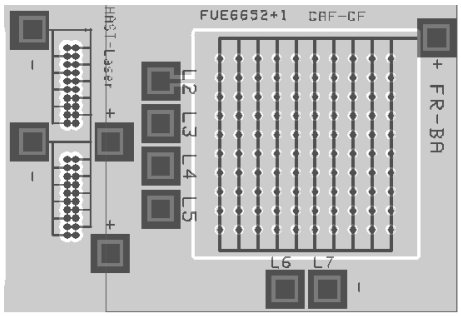

Figure 11: Via2Via and Via2plane test structures of HAST test coupon

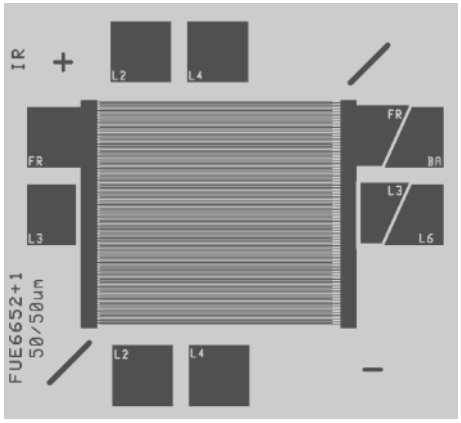

Figure 12: Comb structure, Front layer of applied HAST test coupon

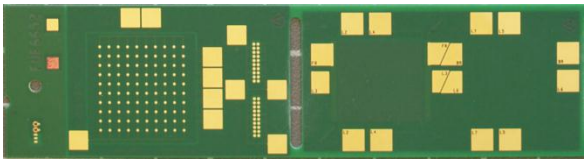

Figure 13: Thinboard HAST test coupon

Results

Built test vehicles and board thickness

After pressing the built test vehicles were singularized from the panel and the final thickness was evaluated. Table 6 shows the measured thickness values for the boards. Cross sections of the TV1 and TV3 are given in Figure 15 and Figure 16, respectively. Table 6 shows the mean value for a random sample of 15 TVs with the thickness measured manually with micrometer gauge.

Table 6: Thickness values of built test boards

Test Vehicle	Build-ups	Thickness Pos. A. Mean / σ [µm]	Thickness Position B Mean/ σ [µm]
TV1	3+2+3	443 / 5.4	482 / 4.3
TV2	1+A6+1	481 / 3.3	498 / 4.3
TV3	A8	485 / 5.5	512 / 6.6

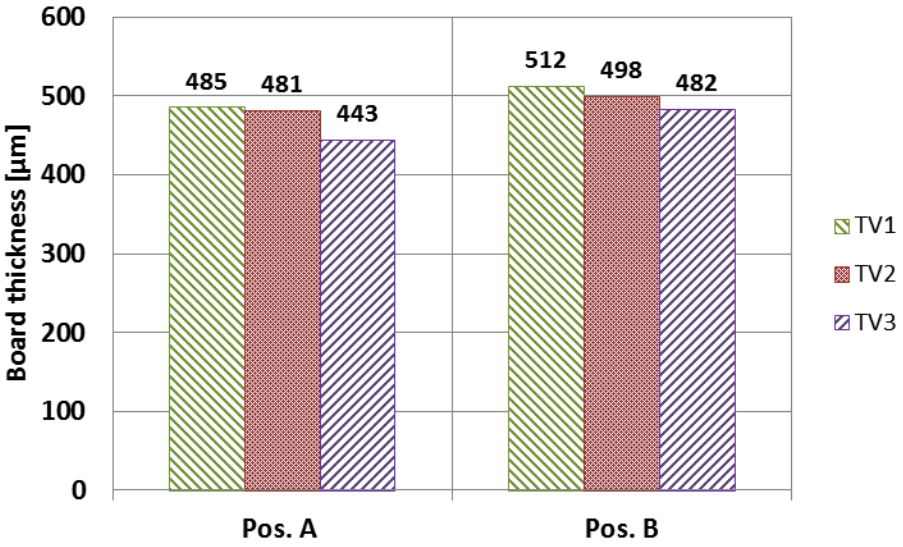

Figure 14: Mean thickness of the manufactured thin boards (TV1 to TV3)

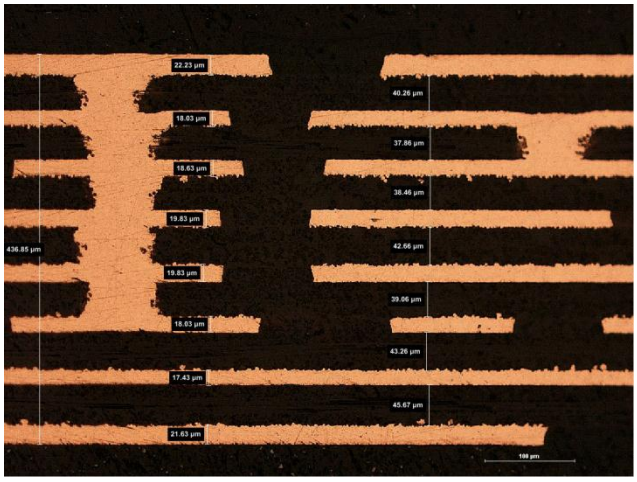

Figure 15: Cross Section of TV1 (3+2+3 HDI/FV bildup)

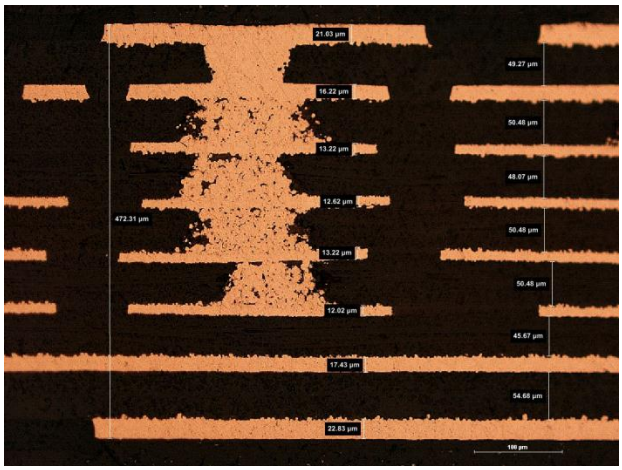

Figure 16: Cross section of TV2 (1+A6+1 ALIVH-C build-up)

Reflow performance

The results of the reflow testing are summarized in the subsequent Table 7. The results of the components show that the HDI/FV board performed significantly better than the two ALIVH build-ups. While at the TV2 and TV3 most of the delamination failures occurred between the 3rd and 4th reflow cycle all TV1 samples survived a number of 15 reflow runs. An example for a typical failure that was observed at TV2 and TV3 is given in Figure 17.

However it has to be pointed out that the big difference observed cannot be directly related to the influence of the manufacturing process. Rather than that it has to be considered that the used FR4 HDI prepreg material is a most recent generation FR4 material that has been optimized for reflow behavior and has a known outstanding reflow performance. Thus it is as expected that TV3 shows the best performance in MSL testing.

If the cross sections the failures at TV2 and TV3 are investigated in more detail it is visible that the delamination failures occur in both cases which feature design characteristics which are known to be critical for reflow testing, such as structures with full copper areas. The analyses did not show evidence for an interface failure that could be related to the applied copper surface adhesion promotion system. Rather than this the cross sections show a mixed failure mode with cohesive failure in the prepreg layer as well as adhesive failure at the interface (Figure 18). In order to identify the root cause for delamination at the current samples more work has to be done, however although the performance of TV2 and TV3 in the reflow process did not reach the level as it is required for mass production board, it is considered as acceptable taking into account that the samples are built within a development project without any process optimization steps.

Table 7: Results of reflow testing of thin board test vehicles

Test Vehicle	Number of reflow cycles survived	
	Mean Value	σ
TV1	15	-
TV2	2.4	0,8
TV3	3.4	1,2

Figure 17: Cross section after reflow testing, Occurred delamination at TV3

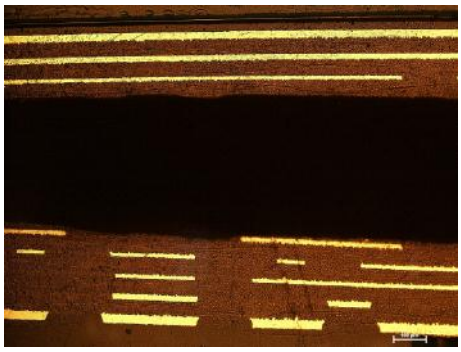

Figure 18: Detailed view on delamination area at TV3

Thermo cycling results

As described above, the temperature cycling was done on bareboard coupons as well as on populated ones. Neither at the bareboard samples nor at the populated ones failures were observed over the test time. Figure 19 shows resistivity versus cycle count for the bareboard thermocycling test. None of the tested specimen exceeds the limit of -10% of resistivity decrease, the test is considered as passed for all part numbers.

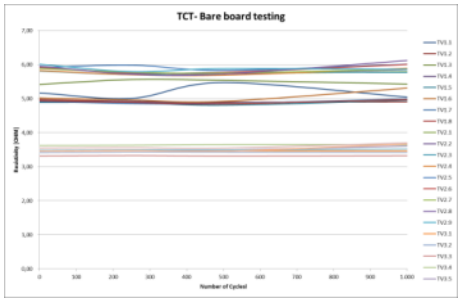

Figure 19: Resistivity versus cycle count for the thermo cycling test, bareboard level

At the thermo cycling of the populated samples also no failure was observed as shown in Table 8.

Table 8: Summary of results of thermo cycling test, board level

Part number	Thermo cycle test
TV1	4/4 passed
TV2	4/4 passed

Based on the obtained results it can be considered that the thermo cycling behavior will not present the primary challenge in manufacturing thinner boards. It is commonly considered that major effect influencing the performance of boards stressed cyclic thermo load is the CTE mismatch between copper at vias and applied dielectric materials. Making the boards thinner does not make the mechanical loads on the copper plating in the plated through holes or the micro vias significantly more severe. This assumption is confirmed by the results of the current work. Additionally no influence of the manufacturing technology was observed. All test vehicles manufactured with the different any-layer technologies passed the limit of 100 cycles in barebord as well as populated configuration.

Results HAST Test

In contrast to the thermo-cycling the electrochemical migration behavior seems to be a more critical issue for very thin boards. The subsequent Table 9 shows a summary of the results obtained from HAST testing of the investigated samples.

Table 9: Summary of result of HAST testing for thin board test vehicles

	TV1	TV2	TV3
Comb L1	1/5 failed	1/5 failed	0/5 failed
Comb L2	1/5 failed	0/5 failed	0/5 failed
Comb L3	0/5 failed	1/5 failed	0/5 failed
Comb L4	0/5 failed	0/5 failed	1/5 failed
Comb L5	0/5 failed	0/5 failed	1/5 failed
Comb L6	0/5 failed	0/5 failed	1/5 failed
Comb L7	0/5 failed	0/5 failed	1/5 failed
Comb L8	1/5 failed	1/5 failed	2/5 failed
V-2-P	2/10 failed	2/10 failed	3/10 failed
V-2-V	0/10 failed	0/10 failed	0/10 failed

In general the table shows that several failures have been recognized. At the current study the samples with an HDI outer layer – TV1 with the full HDI built-up and TV2 with the ALIVH-C built up showed at better HAST performance than TV3.

For the HAST test the via-to-via (V2V) structure can be regarded as the least critical case of the three cases evaluated. As expected there was no failure observed at these structures.

In contrast to the V2V case, for the via-to-plane structure (V2P) at all test vehicles failures were observed. In order to investigate this more in depth the time to failure was plotted versus the test duration as shown in Figure 20. It can be seen that the majority of the failures occur at early stage of the test which might be a sign of residues or impurities due to non-optimized manufacturing conditions. Cross-section analyses of the failed samples did not show evidence of failure due to dendrite growth. All observed dendritic structures can be considered as small compared to the corresponding dielectric gap. However as it is also shown subsequently for the comb structures, the samples show clear signs of electrochemical migration of copper into the dielectric material. Together with the observed small dendrites this is considered to be a major cause for the observed failures.

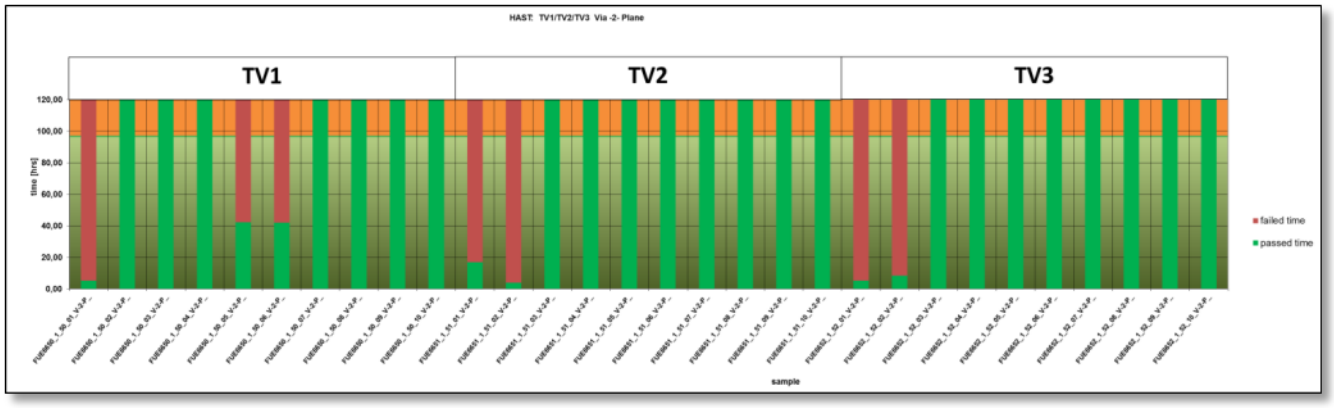

Figure 20: Time to failure for via to plane structures for the thin board test vehicles

Concerning the comb structure the results are similar to the results obtained for theV2P structures. Again TV1 and TV 2 show better results than TV1. For all samples the majority of the failures are located in the outer layer comb structures, literally in layer 1 and layer 8. Figure 21 shows a detailed plot of the monitored resistivity versus test duration for the comb structure on one outer layer (layer eight).

As for the V2P structures the evaluation of cross sections of the failed coupons did not show evidence of excess filament growth or related electrochemical migration effects which could be identified as root cause for the failure in the HAST test. In fact the comb structures showed significant signs of copper migration at the failed samples. Figure 22 shows an example for a failed structure at TV3 in a darkfield view, Figure 23 shows a darkfield/UV image of a failed comb structure of TV2.

Both figures show the clearly the migration front at the copper traces with negative potential. However it is also visible that the migration front has not reached the neighboring conductor at the time of failure. So again it is considered that failures at the comb structure are a combined phenomenon where the migration effects together with dendritic growth or impurities such as copper residues finally result in a drop of the resistivity.

In general based on the experiences available at AT&S related to electrochemical migration phenomenon such as dendritic growth the obtained results are considered as non-critical for all three part number since during manufacturing of the evaluated TVs in first step no specific manufacturing provisions to improve CAF/HAST behavior have been applied. Available experiences show that with special provisions – as regularly applied in mass production – a significant improvement of the electrochemical migration behavior can be achieved.

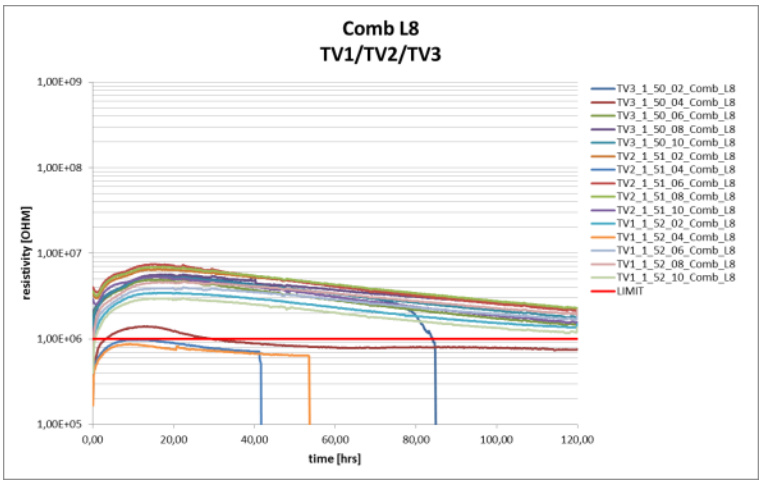

Figure 21: Resistivity for comb structure on outer layer (L8) vs. storage time in HAST test

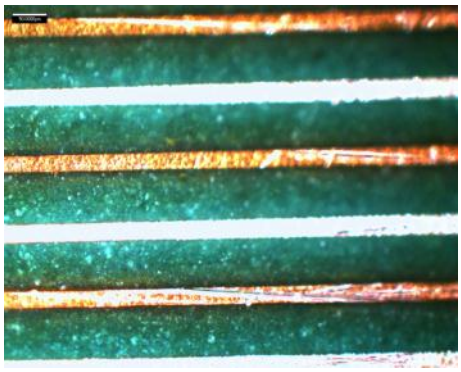

Figure 22: Microscopic darkfield illustration of comb structure on TV3 Layer 1, Solder mask layer removed by grinding

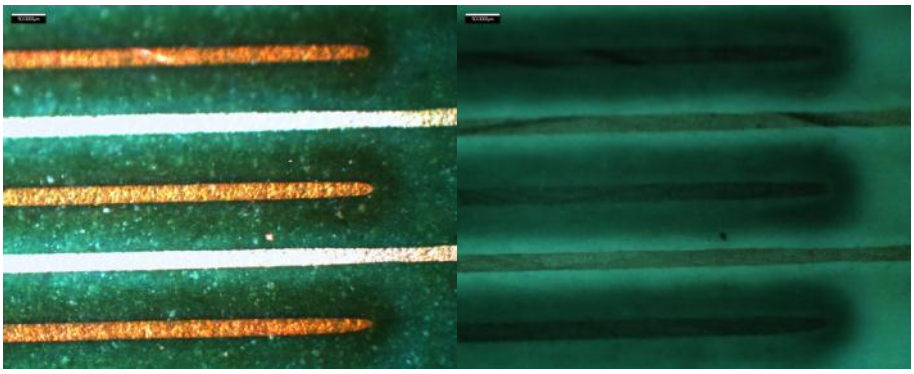

Figure 23: Microscopic illustration of comb structure on TV2 Layer 8, Solder mask layer removed by grinding, left view darkfield, right view with UV lamp

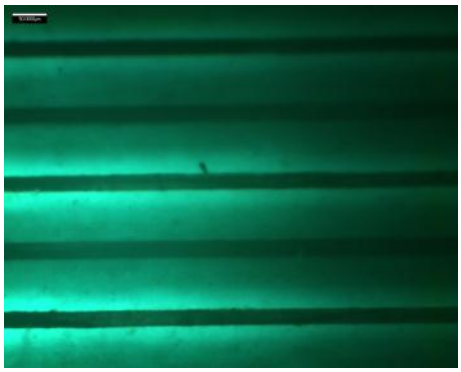

Figure 24: Identified copper dendrite on TV2 layer 8, solder mask partially removed by grinding, UV lamp applied

Conclusion

The smart phone market drives the producers of PCB for mobile systems more and more to reduce the board thickness. For an 8 layer board for a modern mobile phone an any-layer design is considered as almost mandatory, while the thickness target is currently at 600 µm for this kind of stack up and will go down to 400 µm for a rigid 8 layer board in 2013.

The current work showed that already with the currently materials and the available means of manufacturing it is possible to build rigid anlylayer PCBs featuring a build-up of 8 layers with a maximum thickness of less than 500 µm.

To implement the boards different manufacturing approaches were successfully applied. On the one hand a high end HDI process combined with via filling step on the other hand the ALIVH technology. Additionally it was shown that also the combination of pure ALIVH with outer layer HDI, the so called ALIVH-C process could be successfully applied. Board thicknesses between 443 and 512 µm were manufactured. While AT&S has available experiences from almost 20 years of HDI manufacturing in ALIVH has been licensed and introduced in 2011. Thus especially the ALIVH technology promises still additional potential for improvements in manufacturing of thin boards.

The reliability behavior of the samples built during this study is overall considered as acceptable. Currently the material situation for the HDI process can be considered as advantageous compared to the materials situation for the ALIVH process. While this is specifically true for the reflow sensitivity behavior the observed difference in performance of the three produced test vehicles was lower for the electrochemical migration in the HAST test. Finally the temperature cycling of the parts did not cause any failure during this study.

It can be concluded that all observed technologies are generally feasible for building reliable thin boards. Further work will have to focus on potential to meet functional requirements, such as the electrical performance and the economic questions that are corresponding to the manufacturing of very thin boards.

References

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[3] H. Holden, „The HDI Manufacturing Processes," in *HDI Handbook*, Seaside, BR Publishing, 2009, pp. 230-257.

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[6] JEDEC, „JESD22-A104D - temperature Cycling," JEDEC Solid State technology Association, Arlington, 2009.

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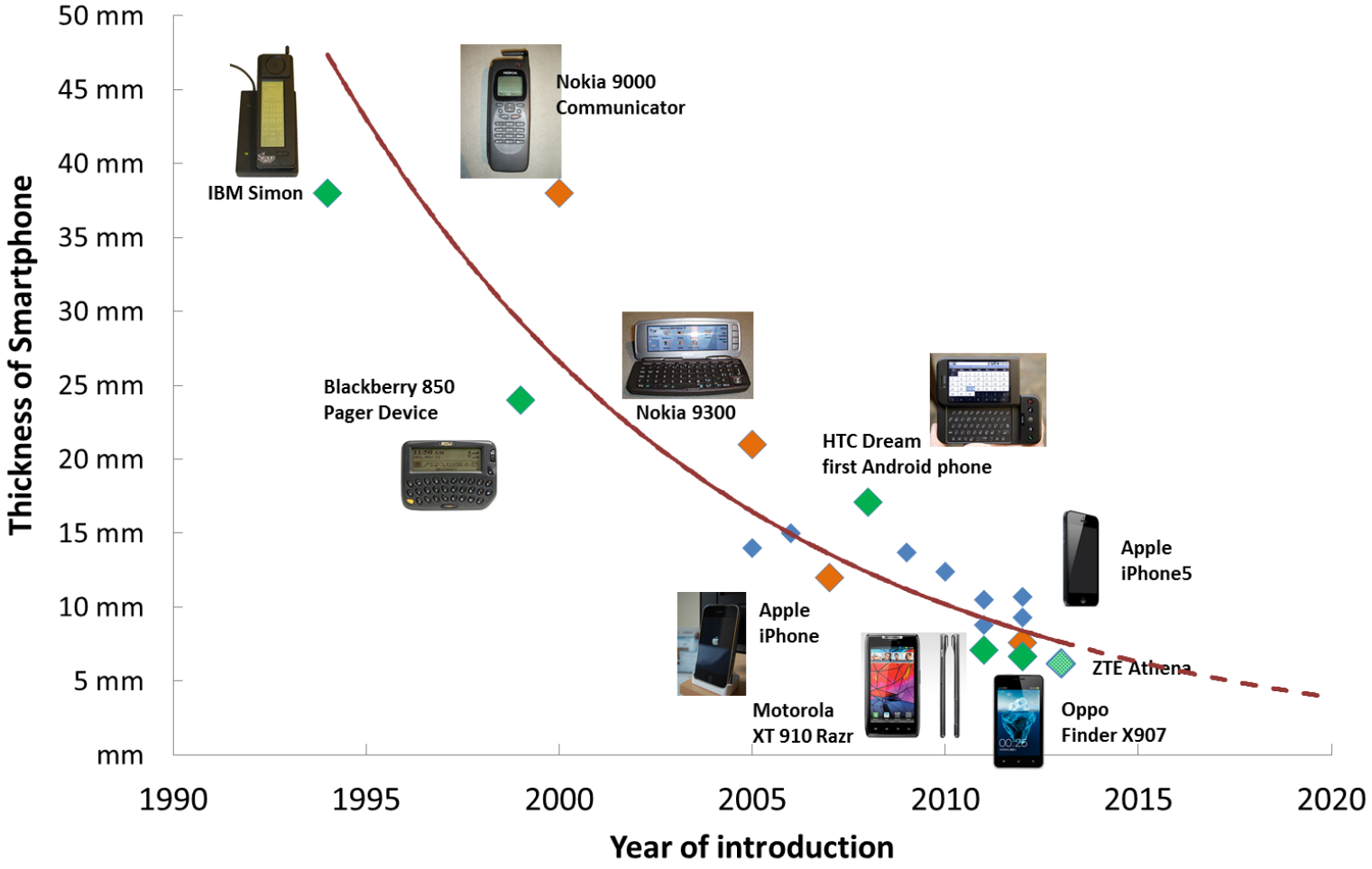
Reliability Performance of very Thin Printed Circuit Boards with Regard to Different any-layer Manufacturing Technologies

Thomas Krivec
R&D Project Leader / AT&S AG

Contents

- Getting thinner: some history
- Project targets
- Test vehicle design, materials and processes
- Thickness of built test vehicles
- Results from reliability testing
- Conclusion

Getting thinner …



Thin Board Project Targets

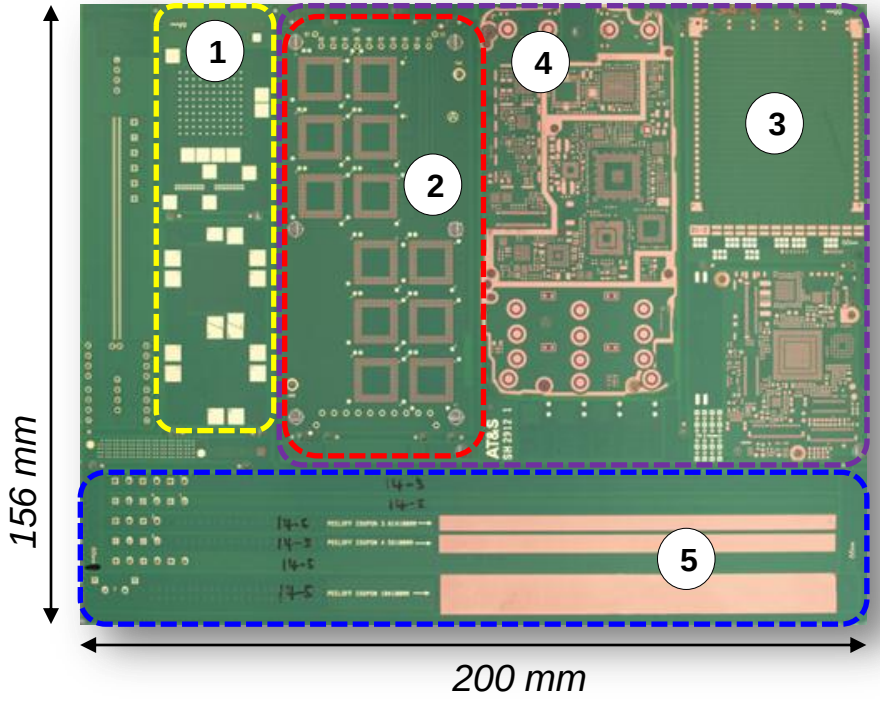
- Manufacturing of a very thin multilayer rigid board with the available process landscape
  - 8 Layer
  - Target maximum total thickness: < 500 µm to
- Show feasibility of compliance with reliability requirements common for mobile segment
- Small volume mass production possible in early 2013

Project Scope and Sequence

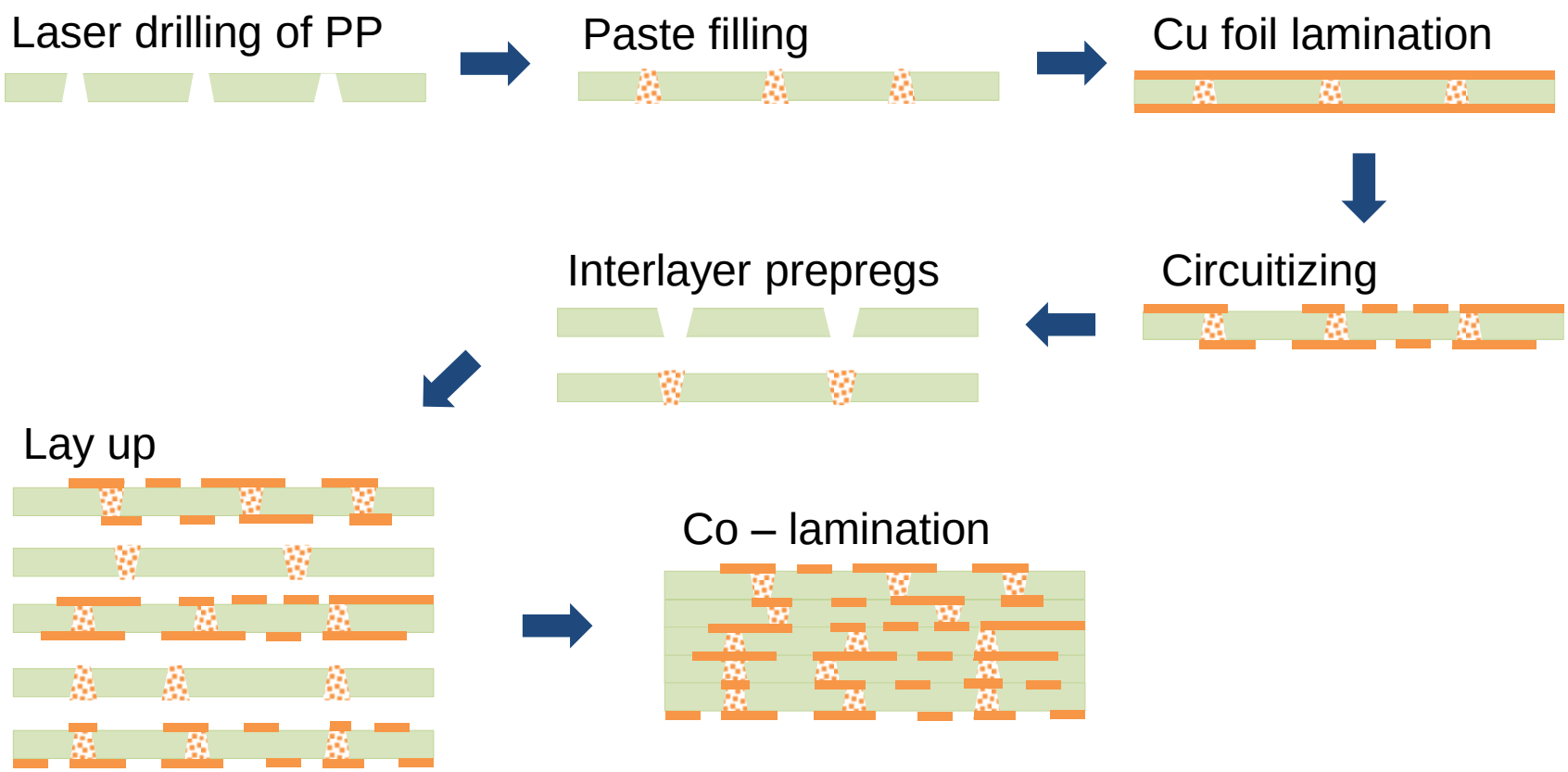
- Clarification of market requirements
  - Impedances and Electrical performance
  - Reliability issues
- Preparation of Solution Concepts
  - Definition of test vehicle (TV)
  - Concept for manufacturing TV with ALIVH + FV/HDI
  - Materials selection
- Manufacturing of TVs
- Reliability testing of manufactured TVs

Test Vehicle

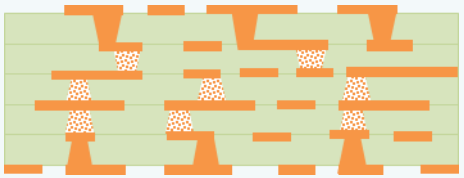
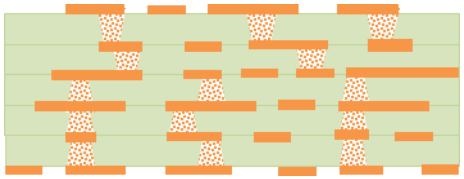
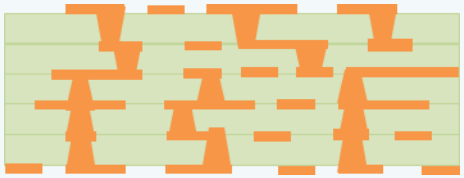
- Evaluation Design
  - HAST (1)
  - Drop test / TCT coupon (2)
  - TST bareboard coupon (3)
  - MSL/RSS coupon (4)
  - Impedance coupon (5)
- 2 basic technology approaches
  - HDI/Filled Via
  - Anylayer Interstitial Via Hole “ALIVH” (Proprietary process introduced in 1996 by Panasonic/Matsushita)



ALIVH Process Flow



Test Vehicle Stack-up

Test Vehicle	Technology	Build-up	Dielectric Material
TV1	ALIVH-C 	1-A6-1	HF FR4 Low Flow HF FR4
TV2	ALIVH-G 	A8	Low Flow HF FR4
TV3	HDI/FV 	3-2-3	HF FR4

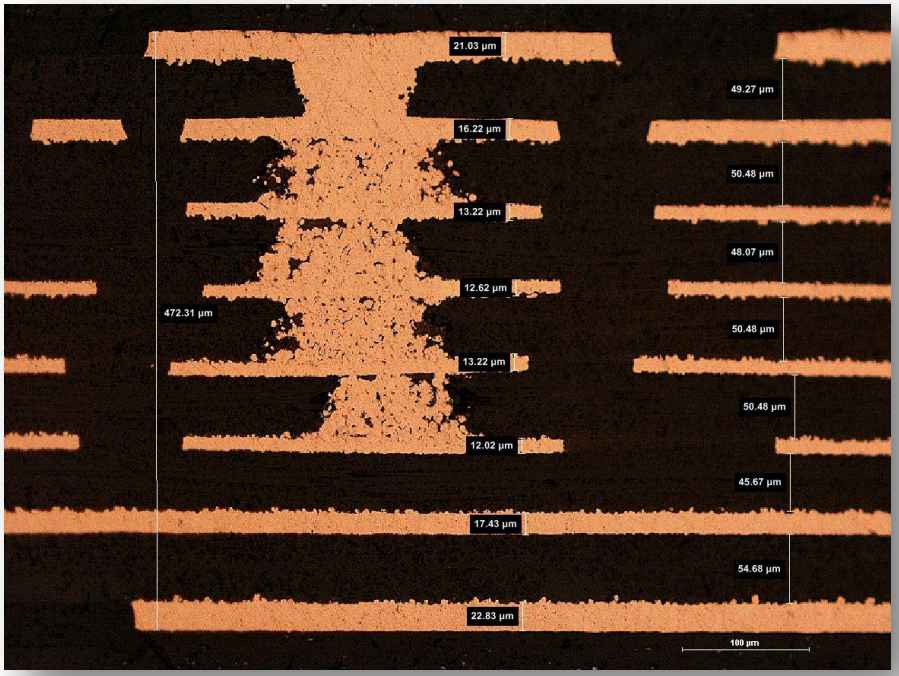
Materials applied

Property	Low Flow FR4 PP	FR4 standard PP	FR4 standard CCL
Halogen free	yes	Yes	yes
Cloth style	1037	1037	1x106
Resin content [%]	73	70	65
Thickness [µm]	50	45	50
Cu thickness [µm]	-	-	12
D_k	4,8	4,1	4,2

- HDI: Copper foils, single sided standard treatment
- ALIVH: Process qualified CU-foil, single sided standard treatment

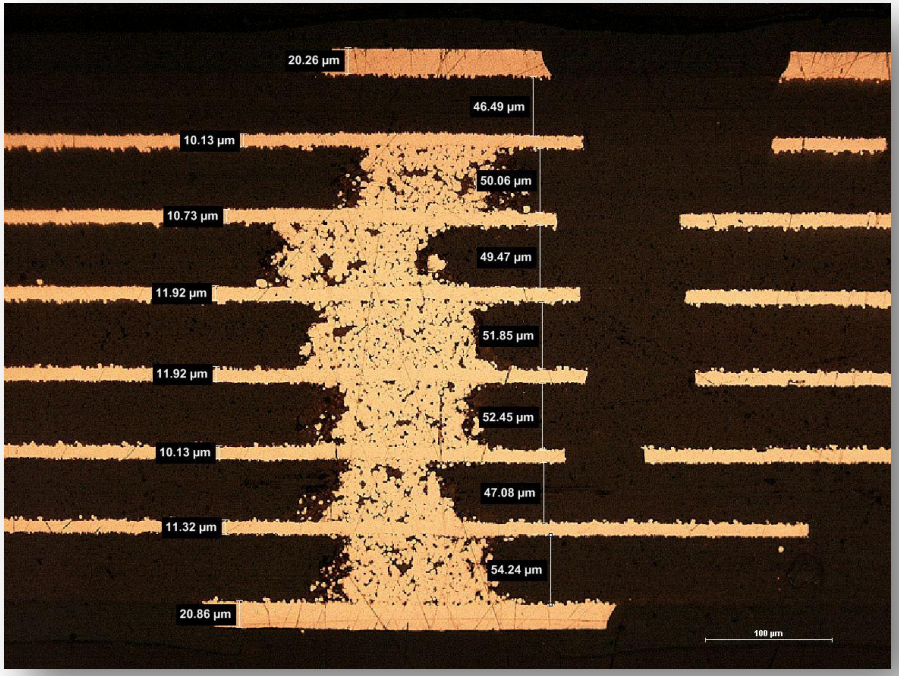
TV1

- Stack up: 1-A6-1
- t = approx. 480 µm
- Thin inner copper layers (12 µm)
- “granular structure” at vias in core
- Filled HDI vias connecting L1 and L2



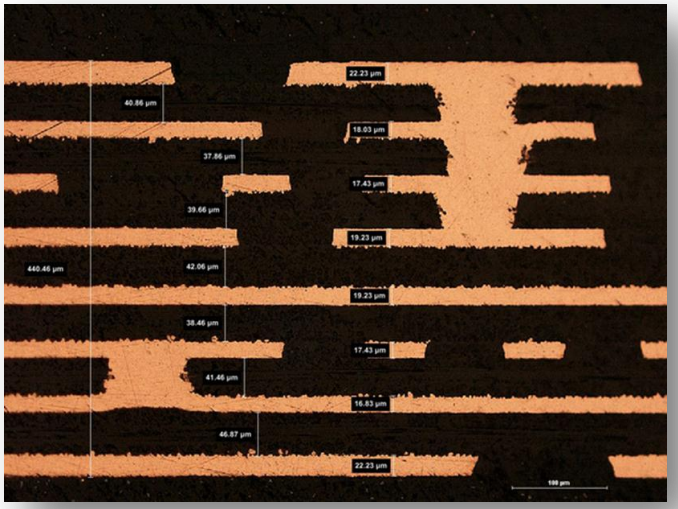
TV2

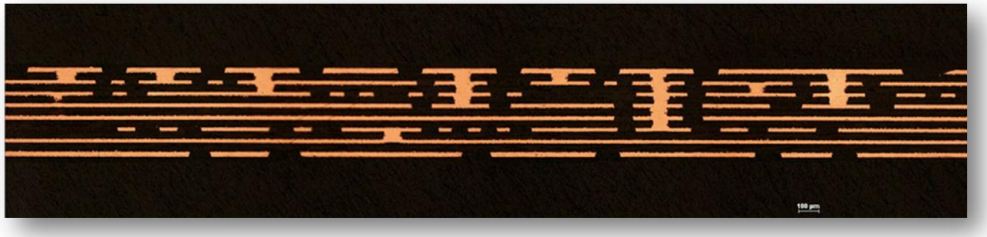
- Stack up: A8
- t = approx. 490 µm
- Thin inner copper layers (12 µm)
- “granular structure” at vias



TV3

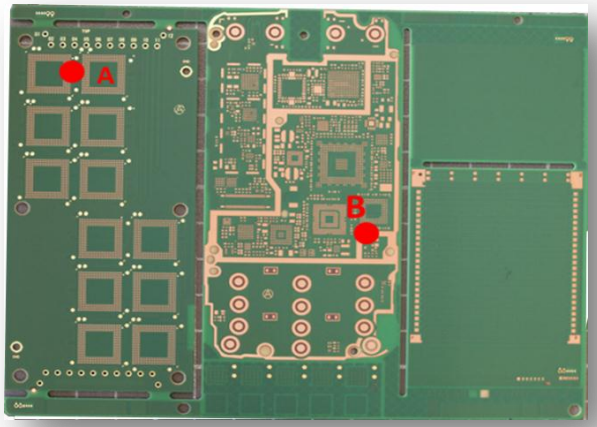
- Stack up: HDI 3-2-3
- t = approx. 450 µm
- Copper layers thickness approx. 20 µm
- Final dielectrics thickness approx. 40 µm
- Compact structure in filled vias





Thickness of Boards

- Measurement at two positions
  - Pos. A: Low copper content in Build-up
  - Pos. B: High copper content in buildup

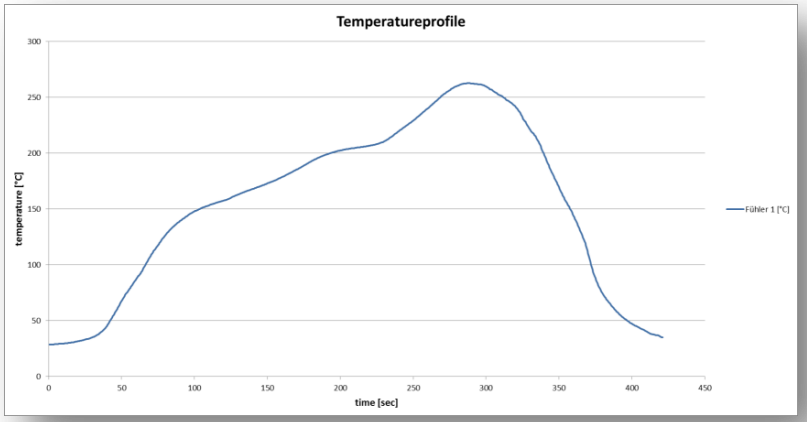


Test Vehicle	Build-ups	t_A Mean / σ [µm]	t_B Mean/ σ [µm]
TV1	1+A6+1	481 / 3.3	498 / 4.3
TV2	A8	485 / 5.5	512 / 6.6
TV3	3+2+3	443 / 5.4	482 / 4.3

Reflow sensitivity Test

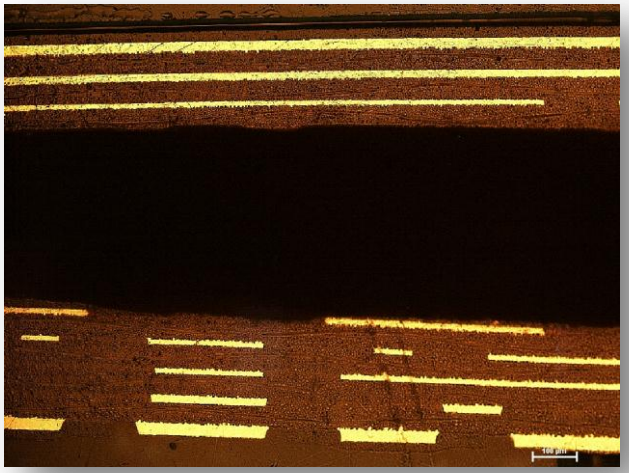
- JEDEC/IPC J-STD-020
- Lead free reflow profile
- T_{peak} = +260 ºC

- 10 samples per PN
- Preconditioning acc. to MSL3acc
  - Drying 24 h at 125 ºC
  - Conditioning 60 ºC / 60% RH /40 h



Reflow Sensitivity Results

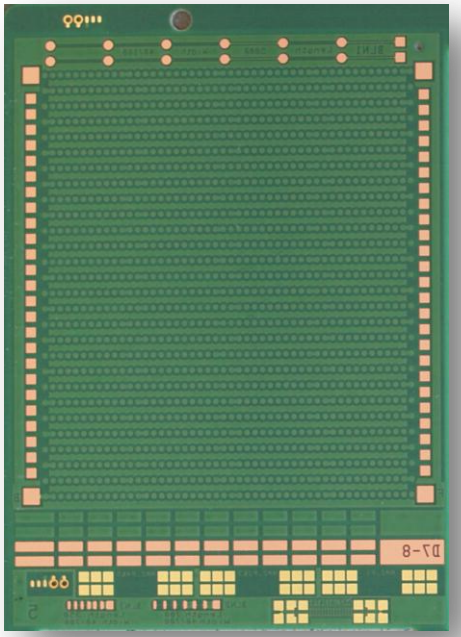
Test Vehicle	Reflow cycles without delamination	
	Mean Value	σ
TV1	7.3	1.3
TV2	8.0	0.7
TV3	>30	-



- Good performance of HDI sample due to material with optimized delamination behavior

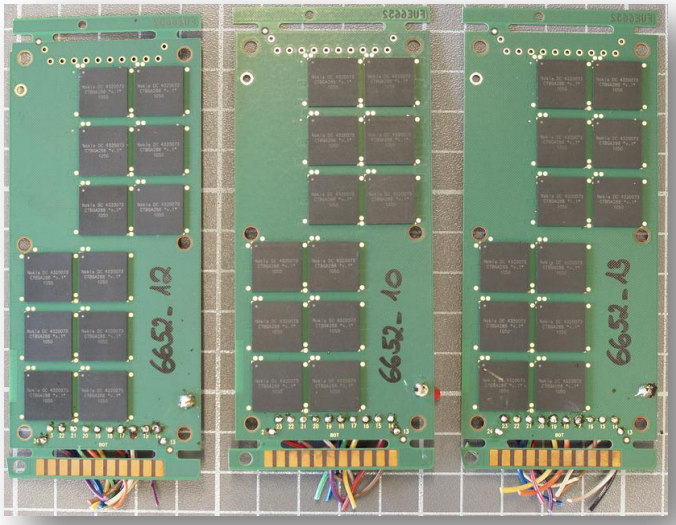
TST Test

- TST bareboard testing
- 2 chamber test setup
- Cold chamber: -55 ºC / 15 min
- Hot Chamber: +100 ºC /15 min
- 1000 cycles
- 8 samples of each part number tested
- Failure criterion:
  Resistivity change <10%



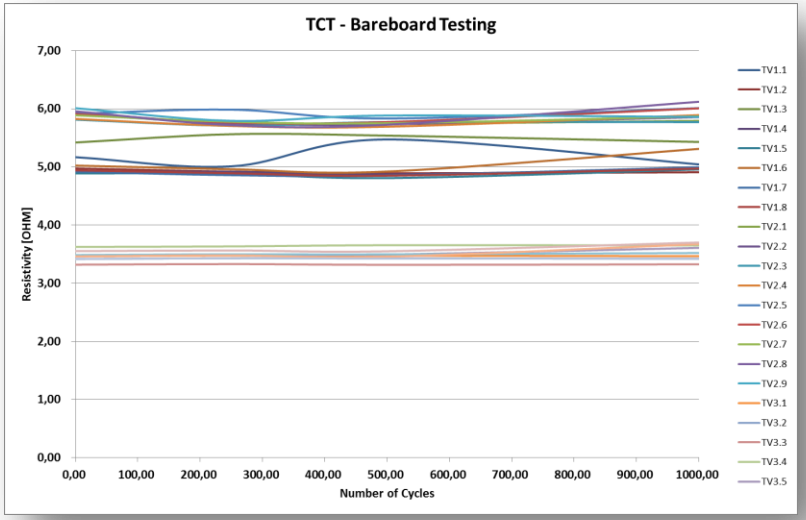
TCT Test

- TCT testing of assembled board
- 1 chamber test setup
- 40 ºC to + 125 ºC
- 5 min soak time at min/max temperature
- 2 cycles per hour
- 1000 cycles
- 4 samples of each TC tested
- Online event detector



TST/TCT Test Results

- Bareboard and populated samples passed 1000 cycles
- No influence of the production approach visible
- Main driver for TCT failure is Cu/PP z-CTE mismatch



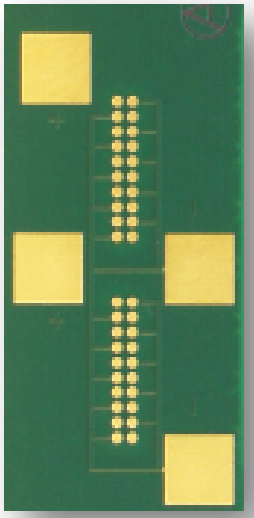
HAST Test

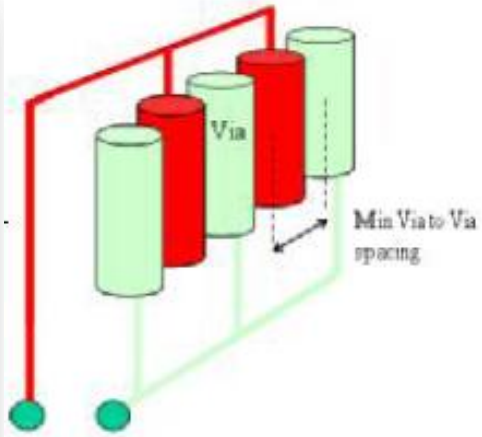
- Test acc. to JEDEC JESD 22-A101C
- Via 2 Via coupon
- Comb structure coupon on each layer
- Online failure detection with event detector

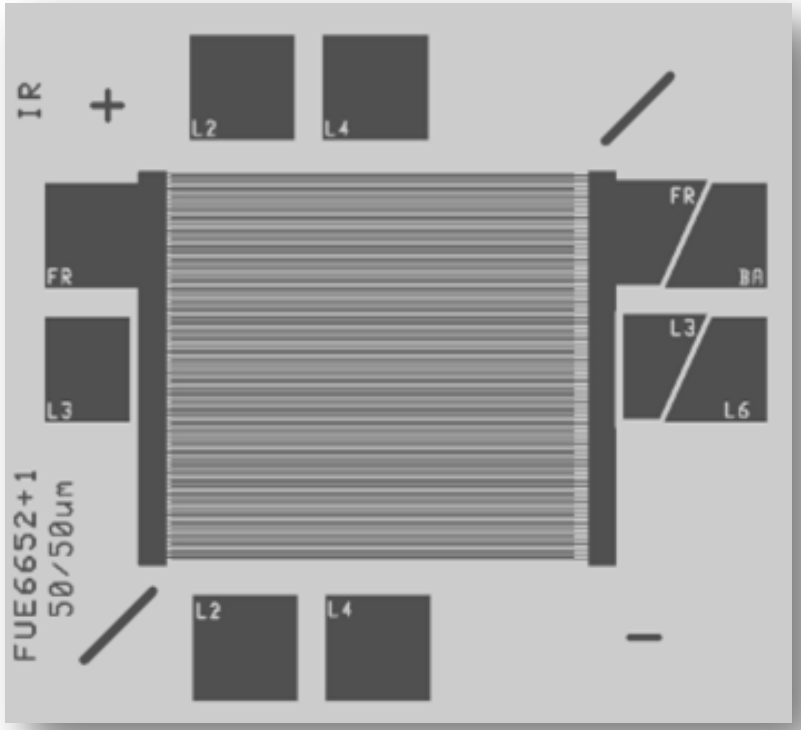
Parameter	Level
Temperature	130 ºC
Humidity	85% r.h.
Bias	3.5 VDC
Test duration	120 hrs
Pass criterion	R > 10^6 Ohm after 96 hrs.

HAST Test Coupons

- Via to Via
- Comb structure Coupon

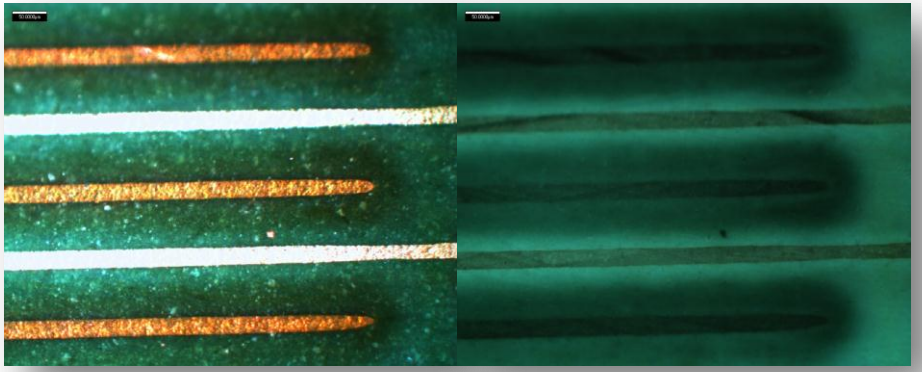






HAST Test Results

- No failures at V2V
- Single Failures identified at comb structures
- Outer layers more affected
- Copper migration visible
- Small dendrite growth observed
- Most failures related to residues: Prototyping process !



	TV1	TV2	TV3
V-2-V	0/10 failed	0/10 failed	0/10 failed
Comb L1	0/5 failed	1/5 failed	1/5 failed
Comb L2	0/5 failed	0/5 failed	1/5 failed
Comb L3	0/5 failed	1/5 failed	0/5 failed
Comb L4	1/5 failed	0/5 failed	0/5 failed
Comb L5	1/5 failed	0/5 failed	0/5 failed
Comb L6	1/5 failed	0/5 failed	0/5 failed
Comb L7	1/5 failed	0/5 failed	0/5 failed
Comb L8	2/5 failed	1/5 failed	1/5 failed

Conclusion

- Boards with 8 layer, t < 500 µm could be successfully built
  - Printed via and HDI any-layer approaches feasible
  - Materials are available
  - Processes can be handled
- First sample lots showed acceptable reliability behavior
- Still open questions
  - Electrical performance: Controlled impedances
  - Drop Test / Impact performance of very thin boards
  - Thermal management for very thin boards

Thank You!

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