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Assembly of Flip Chips Utilizing Wafer Applied Underfill

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Abstract
Wafer-applied underfills are key to the widespread acceptance of flip chip technology. This NIST-ATP funded consortium is developing the materials and processes for achieving a wafer-applied underfill system that is both self-fluxing and reworkable. In the present work, the factors impacting successful assembly of pre-underfilled chips are studied. Flip chips with the underfill material pre-applied to the devices were assembled in the lab using production equipment. The presence of the underfill coating was examined for its influence on vision recognition, placement and reflow.

Introduction
Industry experts foresee double-digit growth in the production of flip chip devices in the near future. Flip chip is increasingly providing the density and performance solution for the demands of today's consumer electronic products. Early obstacles to the successful implementation of flip chip included expensive evaporative IC bumping, and limited availability of bumped printed circuit boards of sufficient density. New technologies such as low cost eutectic bumped IC's and the introduction of high density interconnect printed circuit boards (HDI) have removed these obstacles. One remaining concern for widespread acceptance of the flip chip technology is the underfill of the chip. Underfill dispense is difficult to manage in a high volume surface mount assembly line. The slow cycle time requires multiple equipment sets, increasing the cost associated with underfilling. Recent improvements in fast flow or no flow and snap cure materials have improved the situation somewhat, but the ultimate answer is to remove the underfilling step from the surface mount factory completely.

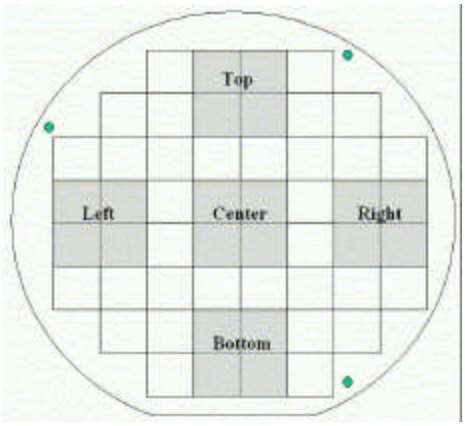
This National Institute of Standards and Technology Advanced Technology Program (NIST-ATP) program seeks to develop the ultimate flip chip underfill solution. The joint venture partners (Motorola, Auburn University, and Loctite Electronic Materials) are developing the materials and processes needed to apply underfill material at the wafer level, for subsequent SMT assembly. The underfill is self-fluxing and reworkable, and cures within a standard reflow cycle. The parts are intended to be delivered in tape and reel or tray format, and can be handled as any other SMT component on the line. The engineering challenges in developing a simple, SMT-compatible flip chip process are considerable.

Extensive studies have been undertaken to characterize this new flip chip assembly process using die with pre-applied underfill. The details of achieving a production-quality placement process were investigated in light of the physical attributes of the underfill materials and the coated die. The die are prepared using a two-layer coating process, consisting of a fluxing underfill layer on the flip chip bumps, followed by a bulk dielectric layer surrounding the bumps. Each layer is b-staged after printing, and the materials are designed to liquefy and flow, then cure during the reflow process. Attributes of the materials and the coating were evaluated and the influence of these properties on the assembly process was assessed. Material attributes such as Tg, CTE, moisture resistance, adhesion and wetting contact angle are covered in detail elsewhere.[1]

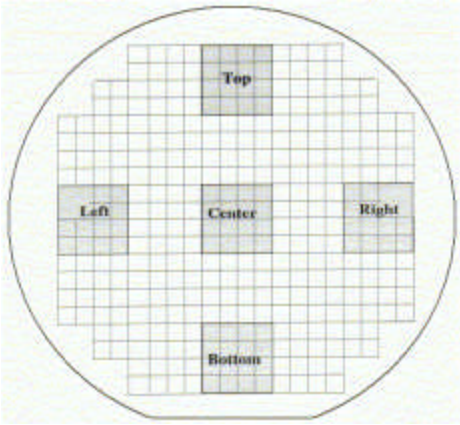
Pre-Applied Underfill Coating Evaluation
Clearly, the outcome of the assembly process using flip chips with pre-applied underfill will depend to a great extent on the quality of the underfill coating. The deposition process must provide sufficient uniformity and consistency to enable a high-yielding assembly process with reliably formed joints and a sufficient perimeter fillet. For this reason, inspection of the as-received coated chips is important for effective assembly process development.

To establish the quality of the underfill coating process, bulk dielectric thickness and consistency were evaluated. After testing a variety of surface profiling methods, a non-contact laser profilometer was chosen for this experimental work. Measurements obtained with the laser profilometer were confirmed by cross-sectioning a few coated die.

Average thickness values for a sampling of dies from left, right, center, top and bottom side of the wafer were compared with the average coating thickness across the entire wafer. The sampling scheme is shown in Figure 1. In this manner, systematic variances in coating thickness could be uncovered and used to optimize the coating process. Two test wafers were selected for study. These include a 12-mil pitch dual perimeter I/O chip, 9.3-mm on a side, on a 100 mm wafer which was developed by Auburn University. The second wafer is the commercially available FA10, from Kulicke and Soffa, having a 10-mil pitch area array I/O layout on a 5-mm chip, on a 127 mm wafer.



(a) 12-mil pitch perimeter I/O wafer layout

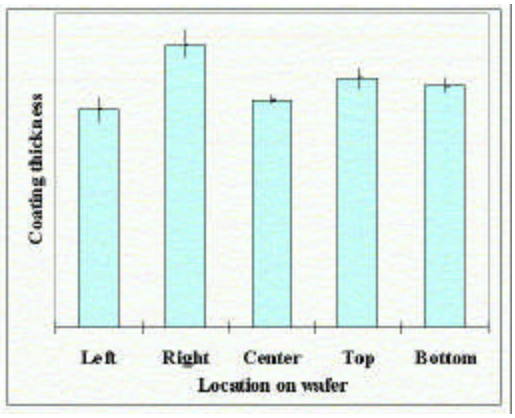


(b) 10-mil pitch area array wafer layout

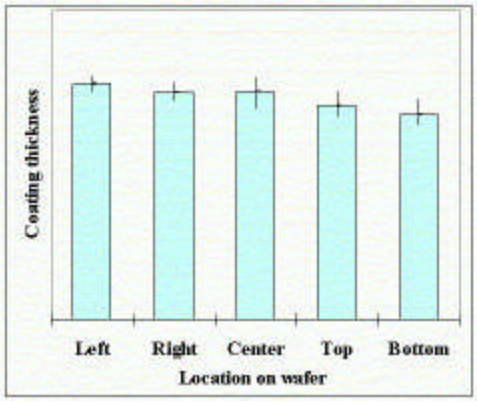
Figure 1 - Wafer Mapping Used For Coating Thickness Data

Column charts were generated to display the coating variation, and this information was used to adjust the process to reduce the variation. Figure 2 shows examples of early coating thickness data for two types of die. Data for die with perimeter I/O only are shown on the left and area array die are shown on the right. Similarly, typical coatings for the two types of wafers are shown in Figure 3.

These data show that it was easier to gain a consistent coating thickness on the area array bump configuration, although later coating process improvements yielded similar results on the perimeter I/O chip as well.

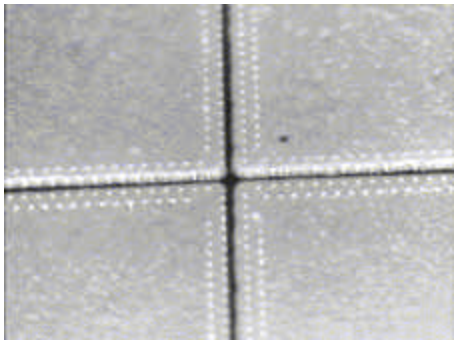


(a) thickness data for perimeter I/O wafer

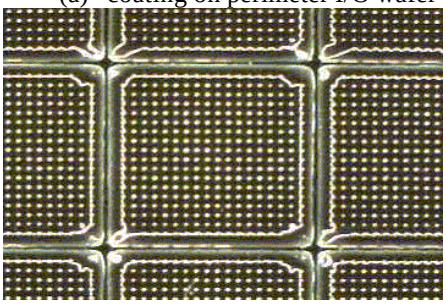


(b) thickness data for area array wafer

Figure 2 - Example of Coating Thickness Variation Across One Wafer



(a) coating on perimeter I/O wafer



(b) coating on area array wafer

Figure 3 - Examples of Coating Appearance

Assembly Process Development

The variables associated with an assembly process using pre-applied underfill coated chips are nearly too numerous to list. In the present effort, development efforts are proceeding in a logical manner through each of the sequential SMT process steps, beginning with vision recognition at placement.

Vision Recognition

The first step in the SMT assembly process that may be impacted by the presence of a wafer-applied underfill is vision recognition at the placement machine. The solder bumps are used as locating features in place of fiducials. In the presence of underfill, the apparent size and shape of the bumps may be altered, in some cases significantly. In addition, the three dimensional topography of an uncoated bumped die aids vision recognition with the formation of shadows around the bumps. These shadows enhance the camera's ability to sense the bright bump against the darkness of the shadows. With a coated die, the topology may be flattened and the enhancing shadows are not formed, further complicating the recognition step.

Fortunately, many placement machines offer flexibility within their vision system to optimize the imaging. Parameters such as light intensity, illumination angle, etc. can be varied. Initial work simply evaluated the effectiveness of the standard lighting scheme in identifying bumps on coated die. The typical change in image for a coated chip as seen by the vision system is shown in Figure 4.

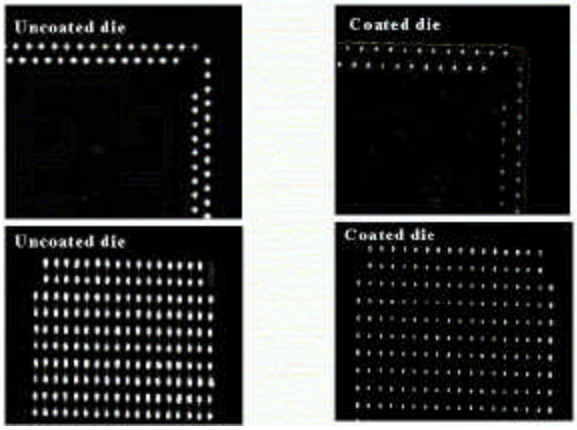


Figure 4 - Vision system images of perimeter I/O chip (top) and area array chip (bottom)

The ideal die should have sufficient contrast between the bumps and their background for component inspection, as reduced contrast increases the probability of die inspection failure. Earlier work studied the influence of coating color on the contrast achieved in vision recognition, concluding that the only viable choice for coating color was black.[2]

The ability of the vision system to recognize the bump is related to the bump area, as the minimum detection limit of vision recognition is determined by the number of pixels in the image of the feature to be detected. The number of pixels of a feature is determined by the magnification level of the camera, in addition to the physical size of the feature. On the lab placement machine, there are two upward-looking cameras, with the front camera having better resolution. The minimum number of pixels for consistent detection with this camera is four, on an eight-pixel pitch. With the camera magnification of 14 um per pixel in the X direction and 11 in Y, the theoretical minimum detectable feature size is a bump of 56 um x 44 um in dimension, or about 2500 square microns.

Since the supplier of coated die will need to produce a product that is acceptable for use in an SMT factory, several bump inspection methods were examined to establish a technique for predicting the ability to recognize coated die. The most straightforward method was simply to inspect the coated die with a microscope and use a standard image analysis software package to measure the open area of the bumps. The dies were then tested on the machine vision recognition system to establish the correlation between open area of the bump and the ability to recognize the bump. There are three possible states in terms of coated die bump recognition: consistently recognized bumps,

consistently unrecognized bumps, and unrepeatable bumps, which have inconsistent results in that the bumps are sometimes recognized by the vision system and sometimes not with no apparent changes in lighting or other variables. See examples of the three states in Figure 5. Each inspected bump was placed in one of these three groups.

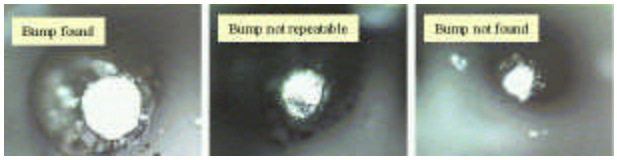


Figure 5 - Bumps on Coated Die as Inspected by the Universal Vision System

Two hundred, nineteen bumps were included in the study. First, it was noted that bumps having an area of 2500 square microns could not be recognized by the vision system, and the open area needed to be larger than this to be consistently recognized. The recognized bumps have a statistically larger average bump area than unrecognized or not repeatable bumps (Figure 6). Note however, that there is significant overlap in the distributions. Within the shaded area of the graph, a bump with a given area may be not recognizable at all, sometimes recognizable, or always recognizable. To supply coated die that can always be recognized and placed, bump areas at the upper end of the range must be specified.

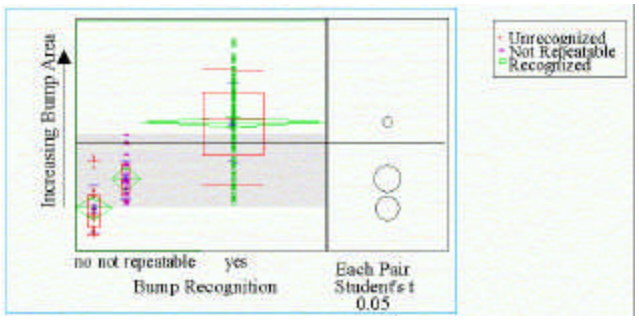


Figure 6 - Bump Recognition Versus area Measurements

Work is in progress to test the practicality of achieving the required bump area with the coating thicknesses that are required to completely fill under the chip and form a fillet. To estimate the amount of underfill that is needed to underfill the chip and form a fillet around the perimeter, simulation of a single solder joint reflowed in an underfill environment was performed.[3] The simulation showed that acceptable underfill fillet formation requires that the coating thickness is comparable to the bump height. This very preliminary work suggests that the coating thickness that yields the open area that is best for vision recognition may be too thin to assemble properly (Figure 7). For this reason, various schemes to improve the detectability of the bump open area are underway.

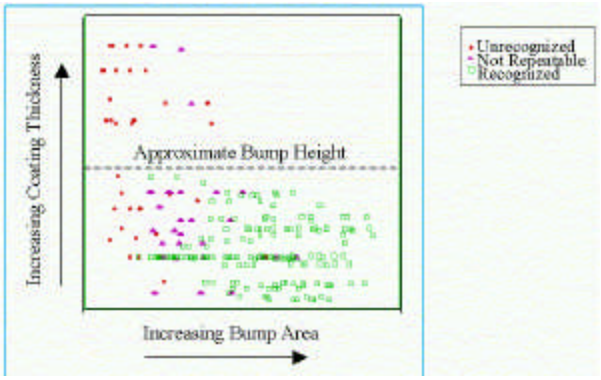


Figure 7 - Bump Area Versus Coating Thickness

Placement Tack

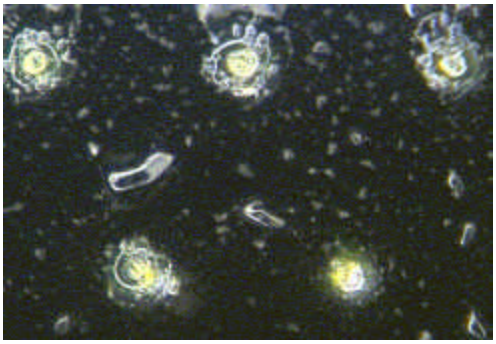
In a conventional SMT process, solder paste provides not only fluxing but also tack to hold the components in place during transfer to the reflow furnace. Flip chip components are normally tacked with flux. With pre-applied underfill, several approaches could be used to hold the flip chip in place. Since the material under study is a fluxing underfill, no flux is needed during assembly, and flux will not be used to tack the chip in place. Instead, the pre-applied coating is formulated to soften at a slightly elevated temperature. In its softened state, the material itself provides the tack needed to hold the chip in place.

Three different approaches could be used to heat the pre-applied underfill in a production environment. The board could be heated, which would soften the pre-applied underfill upon placement of the chip. The drawback to this method is that if the flip chip is on a board with other SMT parts, the paste for those parts could dry out and cause defects. Another method is to pick the part and transport it to a heating station prior to placement. The surface of the pre-applied underfill would be heated directly. This is being studied as a possibility, although the low thermal mass of a flip chip is a potential concern. The final method is to heat the underfill through the chip by using a heated pick-up nozzle. This approach is being studied as well. The target is to be able to heat the chip within the time that it normally takes to flux a flip chip.

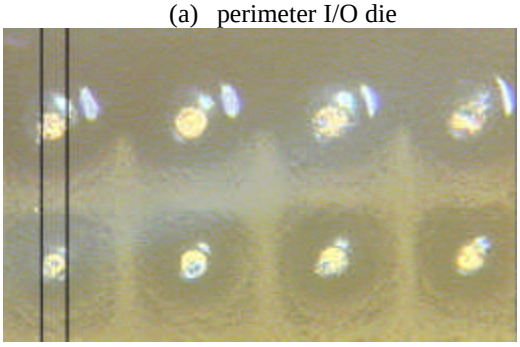
Experiments are underway that examine the effect of temperature and placement force on the tack of the flip chip with pre-applied underfill. To confirm sufficient contact after placement, two experimental responses were devised. First, experiments are carried out on glass substrates for easy visual inspection. Observations were made by examining the contact of the chip to the glass, with a flattened bump appearance indicating sufficient bump-to-pad contact. In addition, chips were placed on test boards

and a die shear tester was used to remove the tacked chips from the substrates. Qualitative data was obtained by examining evidence of the die footprint on the PCB.

These experiments showed that in general, the higher the temperature and placement force, the greater the tack, as expected. Furthermore, the bump configuration on the chip plays a major role in defining the degree of tack. The area array die also showed a significant number of flattened bumps after placement, using the glass slide experiments. This can be seen in Figure 8.



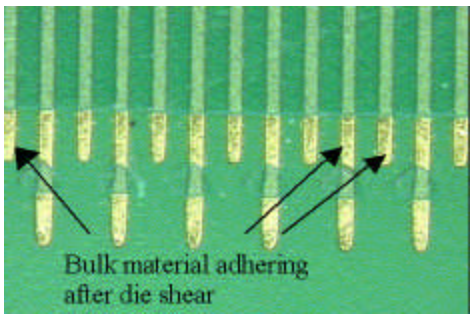
(a) perimeter I/O die



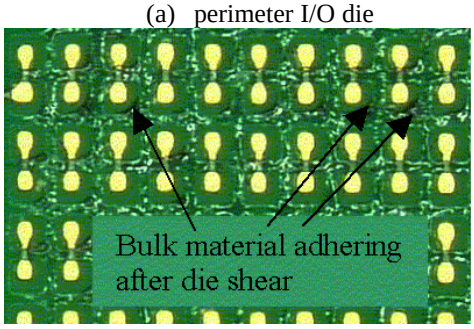
(b) area array die

Figure 8 - Appearance of Chip Tacked to Glass Slide

The area array test die showed greater evidence of adhesion to the PCB than the perimeter I/O chip, as shown in Figure 9. The more effective tack mechanism is associated with the bumps on the die than with the bulk dielectric underfill that coats the remaining open area of the chip. Using sufficient heat and placement force permits adequate tacking of both types of die.



(a) perimeter I/O die

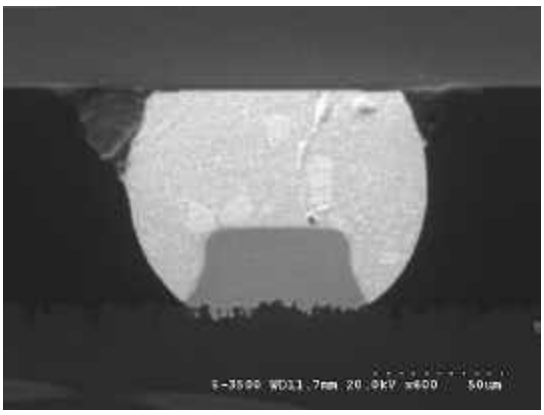


(b) area array die

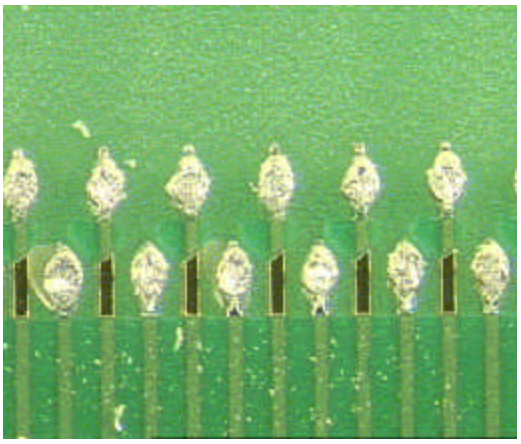
Figure 9 - Appearance of Chip Tacked to Glass Slide

Fluxing Capability

The fluxing action of the underfill printed on the bumps is essential to eliminate oxides and to provide adequate solder wetting to the printed circuit board pad. In addition, it is important that the underfill maintain its efficacy after b-staging and after storing the finished parts. To test the efficacy of the fluxing underfill layer after storage, parts were coated and b-staged, then stored in an inert, dry environment and tested at various time intervals. Testing consisted of assembly of the chips to test boards, followed by die shear to test joint strength and wetting to the PCB pads. After 6 months of storage, the parts were observed to display wetting characteristics equivalent to the initial tests, with no degradation in flux efficacy.



(a) Solder joint formed after storing chip for 6 months

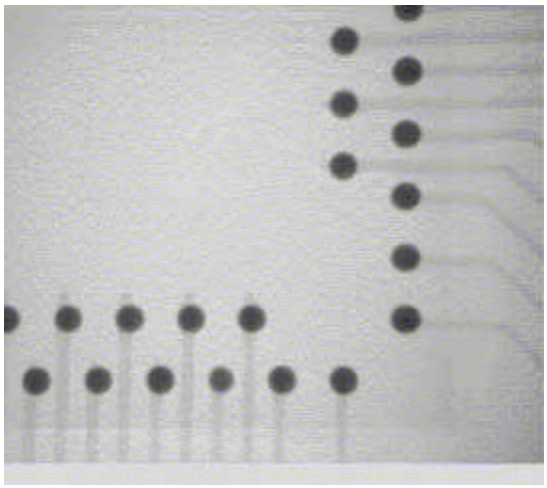


(b) Die shear results for chip stored for 6 months

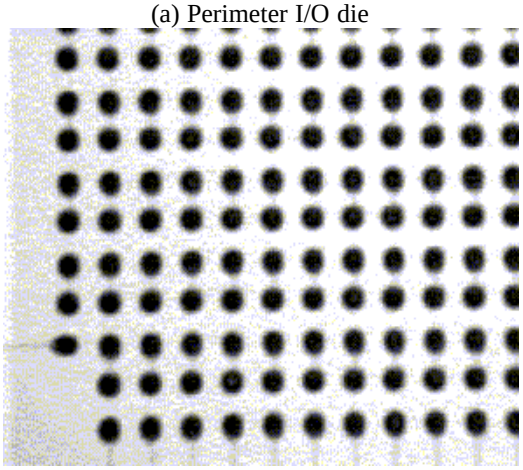
Figure 10 - Flux Efficacy Test Results

Reflow

In order to evaluate the performance of the wafer applied flux underfill materials, both full area array and perimeter I/O test vehicles were built with each test build including several thicknesses of coating on the chips. One hundred percent bump recognition was achieved with area array die, and a slightly lower percentage was observed with perimeter I/O die. This was due to some occurrences of bulk dielectric reducing the bump open area, as was displayed in Figure 7. By looking for multiple bumps at the corners of the die, sufficient alignment of the die can be attained in this case. Figure 11 displays the x-ray images of die registration for assembly. It can be seen that the flip chip bumps are well-aligned with the copper traces on the PCB.



(a) Perimeter I/O die

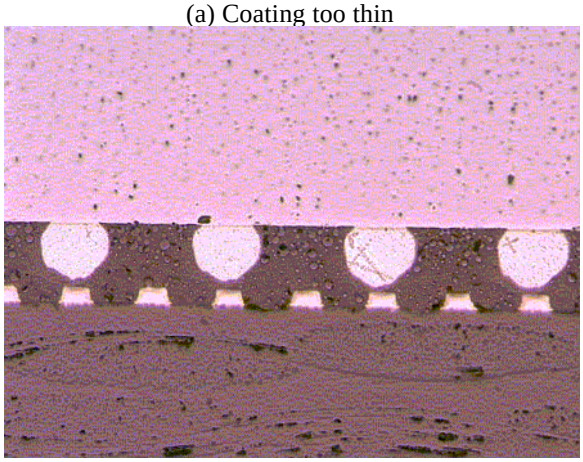


(b) Area array die

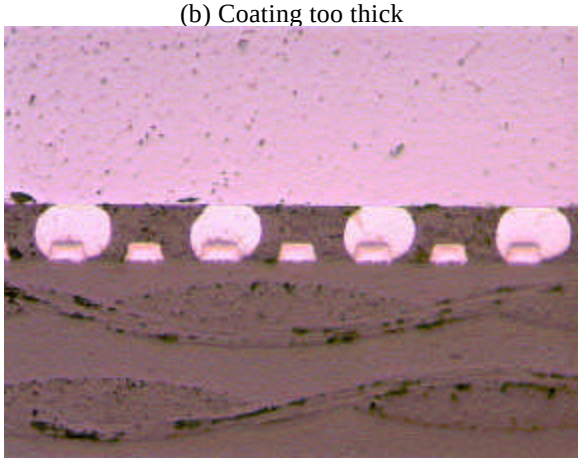
Figure 11 - X-ray Images of Die After Placement

After reflow, parts were cross-sectioned to check the appearance of the solder joints. As can be seen in Figure 12, there is an optimal coating thickness for achieving good solder joints and sufficient contact of the bulk dielectric with the substrate. If the coating is too thin, as in Figure 12(a), there will be gaps in the underfill between the bumps were the bulk dielectric did not contact the board. In Figure 12(b), there was bulk underfill coating the tops of the bumps which interfered with proper joint formation. In 12(c), the coating thickness is sufficient to completely fill the gap between the chip and the board without interfering with solder joint formation.

(a) Coating too thin



(b) Coating too thick



(c) Optimal coating thickness

Figure 12 - Assembly Results Using Die with Various Coating Thicknesses

The experiments to date also have shown that dry storage of the parts will be important. Assemblies built with chips that had been shipped without dry packaging resulted in underfill voids that were not observed when the chips were baked prior to assembly.

Conclusion

Experiments have investigated numerous aspects of the assembly of pre-underfilled flip chip parts, starting with vision recognition at placement through reflow. These results demonstrate a robust process with the potential for high-yielding production assembly. A method for predicting vision recognition has been devised, and one hundred percent vision recognition of coated die was achieved. A method to successfully tack the flip chip in place has been developed, and the influence of several process variables has been examined. It was discovered that the ability to tack the chip at placement depends not only on the placement temperature and force but also on the bump configuration of the chip, with the bumps providing a more effective tack mechanism than the bulk underfill surrounding the bumps. Study of the process variables associated with reflow has been initiated, with early results demonstrating the significance of coating thickness on the final assembly results. Future work will concentrate on full characterization of the assembly process and development of a suitable control plan for production.

Acknowledgements

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Reference

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3. Zhao,R., Zhang, Y., Johnson, R.W., Harris, D., "A Study of Normal, Restoring, and Fillet Forces and Solder Bump Geometry during Reflow in Concurrent Underfill/Reflow Flip Chip Assembly," Electronic Component Technology Conference, Orlando, FL, May 2001.