Chip Scale Package and Flip Chip Assembly Using Tacky Flux

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Introduction

Application of solder paste by using stencil-printing process is a commonly used method for high volume electronics circuits manufacturing. This process has proved to be the fastest and most cost-efficient. Unfortunately this method has shown its limitation for components with pitch smaller than 300 micron. For these components an alternative method is the tacky flux process. It takes place directly on the fine pitch component mounter equipped with flux-dipping unit.

The process stages can be described as follows:

1. Pick up component;
2. Dip component bumps in the flux unit;
3. Place component on the substrate.

The expectation is that this assembly process will allow handling of components with bump pitches down to 100 micron. Therefore it can be extremely interesting for assembly of Flip Chips with eutectic bumps. When FCs with eutectic bumps are placed in solder paste, the position of most components is corrected during reflow, due to the self-alignment of the liquid solder.

Likewise, when components with eutectic bumps are placed in flux, the position of most of them is also corrected, due to self-alignment, but the placement accuracy requirements have not been fully investigated.

This article presents the research findings with reference to the relationship between placement accuracy and formation of solder joints for components with eutectic bumps placed in flux.

Set up

To simplify the execution of the research experiments, it was decided not to use components with extremely small pitches, because of components and substrate availability limitations. Two types of components – CSPs (750µm pitch) and FCs (450µm pitch) were used in the research and the results were extrapolated to components with pitches down to 100µm.

Two different board layouts were used – a copper defined for CSP placement and a solder resister defined for FC (See Figure 1).

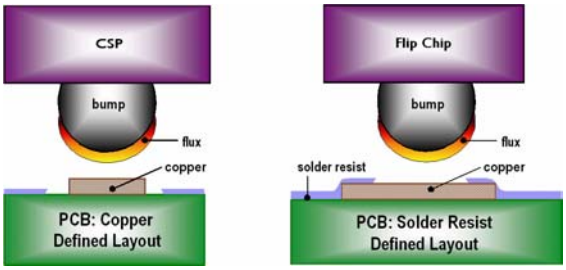


Figure 1 - Copper defined & Solder Resist Defined Layout

The components were placed with Assembléon's Advanced Component Mounter – ACM, which is equipped with a flux-dipping unit. CF2400 Epoxy Flip Chip Flux from Alpha Metals was used in the experiments.

The verification run was done with increasing offsets on respectively three different Cu-pad sizes and three different solder resist apertures. The components were mounted with increasing positive and negative offsets in X-direction. All given offsets were measured from the nominal position. Two test-plans - for CSP and FC were executed. In total 450 CSPs and 450 FCs were placed.

Experiments with CSPs

Flux layer thickness in the flux unit was established at 95µm, which was equal to 50% of the CSP's bump height. The CSPs were first dipped in the flux unit and then placed on the test board with negative and 5 positive offset steps. Per offset step, 15 components were placed on 3 different copper-defined pad layouts:

- Cu pad = bump diameter;
- Cu pad = 85% of bump diameter;
- Cu pad = 70% of bump diameter.

After placement, the boards were soldered and the components were electrically tested. The daisy chain

measurement results are shown with a dashed blue line in Figure 2. In the same figure, the theoretical tolerance positions of the solder resist are given.

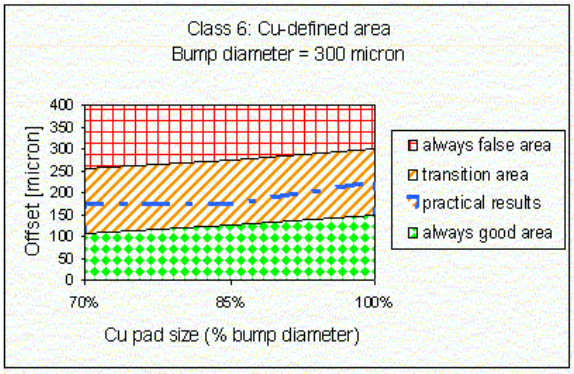


Figure 1 - Placement areas for Cu-defined Footprint

There were three theoretical areas:

- an always good area: This corresponds with the Cu pad or solder area and is a safe area.
- the transition area: This is the tolerance area of the solder resist. When placing here, soldering will be depending on the position of the solder resist.
- an always false area: This is the area outside the solder resist tolerance limit. This results in not soldered connections.

Measurements of several boards showed that the position (tolerance) of the solder resist was not always consistent and could shift in all directions with an offset varying from -30µm to +35µm (See Figure 2).

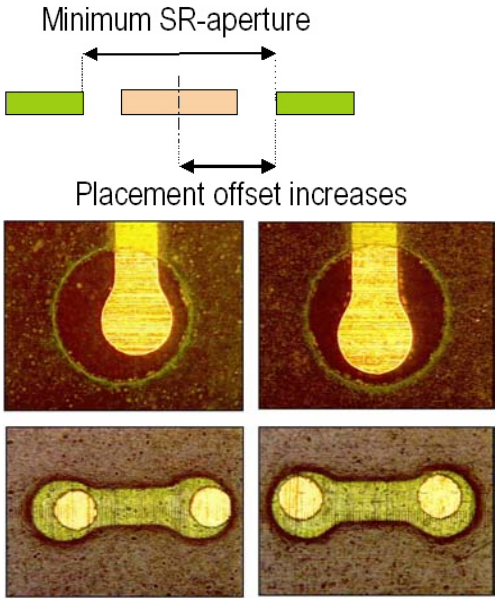


Figure 2 - Shifted Solder Resist

In the position of the bump in relation to the Cu-defined footprint is shown. The upper drawing represents the maximum shift of the solder resist in negative direction and the lower drawing the maximum shift in positive direction.

The maximum allowed placement offset is equal to the Cu-pad size (safe area). The solder resist may not be on the Cu pad and may not be thicker than the Cu-track. In this last case, if the solder resist is shifted to the maximum and if the bump is placed on the Cu-pad edge it will not touch the Cu (See Figure *4*).

The transition area, this is the area in which the solder resist can shift, can increase the allowed placement offset, but this depends on the SR position and the minimum SR-aperture (See Figure 6).

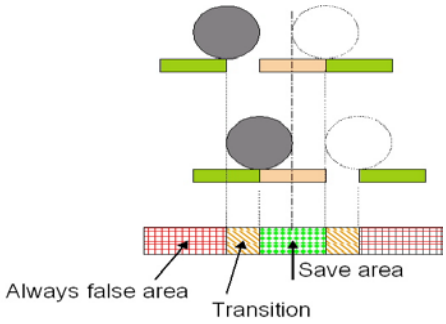


Figure 3 - Placement Limitations for Cu-defined Footprints

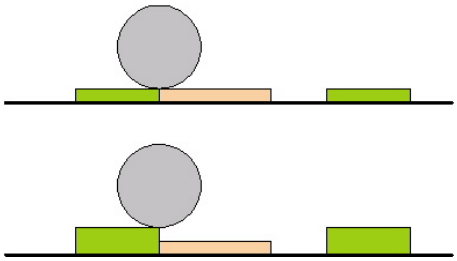


Figure 4 - Bump does not Touch Cu in Case of a Thick SR Layer

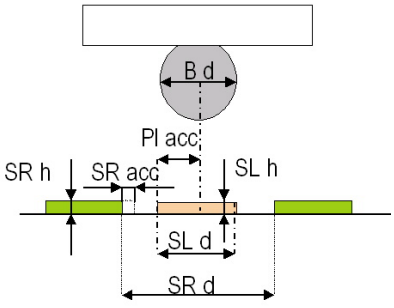


Figure 6 - Nominal SR Position Increases Allowed Placement Offset

In Figure 7 the placement accuracy is given as function of all tolerances.

$$Pl_{acc} = f\,(B_d\,,\, SL_d\,,\, SR_d\,,\, SR_{acc}\,,\, SR_h\,,\, SL_h)$$

Figure 7 - Placement Accuracy as Function of Tolerances for Cu-defined Areas

Conclusions CSP

Based on the research findings for CSPs and Cu-defined footprints with local Cu-defined fiducials, the following can be concluded:

1. When the bump touches the Cu pad area it will always solder during reflow. This is considered as:

Placement Accuracy < $\frac{\text{minimum Cu pad diameter}}{2}$,

2. assuming the solder resist is not thicker than the Cu-pad. This is found under ideal circumstances. Further research is needed to determine a practical limit.
3. At this stage a safety margin of 10% can be suggested. The latter means that placement offset ± 40% off-pad can be recommended.
4. In the transition area not all bumps will solder during reflow. This depends on the solder resist position;
5. When the solder resist is shifted in positive direction, the allowed offset increases in positive direction and decreases in negative direction;
6. When the solder resist is shifted in negative direction, the allowed offset increases in negative direction and decreases in positive direction.

Experiments with FCs

For the dipping of FC dies, the flux thickness in the flux unit was established at 70µm (50% of the FC bump height). The same experiments as with CSP were carried out. FC dies were placed with 5 negative and 5 positive offsets. Per offset step, 15 components were placed on 3 different solder resist defined pad layouts, namely:

- Solder Resist (SR) aperture = bump diameter;
- SR aperture = 85% of bump diameter;
- SR aperture = 70% of bump diameter.

After placement the boards were soldered and after soldering the components were measured (daisy chain measurement). Several boards were used in the experiments.

The position of the solder resist was not the same on all boards, due to the solder resist tolerance. After analysis of the research data the following could be concluded:

The fiducials measurement introduced an extra offset. This offset can increase, compensate or decrease the given offset steps. This explains that for certain offsets in a positive / negative direction soldered / not soldered FCs were found. Also in a wide area soldered / not soldered components were found;

For the tested combination, SR aperture = 70% of the bump diameter, some bumps rested on the solder resist layer and did not touch the Cu. During reflow these bumps did not solder (See Figure 10).

There were two visible theoretical areas:

- a SR aperture area:
- an always false area: This is the area outside the SR–aperture. When placing there, this results in not soldered joints.

Figure 10 shows the position of the bump in relation to the SR-defined footprint and the placement areas.

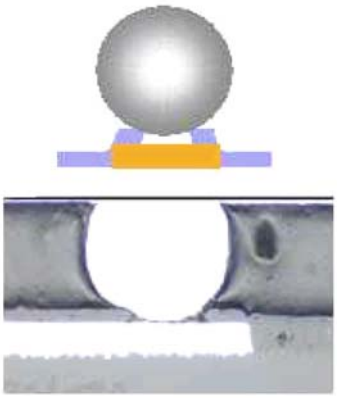


Figure 8 - Solder Resister Aperture is Equal to 70% of Bump Diameter

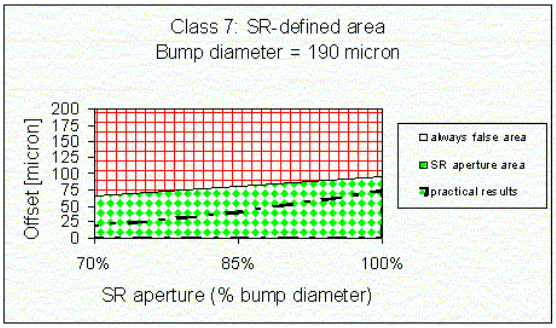


Figure 9 - Placement Areas for SR-Defined FOOTPRINTS

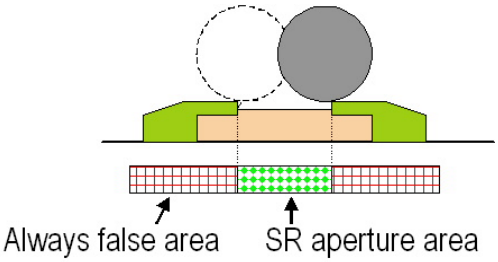


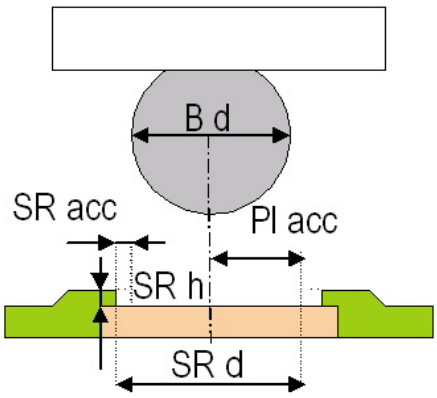
Figure 10 - Tolerance Limits for FC

When a bump is placed on the edge of the solder resist, not all components will flow back to the solder

land. Here a safety margin should be taken into account, depending on some tolerances shows the placement accuracy as function of all tolerances.

In a safe situation, the bump touches the Cu-surface. The SR height plays an important role in the maximum placement accuracy (See Figure 11).

The safety margin depends also on the relation bump diameter and solder resist aperture (See Figure 12).



$PL_{acc} = f (B_d , SR_d , SR_{acc} , SR_h)$

Figure 11 - Placement Accuracy as Function of Tolerances for SR-Defined Areas

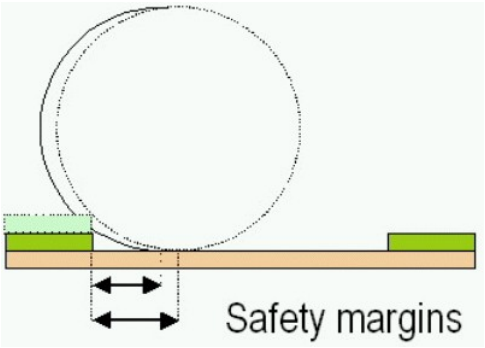


Figure 12 - Safety margin increases for thicker SR Layer

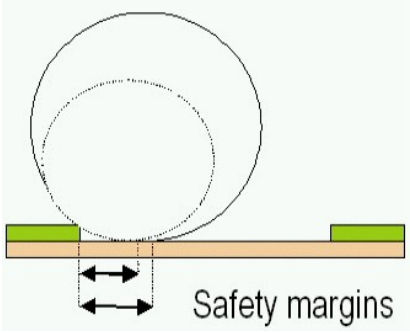
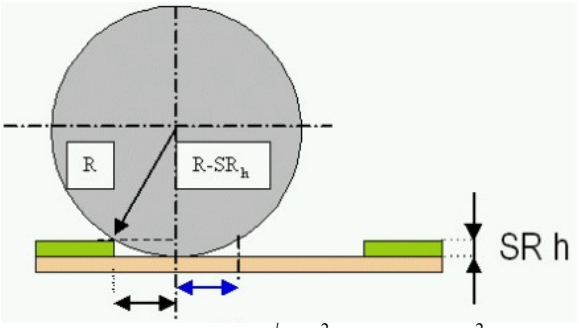


Figure 13 - Safety Margin Increases for Smaller Bump Diameters

If the bump touches the Cu-surface, a safety margin can be calculated (See Figure 13).



Safety margin = $\sqrt{[(R^2) – (R -(SR_h))^2]}$

Figure 14 - Calculated Safety Margin

Table 1 contains the calculated safety margin and placement accuracy for the FC used in the experiments with three different solder resist layer thickness.

Table 1 - Calculated Safety Margins and Placement Accuracy

Bump diameter 190μm		**SR aperture 190μm**	**SR aperture 160μm**
SR layer thickness (μm)	Safety margin (μm)	Placement accuracy (μm)	Placement accuracy (μm)
5	30	65	50
10	42	53	38
15	51	44	29

Conclusions FC

For FCs and SR-defined footprints with local SR-defined fiducials the following can be concluded:

1. There is a strong relationship between bump diameter, minimum SR-aperture and SR height. All parameters play an important role in the maximum placement accuracy;
2. From the results of the performed experiments can be concluded that an allowed offset of 20% from the solder resist aperture is a safe value for the cases the solder resist aperture ≥ 85% of the bump diameter. The solder resist height, in this cases, on the Cu-pad is ≤ 10μm;
3. If the SR-defined fiducials is shifted the SR-defined footprint is also shifted over the same distance. The allowed offset stays the same for a shifted and not shifted solder resist layer;
4. For the tested combination, SR aperture = 70% of the bump diameter, some bumps rested on the solder resist layer and did not touch the Cu. During reflow these bumps do not solder.

Extrapolation Results and General Conclusions

The research revealed that the placement accuracy depends not only on the pitch of the component but

also on the board layout. For copper defined footprints, it can be concluded that the bumps must touch the solder land. Therefore, a placement offset of 40% off-pad can be allowed. For solder resist defined footprints, there is a strong relationship between bump diameter, solder resist aperture and solder resist height. The research findings show that the allowed placement offset is 20% off-solder resist aperture.

The extrapolation of the research results down to pitch size of 100µm are shown in Table 2, assuming that the copper pad sizes should be 70% of the bump diameter for CSPs and the solder resist aperture size should be at least 85% of the bump diameter for FCs.

The recommended placement accuracy for CSP and FC components guarantees the highest process quality. A less accurate placement process will not necessarily result in an error, however the chance for failures will increase.

Table 2 - Recommended Placement Accuracy (in µm at 3σ) for Area Array Components Mounted with Tacky Flux

Pitch Size	CSP on Cu-defined pads	FC on SR-defined pads
Pitch 750 µm	80	50
Pitch 500 µm	70	40
Pitch 400 µm	60	30
Pitch 300 µm	40	25
Pitch 250 µm	-	25
Pitch 200 µm (microprocessors mainly)	-	20
Pitch 150 µm (microprocessors mainly)	-	17
Pitch 125 µm (under development)	-	14
Pitch 100µm (under development)	-	10

References

1. Hans, E., Philips CFT, Placement Accuracy for Components with Bumps Placed in Flux, September 17th, 2001. (Philips Internal Report)

Acknowledgements

1. Peters, M., Philips CFT
2. Borissova, N., Assembléon