Development of Wafer Scale Applied Reworkable Fluxing Underfill for Direct Chip Attach, Part II

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Abstract
Manufacturers of consumer electronic products are continuously striving to confer greater functionality to smaller, lighter, and less expensive packages, and flip chip is an important enabling technology for these product trends. Underfill between the die and an organic substrate is necessary to compensate for the coefficient of thermal expansion mismatch. The underfill dispense step is not a typical process for an SMT factory, and demands additional capital equipment, floor space, cycle time and headcount. These additional investments, plus the inability to rework underfilled parts has limited wide scale implementation of flip chip technology.

The National Institute of Standards and Technology Advanced Technology Program "Wafer Scale Applied Reworkable Fluxing Underfill for Direct Chip Attach" (NIST-ATP WARFU) was established to investigate the development of a flip chip underfill process that would be transparent to the SMT line. The program is supporting the successful development of fluxing, reworkable underfill materials and processes for direct application of the materials to die at the wafer level.

While the application of underfill materials directly to the Wafer seems straight forward, many of the material requirements are incompatible with each other. For instance, the necessity of dicing the wafer using water is not compatible with the use of uncured epoxy materials. In addition, the incorporation of fluxing materials into the bulk underfill is known to degrade long-term stability at room temperature. This needs to be addressed, as the stated goal of the program is to provide at least 6 months of on part life prior to use. The methods and materials used to address these concerns are described in the paper.

Introduction
The underfills that are compatible with the parts being processed have been a goal for some time, starting with the early work of Penissi et al.[1] on underfills pre-applied to the substrate. These early materials illustrated some of the processing advantages inherent in pre-applying material prior to the attachment of the part. The shortcomings of this approach have also become apparent. The materials generally have extremely short pot-life on the order of hours, rather than the desired months. Filling these materials to high levels has also been shown to not be feasible. That is, the maximum incorporation of filler seems to be about 20% by weight, which is not sufficient to affect the CTE significantly. This limits the types of devices that can be used with the pre-applied materials.

Reworkablity of the devices has also been cited as slowing the incorporation into mainstream SMT assembly. All other SMT components are generally considered reworkable by some method. This is especially true with the larger devices such as QFPs, BGAs and most CSPs. Flipchips with either conventional or most Fast Flow Snap Cure (FFSC) capillary flow underfills are not generally reworkable. Recently, the introduction of several commercially available reworkable underfills has presented a solution to these concerns[2]. These materials allow the rework of underfilled flip chips.

All of the components for a wafer-applied material have been identified. The issue is creating one package and providing the user with a material with a robust set of compatible physical properties, which

will provide transparent SMT assembly of flip chips and other components requiring underfill.

General Requirements

It is useful to contrast some of the desired properties of both the cured and uncured wafer applied material with that of commercially available materials. This helps to illustrate the difficulty in achieving the overall goal of the project. Key metrics for the wafer applied material are: robust coating process, stability on part of six months, self fluxing capability, for SMT assembly no post-cure, and void free underfill formation. There are other secondary parameters based on the particular part being placed. It is envisioned that there will be as many variations in formulation and performance for wafer applied (pre-applied) underfills as there are for liquid underfills. The requirements are listed in Table 1.

Table 1 - General Requirements

Property	Value
Shelf life	6 months min
Cure	Reflow, no post cure
Reliability	SMT Board level Min 500 thermal cycles –40-125°C Package level min JEDEC III with 500 TCB
Solder Compatibility	Sn/Pb initial Lead free later

Two-test dies in wafer form were chosen for extensive evaluation. First is a 12-mil pitch dual perimeter 9.3-mm on a side developed by Auburn University. The second die is the FA-10 area array die from Flip Chip Technology. These dies are also 5mm on a side.

Development of Wafer Applied Materials

There are three distinct parts to the development of wafer-applied materials. First, the coating process must be defined and then the chosen process must be further defined to provide a robust process. This process includes choosing the coating thickness, the uniformity on the wafer, the reproducibility of wafer formation and dicing the wafer into individual die.

Second, the underfill material must be developed. Factors that must be considered include generating proper material rheology to provide uniform coating as noted above, as well as proper coloration to provide visual inspection capabilities of the solder balls. This aspect will be discussed in detail in another paper[3]. Finally, the reliability of the wafer-applied underfill on the part must be assessed. This can be accomplished initially by evaluating various aspects of the material, such as adhesion as initially cured, after reflow cycles, after moisture exposure, after JEDEC preconditioning etc. Physical properties of the wafer-applied material, such as modulus, Tg, fracture toughness and CTE, can all be measured without actually using flip chip assemblies. The final conclusion is, of course, the assembly of the flip chips (or CSPs) with the wafer applied underfill into functional interconnect units and then evaluating their performance through thermal cycling, JEDEC preconditioning etc.

As noted one of the key requirements is extended on part shelf life prior to use. Current technology used with liquid fluxing underfills falls far short in providing this stability as these systems struggle to have hours of stability at room temperature, let alone months. Fortunately, since the wafer-applied underfill is pre-applied, a simple yet elegant solution is achieved. The materials of the fluxing layer are separated from the bulk underfill layer, so that on part life is not compromised thus providing an avenue to provide the desired stability. This will be discussed in further detail in the paper.

Materials Development

One of the first conclusions reached in the development of the wafer applied material was that a system in which all aspects of the material, underfill, reworkablity and fluxing action were incorporated into a single material would make the accomplishment of all goals difficult if not impossible. First, the solder balls must be covered with a fluxing material in order to create an electrical interconnection. If the formulation incorporates filler in the normal levels of 40-60% by weight then the solder balls will most likely be covered with filler also. This will prevent interconnection from occurring. Fluxing materials are known to degrade the stability of epoxy-based systems. This means achieving the goal of 6 months of stability would most likely not be achieved. Finally, the reworkable material will most likely be expensive since a custom epoxy monomer will have to be designed and synthesized. Current reworkable monomers break down at around the reflow temperature, which is too low to survive the solder reflow temperatures to which the wafer-applied materials will be exposed.

The solution: separate the different functions by separating the materials performing those functions. This will maximize the opportunity for the wafer-applied material to achieve the desired goals. Thus, two or three distinct materials are dispensed over and around the solder balls, depending on final properties needed to achieve the wafer applied underfilled flip chip assembly.

Materials Development-Fluxing Layer

The first layer applied is the fluxing layer. This material is designed specifically to provide fluxing action on the solder balls and substrate pads. The material can be applied by either stencil or screen-

printing. The material is b-staged prior to application of the next materials. Currently the layer is coated between 10 and 25 μm as the optimum thickness has not yet been determined. The key chemical attribute of the flux layer is providing fluxing action to the solderballs and the pads. The flux material needs to be tough enough to withstand the subsequent coating of the bulk layer, and chemically stable enough to maintain activity for at least six months. The acid number can measure the stability of the system. Any significant drop would indicate instability. So far, one month of the study has been completed successfully. Results are shown in Table 2.

Studies of the fluxing activity have been done by placing and reflow soldering test die coated only with the flux layer. Fluxing activity for at least six months has been demonstrated.

Table 2 - Stability of Flux layer by acid number

Date	Acid Content
Start	23.05 mg KOH/g
1 month	24.27 mg KOH/g

Materials Development Bulk Underfill Layers

This layer provides the overall cured properties of the Wafer Applied Materials System. As such the key requirement for the cured system is to provide adhesion to the component and the substrate as well as good performance through various environmental testing such as thermal cycling, JEDEC preconditioning, HAST etc. For CSPs and BGAs mechanical shock resistance is a key attribute. Matching the CTE to the application is also important. Table 3 lists the typical physical properties of the current bulk layer compared to a Fast Flow Snap Cure underfill and a no flow underfill.

Table3 - Physical Property Comparison

Property	Bulk layer	No Flow	FFSC
Tg(DSC)	134°C	103°C	130°C
Filler Loading	50%	0%	40%
CTE,α1	37	60	35
CTE,α2	108	177	110
Wt Gain 48hr boil	0.7%	3.4%	2.1%
Adhesion	4800	1500	3400

Additional testing has been done on the formulation using a modified lap shear with a nitride-passivated flip chip. The results through different environmental testing are shown in Table 4.

Even this early formulation has excellent properties when compared to the technologies it is designed to replace. It is expected however that the bulk underfill may be a different material, depending on the requirements of each application, i.e. CSP materials will be different than that used on a large ASIC or computer processor.

Table 4 Die Shear Adhesion Bulk Layer

As cured	9600 psi
After JEDEC III (6x reflow)	9800 psi
48 hour boil	6200 psi
96 hour boil	5300 psi

The b-staged layer has requirements that are both different and similar to those of the comparable no-flow or capillary flow underfills. When b-staged the material needs to be tack free at room temperature to allow for easy handling by the placement equipment. This is easily tested with simple tack tests. To tack to the substrate, the b-staged material needs to soften at a reasonable temperature.

As the assembly is heated it is important that the underfill material wet to both surfaces. The ability to wet is easily tested with liquid underfills by simply underfilling an assembled test die. With the pre-applied underfill this is more difficult to judge directly. Contact angle measurements are often used to evaluate the ability of a material to wet a surface. It was observed that the initial formulation wetted more effectively to the die than the substrate. This was confirmed with contact angle measurements. A subsequent formulation with adjusted additives was prepared to improve the wettability to the substrate. This is shown in the Figures 1a and 1b.

Stability of the bulk layer has been demonstrated by storing materials for extended periods of time at refrigerator and room temperatures and then measuring the heat of reaction by DSC. Any reduction in the delta H would indicate advancement of the formulation. Results are summarized in the graph below.

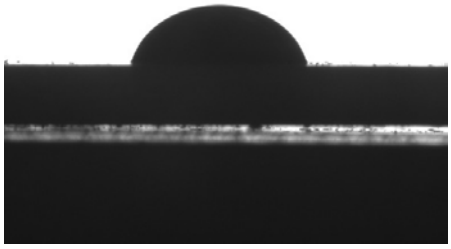

Figure 1a - Before, Contact Angle 71°

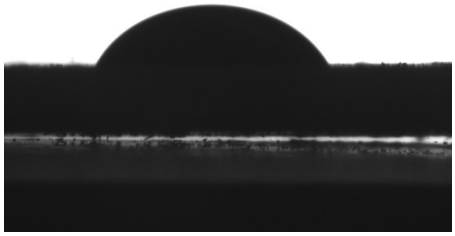

Figure 1b - After, Contact Angle 55°

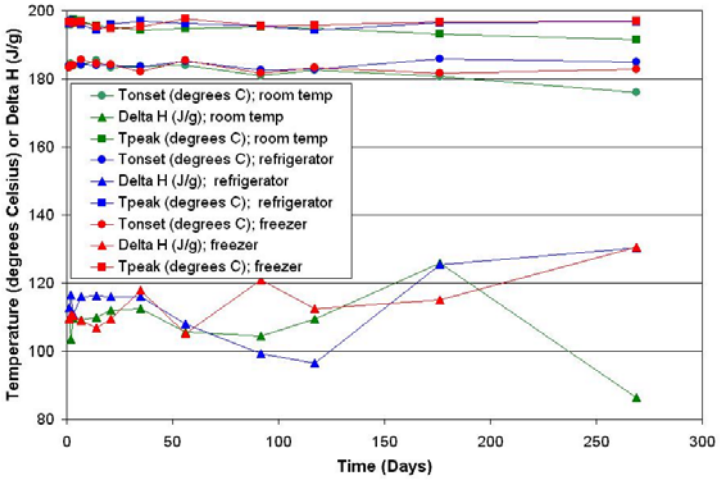

Figure 2 - Stability of Bulk Underfill

Coating-Flux Layer

Uniform coating is the first step in the successful implementation of any pre-applied system. The coating process has to provide uniform coating across the individual die, wafer and finally wafer to wafer. One of the first issues to be addressed is the dicing of the wafer, before or after coating. While it is possible to dice through uncured underfill material, in so doing the uncured material is exposed to water used to cool the saw blade. The uncured material being an epoxy-based system will absorb at least some of the water leading to the potential for void formation during the reflow of the die. Thus, the decision was made to dice the wafer prior to coating. This required the coating method chosen to provide direct imaging of the saw streets, as no further processing of the wafer will be done after coating and b-staging. The flux layer has to be applied only to the solder balls in an amount sufficient to provide fluxing to the pad and the solder balls. It was found that the fluxing layer could be applied with either a screen or a stencil identical to that normally used to apply paste. Figures 3 and 4 show the flux layer on the solder bump. Figure 5 shows the thickness distribution of the bumps after coating illustrating the uniformity provided by the coating methodology.

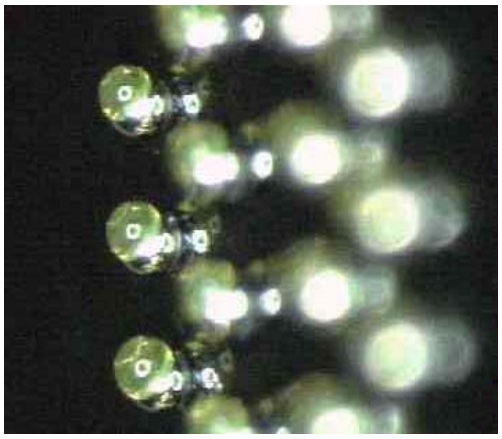

Figure 3 - Flux Layer on Solder Bump

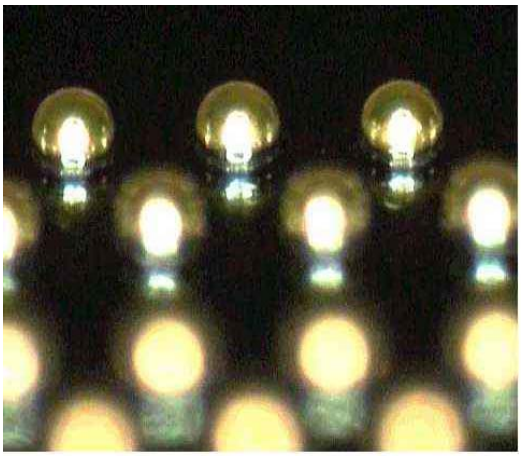

Figure 4 - Flux Layer on Solder Bump

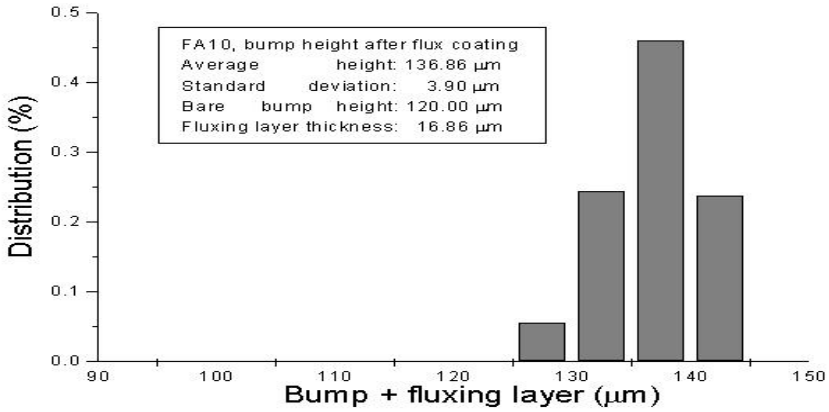

Figure 5 - Bump Height After Coating

Coating-Bulk Underfill Layer

The bulk underfill materials are coated after the fluxing layer is b-staged. The coating technique is a modified stencil print, as described above. The end result of the coating is such that the saw streets are kept clean and the solder balls do not have any bulk layer over the top of the solderballs. In fact it has been determined that the solderballs themselves must be exposed to the vision system to have the component placed accurately.

The requirements are such that the process has to provide the above definition. This eliminates such bulk coating methods such as spin coating or curtain coating unless a secondary imaging step is done after coating. Based on the chemical requirements it was felt that such an approach would add significant complexity to the chemistry as to make it unattractive.

There are a number of coating methods that are widely used today that provide direct imaging of materials. The most successful method tested to date is a modified stencil approach. The stencil is designed to allow coating of the wafer while imaging the saw streets with the stencil pattern. The tops of the die are kept clean by the nature of the stencil process itself. The flux layer is tough enough to resist the squeegee and remains on top of the solder ball. Coated wafers are shown in Figures 6 and 7 below.

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Uniformity of application is critical to the success of the approach. Figure 8 shows the thickness profile of the FA-10 die.

Uniformity over the entire wafer is also required. Figure 9 shows the measured thickness distribution on a diced wafer. The average thickness is just under 110 µm with a standard deviation of 5.7 µm.

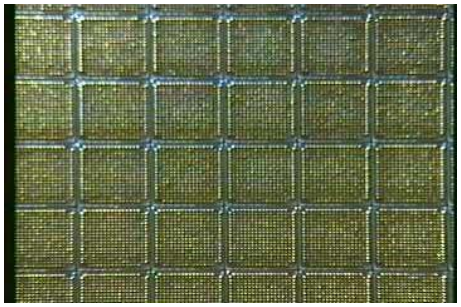

Figure 6 - FA-10 Coated with Both Flux and Bulk Layer

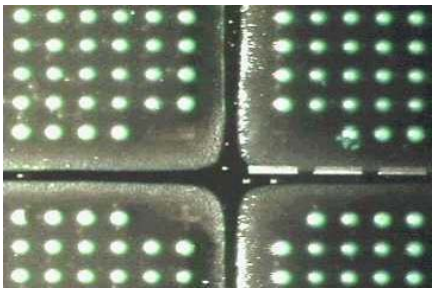

Figure 7 - Closeup of FA-10 Illustrating Clean Saw Street

Figure 8 Thickness Scan of FA-10

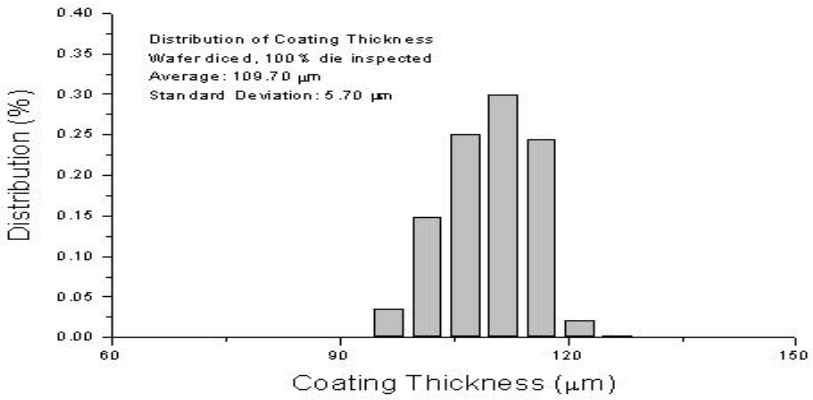

Figure 9 - Coating Thickness Distribution

Conclusion

While considerable progress has been made in defining the coating process, future work determining overall wafer-to-wafer consistency needs to be proven. This work has already been started. The process needs to be extended to wafers larger than 5 inches as well as to CSP and BGAs. Much of this work has been started and results should be available soon.

Initial physical testing of the underfill is extremely promising. More work to improve the cure cycle as well as tailoring individual formulations to specific applications is ongoing.

Initial assembly of the applied underfill system has been performed. Initial feedback is encouraging and will be discussed in detail in the presentation "Assembly of Flip Chips Utilizing Wafer Applied Underfill."[3.]

Acknowledgements

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1. US Patent 5,128,746 Pwnnissi et al
2. Loctite Underfills 3567,3568
3. Danvir et al, Assembly of Flip Chips Utilizing Wafer Applied Underfill, APEX 2002