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Effects of Substrate Design on Underfill Voiding Using the Low Cost, High Throughput Flip Chip Assembly Process and No-Flow Underfill Materials

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Abstract
The formation of underfill voids is an area of concern in the low cost, high throughput, or "no-flow" flip chip assembly process. This assembly process involves placement of a flip chip device directly onto the substrate pad site covered with pre-dispensed no-flow underfill. The forced motion of chip placement causes a convex flow front to pass over pad and solder mask-opening features promoting void capture.

This paper determines the effects of substrate design on the phenomena of underfill voiding using the no-flow process. A full-factorial design experiment analyzes several empirically determined factors that can affect void capture in no-flow processing. The substrate design parameters included pad height, solder mask opening height, pad/solder mask opening separation, and pad pitch. The process parameters include chip placement velocity and underfill viscosity.

The process robustness is measured in terms of the number of voids created during chip placement, and is further analyzed for the location and any visible modes of void formation. The goal of the work is to determine improved substrate designs to minimize voiding in flip chip processing using no flow underfills.

Introduction
The high throughput flip chip assembly process, or "no-flow" process has significant potential to displace conventional flip chip processes for consumer electronics and mobile applications. Reasons for this include the elimination of several processing steps, the reduction of process complexity, reduction of capital equipment requirements, reduction of equipment maintenance, and enhancement of process robustness. Cost modeling and analysis comparing a typical industry flip chip process, the low cost high throughput (no-flow) process, and surface mount assembly[1, 2] quantitatively describe how the no-flow process potentially enhances profit margins. Therefore, much research has been conducted to develop the process and the corresponding materials.

The no-flow process involves a compressive flow of the underfill between the chip and substrate during placement. The resultant flow front is therefore a convex surface moving outward from the central dispense point between the chip and substrate. This flow front crosses dense and often irregular patterns of bumps, substrate metallization and solder mask openings on the surfaces of each component. This flow front is forced into and around these features and therefore, unlike the concave flow front of capillary processing, does not as easily fill the entire gap between the components. Thus, voids are more easily formed in the resultant underfill matrix.

Several parameters have a high probability of effecting voiding in no-flow processing. Substrate design variables such as pad height, solder mask-opening height, pad/solder mask opening separation, and pad pitch potentially increase voiding in the underfill. Additionally, processing parameters such as chip placement speed and underfill viscosity affect the flow front speed and geometry (curvature) and thus potentially increase voiding in the underfill.

Experimental Procedure
The experiments focused on critical design and process parameters which impact voiding in no-flow underfill processed assemblies. The parameters were tested by varying the test vehicles for each combination of substrate design parameters and process conditions according to a full factorial experimental design.

The experiments essentially involve initial controlled dispense of no flow underfill onto substrates having specially designed pad and soldermask test patterns.

This is followed by controlled placement of a transparent glass chip upon the pad site through the pre-dispensed no-flow underfill. The subsequent flow of the underfill is carefully recorded as it is compressed beneath the descending chip and the resultant numbers of voids are logged and analyzed.

The response variable is defined as the number of voids created in the process divided by the number of pads in the site. This makes a dimensionless response variable for the purpose of the experimental analysis that is termed the "void ratio". Void ratios are recorded for each zone and zone sub-category of each assembled site to allow for improved evaluation of the tested factor effects. The voids are also qualitatively analyzed for size and visible modes of void formation.

Test Vehicle Description

The test vehicles used in the experiments were substrates with varied patterns of copper pads and solder mask openings according to the experimental design criterion. The substrates were 0.1cm thick FR4 composites 30 cm X 30 cm in dimension. Each substrate consisted of 9 sections of unique pad pitch (three levels) and pad/solder mask (three levels) separation distance designs. Each section consisted of 15 replicate sites of pad and mask opening arrays. Eight substrates were included to allow for four levels of pad height and two levels of solder mask height. The entire set of test vehicles thus consisted of 72 unique sections of 8 replicated sites or 576 test sites.

The substrates for the tests were designed and manufactured at Georgia Tech's Packaging Research Center to ensure process control. Four copper pad heights were implemented using the designed pattern onto 4.5, 9, 13.5, and 18-micron thick copper-coated FR4 substrates. Two solder mask opening height levels were incorporated as 8 micron and 18 microns. Three pad/solder mask separation distance levels of 0, 25.4, and 76.2 microns were designed into the copper and solder mask arrays. The designed pad pitches were set to 152, 254, and 406.4 microns in the masks. Figure 1 shows a typical substrate test site and a typical pad feature.

Each substrate utilized different mask and copper thickness thereby incorporating pad and solder mask variations with each different substrate. Four zones were implemented for each site. Each site was of a unique geometry and orientation of mask openings. The four zones were: 1. Rectangular pads and openings with a uni-directional orientation of the opening (separation of mask and pad edges on two sides of each pad), 2. Rectangular pads and openings with an omni-directional orientation of the opening (separation of mask and pad edges on all four sides of each pad), 3. Circular pads and openings with an omni-directional orientation of the opening, 4. Control zone. No pads or mask openings present. Each site and zone was further differentiated into "inner", "middle", and "outer" regions based respectively upon the areas of initial underfill dispense, compressive underfill flow over features, and the outer chip and fillet areas. Figure 2 shows schematics of the varied parameters of test site features. Figure 3 shows the breakdown of the test site into zones and regions.

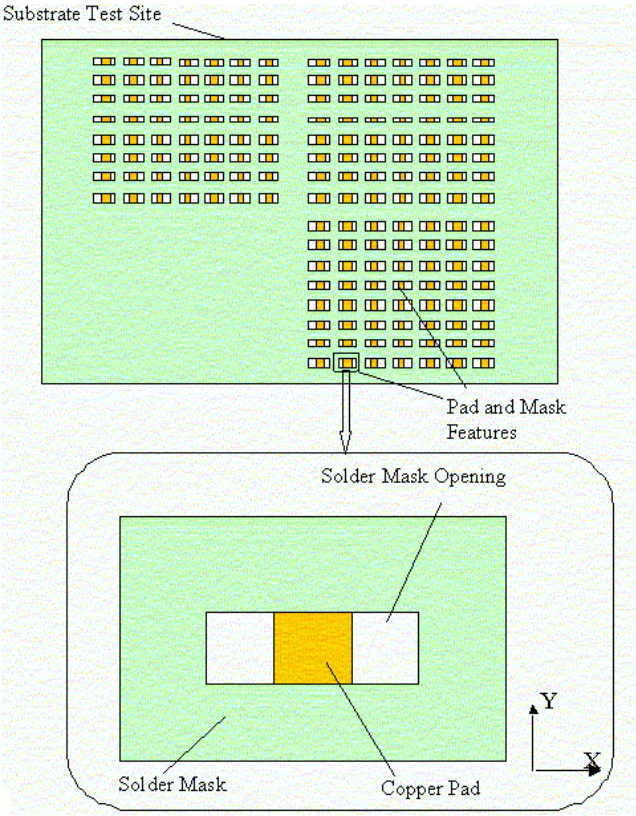

Figure 1 - Typical Substrate Test Site and Feature

Transparent glass chips were used for simulated chips as shown in Figure 4. The chips were 1.78 mm X 1.27 mm plate glass with 1 mm thickness. The chips were not bumped, and the offset gap between chip and substrate was maintained with .02 mm thick double-sided tape placed in strips alongside two edges of each test site.

Assembly Process

The test vehicles were assembled using a fixed no-flow assembly process to maintain consistency throughout the experiment as shown in Figure 5.

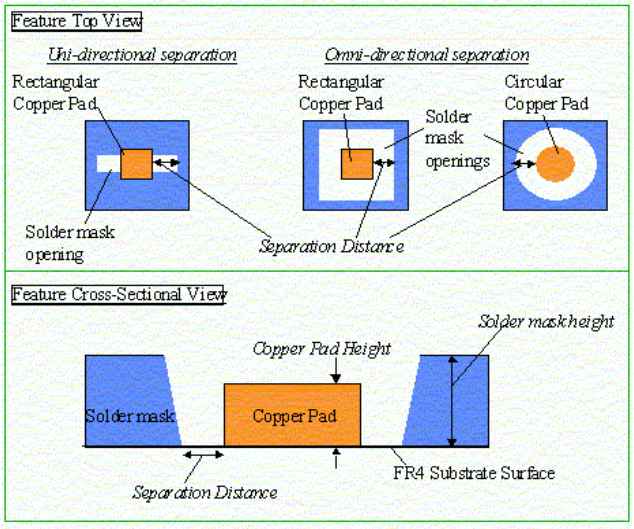

Figure 2 - Schematics of Substrate Design Factors Varied in Experimentation

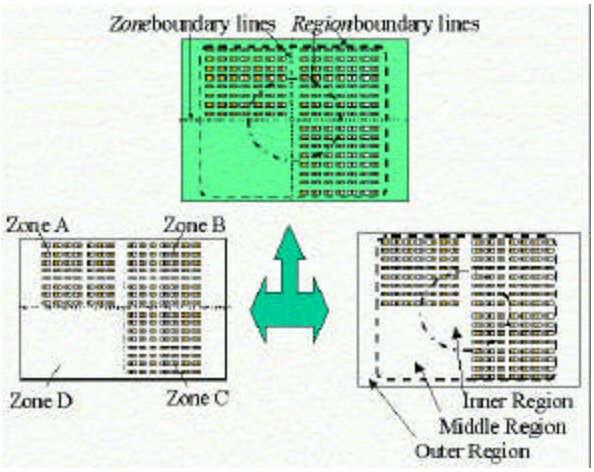

Figure 3 - Test Site Zones A, B, C, and D and Inner, Middle and Outer Regions

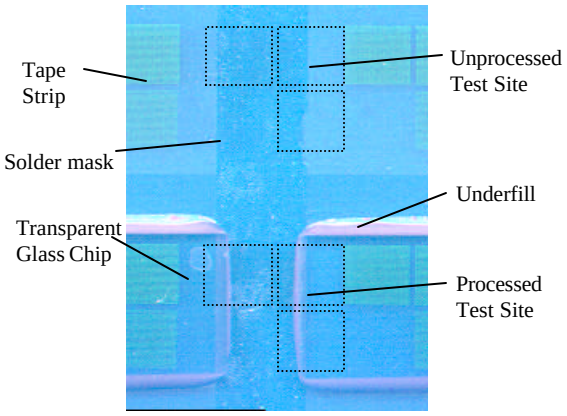

Figure 4 - Assembled Test Substrate Site with Underfill Dispensed and Glass Chips Placed

One of the two-tested underfill materials was dispensed by a Camelot 3700 dispense system on the center of the test site (.040 g) filling the inner region. The substrate was then placed in a Summit 100HR SRT Rework station for glass chip bonding. The bonder then picked up the pre-cut glass chip and placed it directly onto the site with the appropriate velocity setting depending on the selected value in the experimental design. The specific test vehicles of each design and process parameter were assembled in a randomized order defined in the full-factorial experimental design. Figures 6 and 7 show the assembly process with two sequential micrographs during chip placement and underfill flow approximately 0.283 seconds apart.

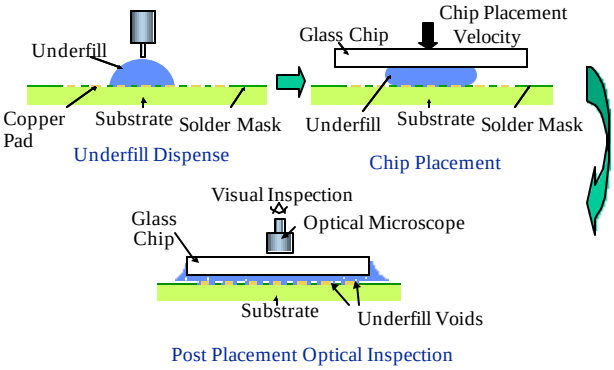

Figure 5 - Chip Attach Test Process and Response Observation

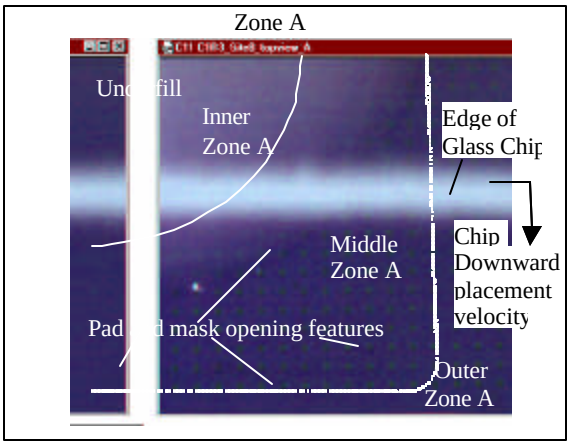

Figure 6 - Placement Process of Glass Chip On Test Site with Underfill Pre-dispensed at the Center (Inner Zones)

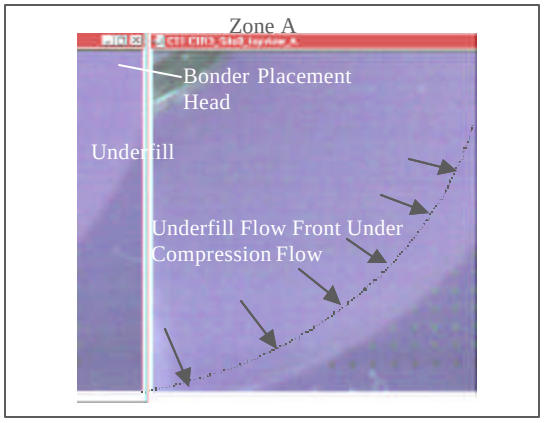

Figure 7 - Placement Process of Glass Chip on Test Site (0.283 seconds after Figure 6). Underfill Compressed Under Chip Inducing Flow Front Over Pads

Enhanced images of the assembled parts were observed through the transparent top surface of the glass chip and captured with a 5X optical microscope. Additional sets were captured using a 10X high speed digital camera to preserve real time pictures showing void capture and a 20X digital Polaroid camera for sample pictures of capture voids after assembly.

Analysis Procedure

Several of the factors studied in the design of experiments were found to have profound impacts on the numbers and sizes of voids captured during processing. The effects of each factor and second-degree factor interaction will be discussed in this section.

All void totals and approximate sizes were entered into a commercial experimental design software for statistical analysis. Each factor was analyzed for main effects and second-degree interaction effects on the response variables. The main effects analysis essentially involved an analysis of the variable response relative to changes in each factor (i.e. “mask height”) independent of the other factors. The factors were then analyzed to determine significant interactions.

The response variables were defined as “total void ratio”, which was further subcategorized into “outer void ratio”, “middle void ratio”, and “inner void ratio”. The void ratios were defined as the total number of voids in the respective region (reference Figure 3) divided by the total number of pads within that region to give unit-less responses. Void totals were found through visual inspection of the test vehicle through the transparent glass chip following assembly.

Results and Discussion

Factor Effects Analysis on Total Void Ratio Response

Several of the factors studied were found to have significant main effects in the initial analysis. Total void ratio was found to be generally increasing with increasing value of solder mask thickness, increasing mask/pad separation distance, and chip placement velocity. These trends indicate large, deep cavities tend to promote void capture, particularly when the die is placed rapidly onto the test site. However, analysis of variance results revealed interaction effects to be prominent in the void ratio response. Therefore, analysis of the interactions between the variables is necessary to realize their accurate effects upon void ratio. Table 1 shows the effects of the tested factors and interactions on total void ratio.

Mask height has significant interaction effects with copper height. The extreme levels of copper height increase void ratio for the thick solder mask height. In addition, increases in separation distance between pad and mask opening edges increases the void ratio at a greater rate as solder mask height is increased.

Copper pad height also has a significant interaction effect with separation distance. This effect is localized as an increase in void ratio for the minimum levels of pad height and separation distance. This effect supports the probable explanation presented in the paragraph above.

Separation distance provides a significant interaction effect with feature pitch. A low separation distance and low feature pitch combination results in a relative decrease in void ratio. However, involvement of feature pitch implies the reduction in void ratio may simply be a density reduction of voids due to the higher probability of the increased numbers of voids conglomerating to form slightly fewer voids. The increased void numbers would have relatively fewer obstacles to overcome to join together when present at a low separation distance. A moderate separation distance provides the smallest holes in which voids could be gathered more closely than in the other separation level sites.

Separation distance also has a significant interaction effect with placement velocity. These factors appear to magnify the void ratio as both are increased in level. Thus, increasing both factors results in effectively combining both like main effects to increase the void ratio.

Table 1 - Summary of Main and Interaction Factor Effects on Total Void Ratio

Source Factor	Ranked Significance
Mask Height**	+
Mask Height & Mask/Pad Separation	+
Mask/Pad Separation**	+
Cu Height & Underfill	+
Mask Height & Cu Height	+
Cu Height & Mask/Pad Separation	+
Place Velocity**	+
Mask Height & Underfill	+
Underfill & Place Velocity	+
Mask/Pad Separation & Feature Pitch	+
Cu Height**	+
Mask/Pad Separation & Place Velocity	+
Mask Height & Zone	o
Cu Height & Feature Pitch	o
Cu Height & Zone	o
Mask Height & Feature Pitch	o
Feature Pitch & Zone	o
Feature Pitch**	o
Zone**	o
Cu Height & Place Velocity	o
Mask/Pad Separation & Underfill	o
Feature Pitch & Underfill	o
Underfill**	o
Mask Height & Place Velocity	o
Mask/Pad Separation & Zone	o
Feature Pitch & Place Velocity	o
Underfill & Zone	o
SignificanceTable Legend	Symbol
Significant Factor Set	+
Not Significant Factor Set	o

**Main effects significance subject to analysis of interaction effects for confirmation

Underfill has a significant interaction effect with copper height. Underfill 1 has increased voiding for lower copper heights. In contrast, Underfill 2 has increased voiding for higher copper heights, making broad conclusions about all no-flow underfills erroneous.

Underfill also has a significant interaction effect with placement velocity. Both underfills tested show increased voiding with increased placement velocity. Underfill 1 shows a higher sensitivity to placement velocity and results in a greater increase in void ratio as velocity is increased.

Factor Effects Analysis on Outer, Middle, and Inner Void Ratio Responses

The auxiliary response variables of Outer, Middle, and Inner Void Ratios were correlated with Total Void Ratio. The results provided significance data on the effect of zone on the relative proportions of numbers voids that remain near the pad sites to numbers of voids swept outward from the pads during no-flow processing. The mean Middle and Outer void ratios relative to each zone are listed in Table 2.

Table 2 - Zone effects on Middle and Outer Void Ratios

Zone effects on Middle Void Ratio	
Source Factor	**Mean Middle Void Ratio**
Zone A	0.26
Zone B	0.17
Zone C	0.15
Zone D	0.00
Zone effects on Outer Void Ratio	
Source Factor	Mean Outer Void Ratio
Zone A	0.08
Zone B	0.12
Zone C	0.16
Zone D	0.00

The data indicates Zone A has the highest number of capture voids remaining near the pads after chip placement. Excluding the control zone D, Zone C has the fewest number of voids remaining near the pads after chip placement. Zone B fell between zones A and C. These relative differences across the zones have interaction effects as well. These relative differences in these void ratios are increased with increased solder mask thickness, and separation distances. Figures 8, 9, and 10 show sample views of capture voiding near the features of Zones A, B, and C, respectively. In sum, zone A possessed rectangular, unidirectional features that caused increased amounts of voiding near the features.

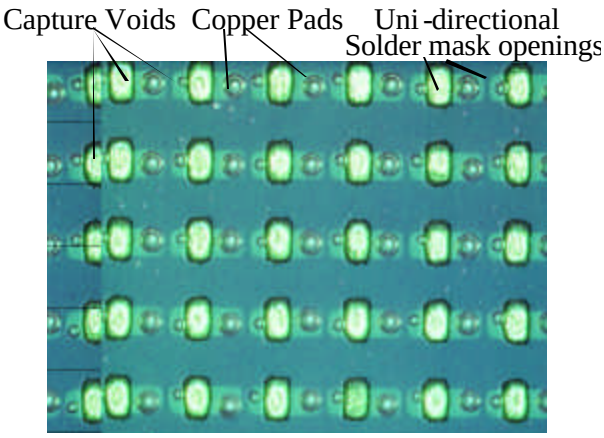

Figure 8 - Sample View of Middle Zone A Capture Voiding

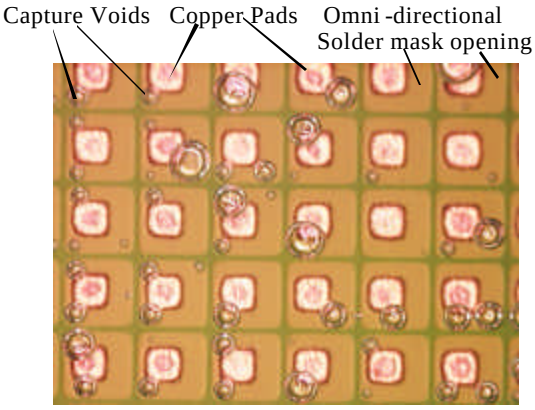

Figure 9 - Sample View of Middle Zone B Capture Voiding

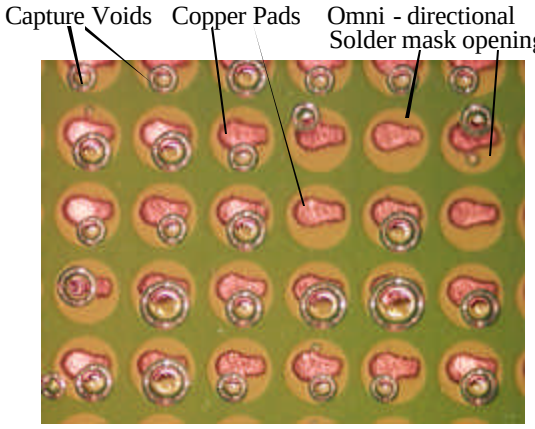

Figure 10 - Sample View of Middle Zone C Capture Voiding

Analysis of variance of the factors on inner void ratio revealed significant main effects with placement velocity and feature pitch. Increases in either placement velocity or feature pitch resulted in significant increases of inner void ratio. These factors also had a significant interaction effect with each other, magnifying inner void ratio with their combined effect.

Observations during experimentation revealed an increased amount of voids captured between the chip and underfill with higher placement velocity. Thus, voids found in the inner region were not captured or located on the substrate features, but rather by capture between the chip and the underfill interface.

This chip/underfill capture phenomena is supported by the main effect of substrate feature pitch. Increasing feature resulted in increasing mean inner void. Division of inner void response by the numbers of pads present in the inner zone regions yielded numbers within 27% of each other thus signifying the feature pitch has less of an effect on void totals in the inner zone region.

Compression Flow Analysis

An analysis of the fundamental properties of viscous fluid flow was conducted to determine the physics behind void capture observed in the experiment. The high throughput flip chip process involves underfill flow between the chip and substrate by compression induced between the two surfaces as the chip approaches the substrate. The chip requires placement force to push down through the viscous underfill until the chip contacts the substrate. The placement force is induced by a pressure differential in the underfill material that results from a convex flow front in the underfill material surface adjacent to the surrounding atmosphere. This convex flow front has a significant potential to cause void capture in features such as interconnect pads and solder mask openings present on the substrate interface. Figure 11 shows the equivalent approximation of the flip chip package with two parallel circular plates with a viscous fluid squeezed between them.

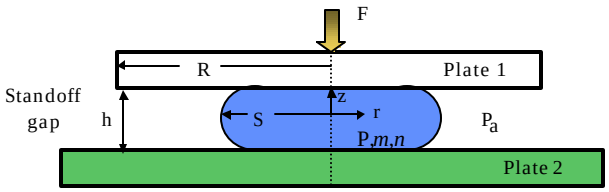

Figure 11 - Compression Flow between Equivalent Circular Parallel Plates

The analysis approximates a quasi-steady state, symmetric, and inertia free flow of a shear-thinning, power law fluid. The fundamental momentum equations and shear stress components reduced to the solution of a radial fluid velocity profile of equation 1. The terms *h, n, m, P, r, and z* represent the offset gap height, power law index, consistency index

(apparent underfill viscosity), pressure, radial position, and z-coordinate respectively.

$$v_r = \left(\frac{h}{2}\right)^{1+1/n} \frac{1}{1/n+1}\left(-\frac{1}{m}\frac{dP}{dr}\right)^{1/n} \cdot \left[1-\left(\frac{2z}{h}\right)^{1+1/n}\right]$$

The fluid velocity distribution revealed both the convex shape of the flow front and the relative dependence upon placement velocity and underfill viscosity. In summary, increased placement velocity and decreased underfill viscosity resulted in increased flow front curvature and extension which is proportional to the probability of void capture within an aperture on a substrate or chip face. These findings support the experimental results where increased placement velocity and decreased underfill viscosity provided relatively lower void ratios.

Conclusions

In this work, the primary factors influencing void formation in no flow underfill processing have been determined with respect to substrate design factors and assembly process parameters. Some of the key factors are the solder mask thickness relative to the substrate and copper surfaces, the separation distance between copper pad and mask opening edges, pad and feature shape, and chip placement velocity. Combining the minimum values of mask height, copper pad height, and separation distance factors provides an effective minimum in the size of the aperture at the pad sites including a relatively shallow hole depth and no region of extended depth surrounding a pad hence tends to minimize void formation.

In summary, the void ratio is effectively minimized by minimizing aperture depth of the solder mask opening, separation distance between copper pad and solder mask opening edge, and placement velocity. Metal-defined pads should be fabricated with minimal mask opening depths and lateral dimensions as well as minimal copper pad heights. The pads and mask openings should be circular to minimize the numbers of voids that shall remain near the pads.

The results of this study are fundamentally accurate for conventional flip chip packages using bumps on the silicon interface. Bumps on the chip interface were evaluated to provide potential for void capture at the silicon interface adjacent the bumps, but any formed voids are usually swept outward from the bumps to the underfill fillets during chip placement. This analysis would be tested in subsequent experimentation.

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References

1. D.F. Baldwin, and N.W. Pascarella, "Advanced Encapsulation Processing for Low Cost Flip Chip Assembly-A Cost Analysis," *3rd Intl. Symp. Adv. Pack. Matls. Proc. Prop. and Inter.*, Braselton, GA, March, 1997.
2. D.F. Baldwin, and L.P. McGovern, "High-Throughput, low-cost flip chip-on-board assembly," Electron Packaging Prod, Vol. 38, No. 2 (1998), pp 68-76.
3. R.B. Bird, R.C. Armstrong, and O. Hassager, Dynamics of Polymeric Liquids, Vol. 1: Fluid Mechanics, John Wiley & Sons(New York., 1977).
4. R. W. Fox, A.T. McDonald. Introduction to Fluid Mechanics, Fourth Edition. New York 1992.
5. A. J. Hayter. Probability and Statistics For Engineers and Scientists. PWS Publishing Company (Boston MA, 1996).
6. J.H. Lau (Ed.), Flip Chip Technologies, McGraw-Hill (New York, 1996).
7. P.J. Leider,; R.D. Bird "Squeezing Flow between parallel disks. I Theoretical analysis", Ind. Eng Chem., Fundam., 13 (1974), pp. 336-341.
8. J. Neter, M.H. Kutner, C.J. Nachtsheim, and W. Wasserman. Applied Linear Statistical Models, McGraw-Hill (Boston MA, 1996).
9. L.P. Thorpe. "High Throughput Flip Chip Assembly Process and Reliability Analysis Using No-Flow Underfill Materials," MSME Thesis, School of Mechanical Engineering, Georgia Tech, Atlanta, GA. 2000.
10. R. Tummala, E. Rymaszewski, A. Klopfenstein, "Microelectronics Packaging Handbook", Second Edition, Part I, II, III, 1997.