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Advanced Laminate and Prepreg for PWBs with Embedded Components

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Abstract
The technology for embedding components in PWBs will change the process how PWB are fabricated over the next few years. At the present time, polymer thick film is the most frequently used material to embed "passives" in PWBs. However, these do not meet the stringent tolerances that will be needed in the future and will be replaced by new materials based on ceramic, thin film or even with silicon. The coefficient of thermal expansion (CTE) of such new technology embedded components is, in most cases, lower compared to the CTE of standard glass-reinforced materials used today. In addition, the distance between the component lead and the PWB connection will be shorter and will thus absorb less stress. For the effective use of embedded components, the dielectric thickness between the conductive layers will be reduced. High dielectric strength, CAF resistance and low migration are required, while resin recession cannot be accepted on plated inner via holes. This paper explains the impact of CTE imbalances caused by the different materials used in a PWB. It also provides guidance on how PWB manufacturing process can be modified to accommodate the new requirements from the PWB fabricators, assemblers and OEMs. These requirements are for high dimensional stability of the laminate and prepreg to improve manufacturing yields during bare PWB fabrication, during assembly and during the life cycle of the electronic device in the field. The paper also explains the risks of metal migration and conductive anodic filaments (CAF) in PWBs and the need for lower dielectric constant (Dk). The new materials are processable in standard PWB fabrication lines and can accommodate the needs engendered by halogen-free resin systems.

Introduction

The introduction of chip-size packages (CSPs) has considerably increased the wiring density of PWBs, a technology made possible by micro-via holes. The reduction in pitch sizes to less than 0.8 mm and the increased number of I/Os has doubled the number of micro-via layers on each side of the PWB from one to two. This is because, due to the small distance between the solder lands on the external layers, this area is no longer available for conductor routing. Meanwhile, larger areas of silicon are being used inside component packages and the area of the packages is being better used. The distance between the contact areas of the Interposers and the printed circuit board are becoming smaller, so the mismatch between the CTEs of the printed circuit board, the component housing and the silicon must be compensated for over an ever shorter distance. When embedded components are used on the board, the situation becomes even more difficult. The chips no longer have an Interposer linking them to the board, and they are connected directly to the PWB. This paper tries to explain, what materials are needed in the future to bring the PWB in line for use with embedded components.

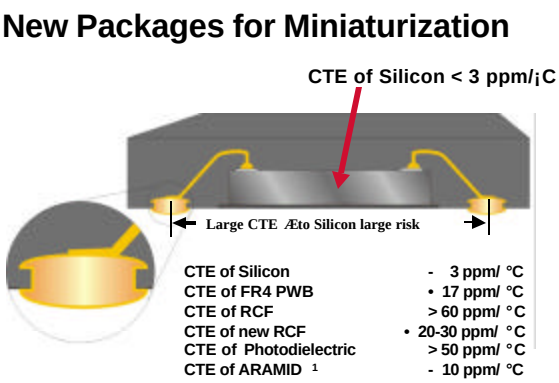


Figure 1 - The CTE of Chip Package Material

Trends with Printed Circuit Boards and Component Packages

The trend to increased functionality and a larger number of components, coupled with pressure for lower costs, have been forcing the industry to find new ways to integrate components in such a way that component housings and printed circuit boards are combined into a single unit. Internationally, the Packaging Forum in Tokyo already pointed out in 1999 the connection between printed circuit board substrates and those used in chip packages.

Roadmap of Package Material Technology:
Substrate Materials for LSI Package

Year	1998	2005	2010
Pin count	600～700	1200～1500	2000～2500
Package technology	BGA	BGA, CSP	CSP, Bare chip
Tg (TMA) (°C)	160～180	180～200	200～220
CTE (ppm/°C)	14～15	8～10	6～8
Dielectric const (1MHz)	4.4～4.6	3.0～3.5	<3.0
Dielectric loss (1MHz)	0.02～0.025	0.01～0.015	<0.005
Conductor thickness (µm)	12, 18	9	5
Insulator thickness (µm)	50～60	40～50	30～40
Peel strength (kN/m)	1.0～1.2	1.0～1.2	1.0～1.2
Via diameter (µm)	100～150	60～80	25～50
Resist resolution (µm)	16～65	6～35	5～30

Figure 2 - The Base Material Used for Chip Packages[1]

Roadmap of Package Material Technology:
Substrate Materials for Printed Wiring Board

Year	1998	2005	2010
Tg (TMA) (°C)	120～130	140～160	160～180
CTE (ppm/°C)	14～15	12～13	10～12
Dielectric const (1MHz)	4.4～4.6	3.0～4.0	<3.5
Dielectric loss (1MHz)	0.02～0.025	0.013～0.015	<0.01
Conductor thickness (µm)	12, 18	12, 18	12, 18
Insulator thickness (µm)	60～100	60～100	40～60
Peel strength (kN/m)	1.0～1.2	1.0～1.2	1.0～1.2
Via diameter (µm)	150～250	100～150	80～100
Resist resolution (µm)	50～100	30～70	25～50
Flame retardancy	V-0	V-0	V-0

Figure 3 - The base Material Used for Printed Circuit Boards[2]

If a comparison is made between the two different substrates, it becomes clear that the printed circuit board material of the future corresponds more or less to the base material used for chip packages today. For chip packages, inflammability to UL94-V0 standards is not required. On the other hand, UL94-V0 standards are an absolute requirement for new base materials used for printed circuit boards with integrated components. High Tg epoxy resins are also required for these applications, since these usually have better dimensional consistency over a larger temperature range. In the future, printed circuit boards will have even finer conductor lines and spaces, which necessitates a laminate with a more even surface. The copper foil used must have less variation in both roughness and thickness, so that the etching times and tolerances vary as little as possible.

Micro-via Technology for the Production of PWBs with Integrated Components

The ability to produce the smallest buried and/or blind holes with micro-via technology was an important milestone on the way to embedding active and passive components in the printed circuit board. It was only possible to achieve the required component density if the via holes connecting the different conductive layers did not require too much conductor routing space on the surface of the printed circuit board. During the miniaturization process, the pitch between the solder lands was reduced to less then 0.8 mm. The insulation distances between the pads are very small. For this reason, the outer surface of the PWB area is no longer available for conductor line routing. The conductor lines have to be placed on the two inner layers that are positioned under the solder lands for CSP or flip chip components. The micro-via technology used to conduct these layers has to be capable of connecting the solder lands to the next two inner layers in a cost-effective manner. Here, the parallel structure of the micro-via connections (see Cap Layer Technology in Figure 4) offers clear cost advantages compared to the conventional sequential technique.

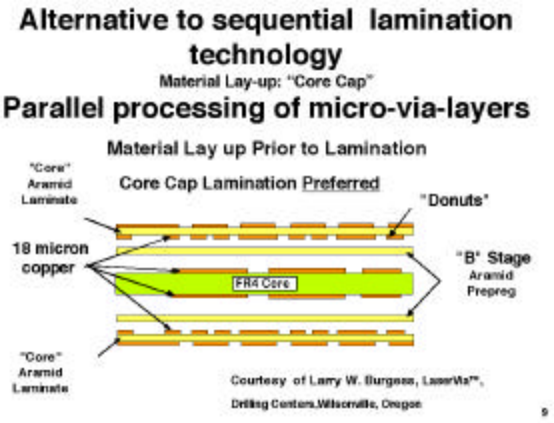


Figure 4 - Micro-via printed circuit boards manufactured in a parallel process[3]

JISSO International Council (JIC) to Harmonize Standards from the Silicon to the Assembled PCB

In the year 2000, the JISSO International Council (JIC) was created. The organizations representing the electronics industry worldwide placed themselves closely behind the development of the Japanese JISSO concept. JISSO describes the harmonization of all technologies and processes, which are necessary for the production of electronic devices in Japan, starting with the pattern on the silicon to the finished, fully-functional device. Since the Japanese JISSO team already had active working groups on the JISSO concept, the JIC first undertook the harmonization of the common technical terms and definitions. It is no easy task to harmonize the terms used by the semiconductor industry with those used by the semiconductor assemblers, the manufacturers of discrete components, the printed circuit board designer, and the manufacturers and assemblers of printed circuit boards. In the meantime, however, the first draft of the Terms and Definition document have been created by the JIC members. (more details on this subject can be obtained by the author of this paper).

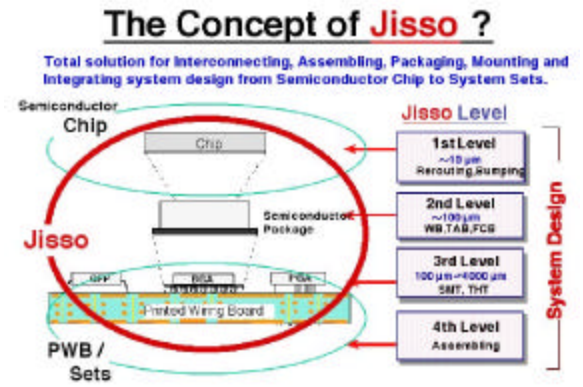


Figure 5 - The JISSO concept 2001

Figure 6 - Participants in the JIC in Okinawa

The strong dominance of the Japanese electronic industry is clearly seen by the large number of Japanese participants. Europe was represented by two participants only.

Dimensional Behavior of Printed Wiring Boards

Today, PWBs for the professional sector are predominantly manufactured using substrates reinforced with woven glass fiber fabric impregnated with epoxy resin. The issue of the wettability of glass fiber fabric was largely resolved by the use of special surface treatments, which allow for sufficient resin adhesion. Over the last 40 years, this material has become the preferred product for high quality printed circuit boards.

With minimum insulation distances from hole wall to hole wall of 1 mm, the material properties of glass fabric reinforcement were fully adequate. With High Density Interconnect (HDI) printed circuit boards, however, which have insulation distances of less then 1 mm from hole wall to hole wall, and only one glass fabric layer as an insulation layer between the conductive layers, standard FR-4 substrates were clearly pushed to their limits both as regards their dimensional behavior and their resistance to migration. Because of this, new laminate reinforcements based on organic non-woven materials were developed by the industry. The objective was to overcome the limitations of the glass as well as of the woven fabric.

During the production of PWBs, it is important to maintain accuracy and to keep dimensional changes and manufacturing tolerances to a minimum. When components are integrated into a printed circuit board, these manufacturing tolerances become still smaller. Solder land connections from the board to the silicon will have pitch spacings ranging from 75 to 300 µm. With embedded components, it is important to make sure that the dimensions of the prepregs correspond accurately to the size of the etched and through-plated inner layer. In the 'Any Layer Inner Via Hole[4] technology used by Matsushita of Japan, 100% non-woven aramid (NWA) reinforced prepreg has been used since 1997. This ensures that a high level of dimensional stability is maintained during the large-scale processing of PWBs.

If the embedded components are constructed on a polymer thick film base, i.e. on epoxy screen ink, as used with 'SIMOV'[5] technology, the dimensional changes are compensated for by the epoxy resin used in these components. The component specifications required in the future have substantially closer tolerances, which can no longer be achieved using polymer thick films. The new components are made of ceramic, silicon and/or thin-film and are embedded into the printed circuit board. The coefficients of thermal expansion (CTE) with these component materials are between 2.5 and 8 ppm/K. The PWB material will also have to adapt within the coefficients of thermal expansion in the X and Y directions to the dimensional changes occasioned by the embedded components.

If the printed circuit board is manufactured as a core with embedded components, components on the external layers will still be assembled and soldered in the conventional way. In the near future, however, it will be necessary to use lead-free solder. It has been seen that lead-free solder joints are not as flexible as joints made with lead-containing solders. Because of the higher rigidity, the entire thermal stress, created during soldering of the printed circuit board and during the operation of the device, will be transferred via the 'more solid' lead-free solder to the component connection points. Here it plays only a lesser role no matter whether this component is inside the printed circuit board or mounted on the surface. The thermal stress created leads to a high load on the component connections. If the stress is too large, the components at the junction points are destroyed.

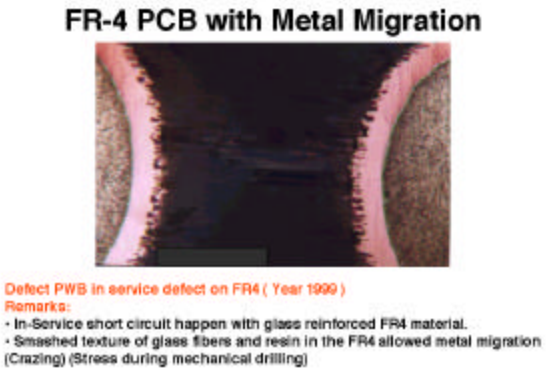


Figure 7 - Migration between the Plated-Through Holes of a Printed Circuit Board

Possible Solutions to the Problem

Especially with HDI printed circuit boards, the glass fabric-reinforced base material changes dimensions when subjected to soldering temperatures. Compared with an NWA reinforcement, the dimensional changes are clearly significant less. A study carried out with HP showed that, with a PCB measuring approximately 290 x 450 mm, the board was some 100 µm larger after soldering when built on a FR-4 glass reinforced base material than one constructed on NWA reinforced base material.

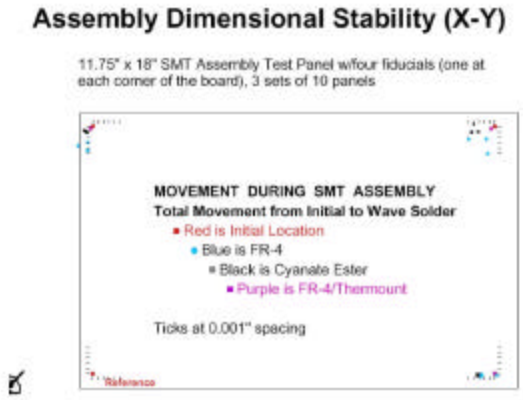


Figure 8 - An HP Study of the Comparative behavior of Glass Fiber Reinforced FR-4 Glass Fiber Reinforced Cyanate Ester Resin and 100% Non Woven Aramid Laminate and Prepreg Impregnated with High Tg Epoxy Resin Systems

Similar values have also been determined by several printed circuit board manufacturers in the United Kingdom, Finland and other countries. The investigations have shown that 100% non woven laminates with a coefficient of thermal expansion of <12 ppm/K can be manufactured routinely and processed in HDI printed circuit boards. Even lower values of 10 ppm/K have been reported for PWBs made using the ALIVH® technique (source: Lecture at EIPC Summer Conference 2001, in Copenhagen, Denmark, June 2001).

Boundaries of the Technology

The use of non-reinforced materials (e.g. pure or filled epoxy resin systems used in resin-coated copper films) may lead to cracking due to temperature changes. The coefficient of thermal expansion of these resins is 3 to 4 times higher than reinforced base materials used for the micro-via layers of HDI printed circuit boards. For the production of printed circuit boards with embedded components, it is necessary to make sure that the coefficients of thermal expansion of the base material and of the prepregs are adapted to those of the silicon or the ceramic of the components. This will help to avoid stress-related defects in the module and/or PCB assemblies.

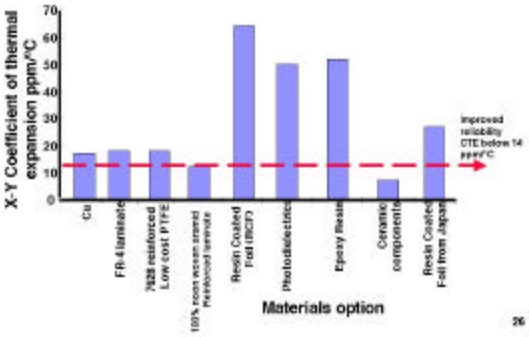


Figure 9 - Thermal Coefficients of Expansion of Materials Used in Printed Circuit Board Production

Printed circuit boards with embedded components should also have high dimensional stability during soldering. Depending on the type of assembly, 2 to 3 soldering steps may be required. The dimension of the laminate should not change significantly during multiple solder processes. Large deviations produce shearing stresses between the embedded components, the electrical connections and the printed circuit board. The forces resulting from this can destroy the electrical connections.

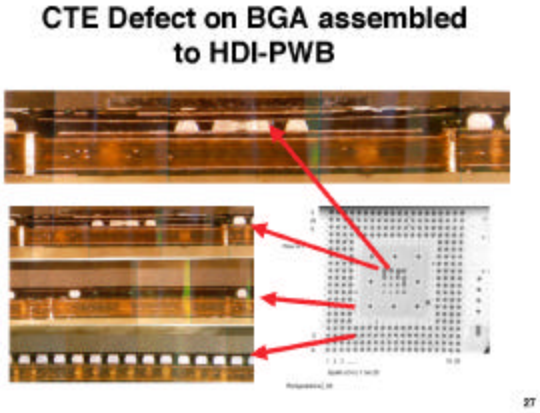


Figure 10 - Stress Damage between the Silicon and the Base Material of the Interposer with an Embedded Chip in a Chip Package

Reliability and Life Expectancy of Electronic Devices

'Resin recession', which describes the withdrawing of the resin from the plated-through hole copper metallization in resin-rich places during the soldering process, is a well-known characteristic of glass fiber-reinforced base material. If the distances between the through holes are smaller or micro-via holes are used, then these cavities can be the starting point for defects such as metal migration or conductive anodic filaments in PWBs. Phenomena such as 'resin recession' have not so far been found with laminate and prepreg that are made from NWA reinforcement material..

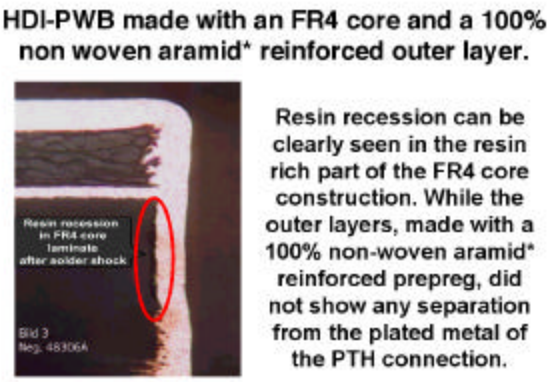
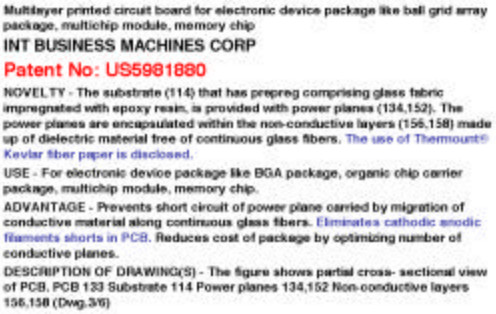


Figure 11 - Resin Recession in Resin-Rich Areas of the FR-4 Part of the PWB the NWA Part of the Upper Hole Area does not Show the Problem

'Metal migration' or 'Conductive Anodic Filaments' (CAF) in printed circuit boards are often the 'time bombs', which create defects in electronic devices. These false connections grow with conductive ions when currents are present, or at increased temperatures with small currents. The conductive connections 'propagate' along the glass fibers or along cracks in the dielectric. With standard FR-4 base material, this has been observed under certain conditions, especially if the insulation distances are small. A large OEM has been able to successfully eliminate this defect on chip packages and MCMs by using laminate and prepreg that are made with NWA reinforcement material.

Use of NWA Laminate reduces the risk for metal migration and CAF in PWBs


Multilayer printed circuit board for electronic device package like ball grid array package, multichip module, memory chip

INT BUSINESS MACHINES CORP

Patent No: US5981880

NOVELTY - The substrate (114) that has prepreg comprising glass fabric impregnated with epoxy resin, is provided with power planes (134,152). The power planes are encapsulated within the non-conductive layers (156,158) made up of dielectric material free of continuous glass fibers. The use of Thermount® Kevlar fiber paper is disclosed.

USE - For electronic device package like BGA package, organic chip carrier package, multichip module, memory chip.

ADVANTAGE - Prevents short circuit of power plane carried by migration of conductive material along continuous glass fibers. Eliminates cathodic anodic filaments shorts in PCB. Reduces cost of package by optimizing number of conductive planes.

DESCRIPTION OF DRAWING(S) - The figure shows partial cross- sectional view of PCB. PCB 133 Substrate 114 Power planes 134,152 Non-conductive layers 156,158 (Dwg.3/6)

Figure 12 - Packages Manufactured with NWA Laminate and Prepreg do not Exhibit CAF between the Conductor Layers and Large Ground- and Power-Plane Layers

High Tg Resin Systems

Processing recommendations for new high Tg prepregs specify longer pressing cycles compared to conventional FR-4 prepreg materials. This is an important point for the production of printed circuit boards containing NWA reinforced laminate and prepreg in connection with high Tg resin systems. If the press cycle is too short, the resin is not cured properly. Delamination during component soldering, rework-soldering or during the solder float test will occur. In the past, this type of delamination was attributed to a high level of humidity accumulated in the dielectric. Investigations lately showed, however, that this increased build-up of humidity was caused by under-curing of the epoxy resin. It was seen that even 'bone-dry' printed circuit boards could be subject to delamination if the epoxy resin was not fully polymerized.

It has been established that only a fully-cured resin can produce the required stability of the base material. This is also a requirement if the board is to survive the high temperatures encountered during the soldering processes. Regarding lead-free soldering, higher soldering temperatures are required. This means that the required temperature resistance of the PWB will continue to rise in the future. It is thus necessary to carry out checks during the multilayer pressing process to make sure that the circuit will perform successfully when submitted to high temperatures.

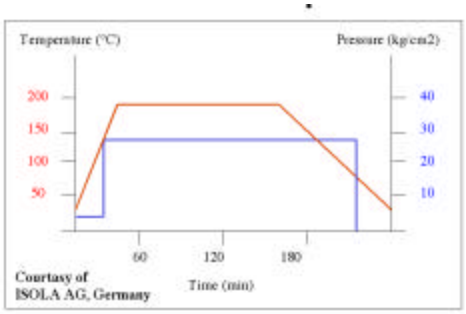


Figure 13 - Typical Press[6] Cycle with High Tg Epoxy Resin Systems Used in Connection with NWA Reinforcement

Humidity Impact on PWBs Containing NWA Laminate and Prepreg

Laminate and prepreg containing aramid are used for nearly 10 years in PCBs for avionic and space application. The reliability has been proven in many applications. In the avionic industry Polyimide resin systems have dominated the market. This resin types have higher water absorption compared to standard FR4 Epoxy resin systems. A bake or drying process before assembly and soldering is needed when Polyimide resin systems are used. This additional process is well established with high end electronic. For mass products it has been proven, that laminate and prepreg made with NWA reinforcement systems and FR4 resin, does not need such a baking process. However, the epoxy resins must be fully cured. Tests with PWBs fabricated at leading fabricators have shown no defects during solder float tests and in the assembly process of PWBs. Excellent stability in reflow and wave soldering processes are achieved in every day's production. The stress at the plated through hole plating connection or at the micro via layers made with aramid reinforced materials does not show any deformation even when tested at 288ºC for 10 sec.

Minor resin recession was observed in the FR4. No defect was found in the aramid micro via layers or at the micro via holes.

It has been documented that NWA reinforced laminate and prepreg result in a lower Dk PWB. The impact of humidity is similar compared to woven glass used as a reinforcement. However at a lower level. At high frequency application, the NWA advantages in reliable data transmission at high speed.

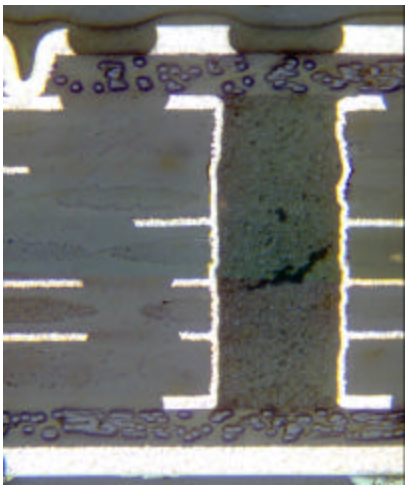


Figure 14 - Cross section of a HDI PWB Made with NWA Reinforced Prepreg after Solder Float Test at 288º C for 10 Sec.

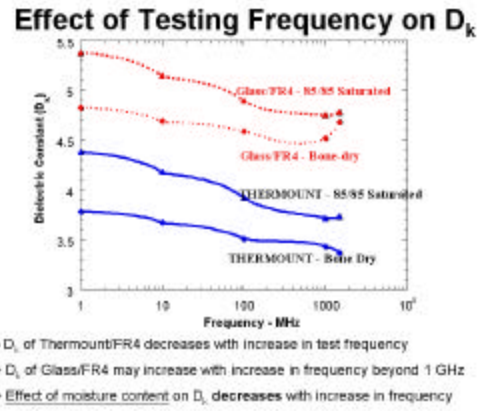


Figure 15 - Effect on Humidity on Dk of FR4 and PWBs Containing NWA Reinforced Laminate and Prepreg[7]

Sample Applications and Development

Today, many modules incorporating ceramic hybrid integrated circuits are manufactured and assembled onto the printed circuit board using conventional soldering techniques. During the next few years, the printed circuit board will be required to take over many of the functions of the ceramic component package. Constantly growing demand for cost reductions and advances in technology will ensure that the required component density, for which ceramic housings are still used today, can be converted to printed circuit technology.

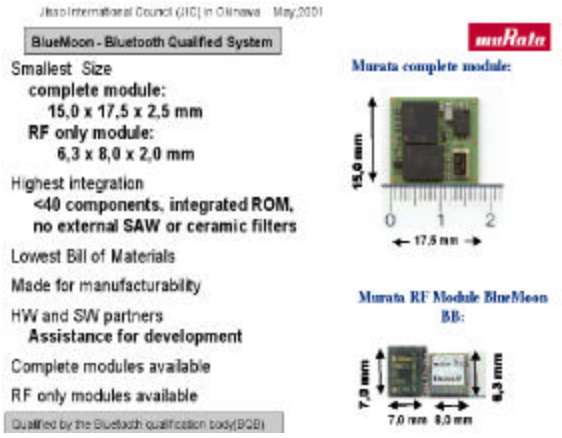


Figure 16 - Example of the Miniaturizations of a BlueMoon-Bluetooth Module

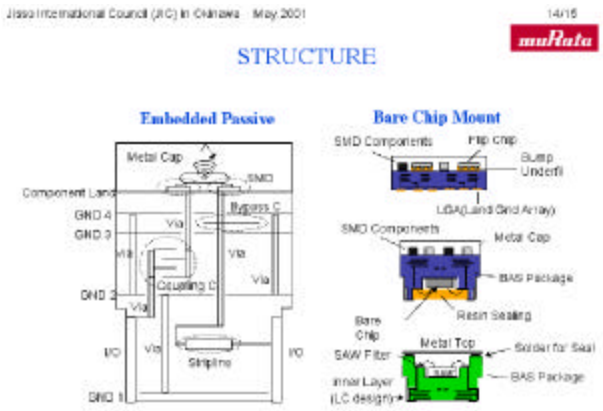


Figure 15 - The Development of Modules on a Ceramic Base During the Next Few Years, the Printed Circuit Board will Assume Many of these Functions

Fig 17 - Example of a UMTS Telephone this type of 'Phone will be Sold in Japan in the Last Quarter of 2001

Development tendencies and outlook

It is already foreseen today that the printed circuit board will be able to replace many of the functions of the ceramic circuit. Apart from more favorable production costs, however, the following technical characteristics must still be guaranteed:

- a low coefficient of thermal expansion of the base material similar to that of ceramics or silicon
- high dimensional stability during the soldering and pressing processes
- simple processing during conventional printed circuit board manufacture
- high dimensional stability of the laminate and prepreg
- simple processing in modern assembly processes
- simple design of micro-via holes on the printed circuit boards.
- Low Epsilon (Dk) for reliable high speed data transmission

The challenges facing suppliers to develop advanced new materials at favorable costs are formidable. Equally, printed circuit board manufacturers are required to introduce new technologies and to offer these at costs, which are favorable to OEMs and Electronic Manufacturing Services (EMSs). PWB designers are required to design printed circuit boards using the new technologies and to use the combination of these advanced technologies to their full potential. Excellent team spirit is required so that the different disciplines can work closely together to ensure that the new technologies are able to meet future technical requirements in a cost-effective manner.

Explanation

NWA: The 100% non-woven aramid reinforced laminate and prepreg used in this report is the material that is manufactured under the trade name THERMOUNT®. , This material is different compared with the generic aramid laminate and prepreg that is NOT based on a 100% aramid reinforcement. Generic aramid reinforcements often using as binder technology epoxy resin. This may have an issue in performance characteristics of the laminate and prepreg during PWB fabrication, in the assembly process during soldering. Dimensional changes and delamination are often the results.

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