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Controlled Surface Etching Process for Fine Line/Space Circuits

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Abstract
The design rule of PWBs and substrates for plastic packages is moving towards higher density as semiconductor chip design evolves into increasingly finer lines. First, it was studied how fine the conventional subtractive process could build line and found that line/space of that process is limited to around 40/40, even if using some new technologies. The next challenge was to find a process that can build line/space and get rid of some issues of the additive or semi additive process. It was confirmed that the improved pattern plating process used with CSE (Controlled Surface Etching) process is capable of making finer line/space circuits like around 25/25 microns. The CSE process is characterized by a uniform etching of the base copper with an improved soft etching solution.

Introduction
Semiconductor chip design is moving towards increasingly finer lines to meet the demands of more functions and high speed. This trend has placed increasing demand on high density PWBs and substrates for plastic packages to develop many new materials and processes. To achieve such requirements, some of the key points of substrate design rule are the line/space and the land diameter of PTH (Plated Through Hole) or BVH (Blind Via hole). Regarding the land diameter, there have been much effort to decrease hole diameters, and the process has changed from mechanical to laser drilling which became standard in the industry for the processing of smaller holes, such as around 80 microns.

On the other hand, many studies have been done simultaneously to develop smaller line/space. However, the demands for finer line/space are getting stronger and will be even more in the future. Therefore, the first target of this report was to find out what is the minimum line/space that can be achieved with the "subtractive method", because that has been used as the main process in copper line forming in multilayer PWBs since their introductions to the market in the1960's.

Next, another option: the "pattern plating process" was studied to achieve finer line/space. In the 1960's, many kinds of the pattern plating processes such as the "pattern plating process", the "additive process", and the "semi additive process" had been already developed in addition to the panel plating process like the "subtractive process". Recently, such pattern plating processes rather than panel plating have been favored in the industry, due to processability for finer line/space and rectangular cross-section for high frequency. Therefore, the next challenge was to find a process that can support finer line/space technology like 25/25. The "pattern plating process" was studied in order to get rid of some issues in the "semi additive process" and the "additive process", such as the material limitation or insufficient adhesion strength.

Subtractive Process
In general, the finest line/space with the "subtractive process" seems to be around 50/50 in the market. It was studied as to how much finer line/space could be stretched with the process, using SUEP and thin dry film. SUEP (surface uniform etching process) had already been introduced as a process for fine line/space forming. SUEP is a process, which reduces the surface copper foil thickness. The 3 to 5 microns copper obtained after SUEP is effective for making fine lines by the conventional subtractive process consisting of panel plating, tenting and etching. Actually, some production lines have been already installed and are manufacturing the products for fine line/space. In addition, 10 microns thickness dry film was used, which is the thinnest one available, because thinner dry film can make finer line /space due to the better etching factor.

Lines/spaces were built with SUEP, reducing to 3µm copper foil thickness and, 10µm dry film. Figure1 shows 40/40 and Figure 2 shows 25/25. They have trapezoidal cross section, which would be not favorable for electrical performance at high frequency. Figure 3 shows the ration of top/bottom width of lines on a sample. It appears that the degree of the trapezoidal cross section increases rapidly below 40/40. It means that the etching factor decreases at such finer line/space.

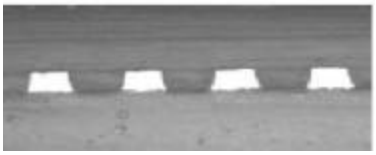

Figure 1 - Cross Section View of Line/Space 40/40 with Subtractive Process

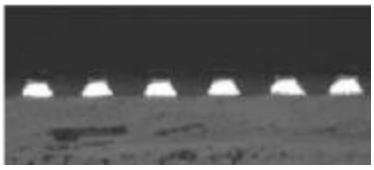

Figure 2 - Cross Section View of Line/Space 25/25 with Subtractive Process

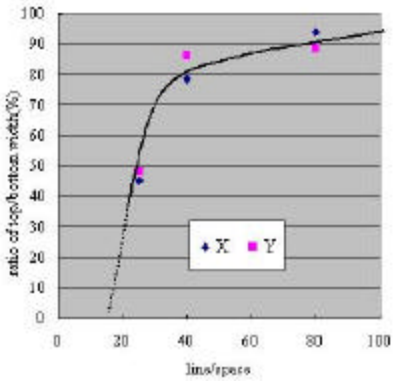

Figure 3 - The Ratio of Top/Bottom Width with Subtractive Process (Base Copper Foil: 3μm, Plated Copper: 12μm)

From the results above, it was concluded that 40/40 was about the lower limit for fine line/space made with subtractive process. In addition, the pattern density difference on a substrate is another issue, since its necessary to compensate pattern mask in order to get designed line/spaces. In this point of view, it is hard to make finer line/space with the subtractive process.

Pattern Plating Process

As mentioned above, the pattern plating processes can build finer line/space than the panel plating process like the subtractive, because it's easy to get the exact line dimension by building lines between plating resists like dry film. Many kinds of pattern plating process like the "additive", the "Semi additive", the "pattern plating" were developed in the 1960's. Particularly, the "semi additive" has been recently improved for finer line/space at HDI substrates. However, the "pattern plating" process was selected to build less than 40/40 lines/spaces for the following reasons:

1. The materials, processes and machines used in the pattern plating are similar to those used with the subtractive process.
2. The electrical and physical properties of Plastic packages made with the pattern plating process are similar to conventional subtractive process Plastic packages, except for finer line and space circuits.
3. There is no limitation on insulation materials selection for build up layers.

Particularly, (3) is the big advantage for substrates for the next generation IC, because the electrical performance of dielectric materials used for the conventional build up substrates degrades at higher temperature like over 100 centigrade 1. In addition, it's getting harder to keep enough insulation resistance, as such materials should be getting thinner to provide a proper characteristic impedance. However, the "plating process" can allow us to use materials with stable electrical and /or physical properties. Due to the reasons above, the "pattern plating" process was studied, and improved the conventional "pattern plating" with the CSE process explained below.

Process

The conventional "pattern plating" process, also called the "Plated Solder Stripping" process, have a thick base copper like 20μm and uses plated solder as etching resist for the traces. Such thick base copper makes traces smaller by etching after removal of the plating resist. Plated solder on traces also requires an alkali etchant that has an inferior etching factor for base copper. In addition, that also causes overhang on traces, which disturbs plating resist stripping. Therefore, conventional "pattern plating" process should be improved to make finer line/space. First, SUEP was adopted to thin the base copper down to a few microns. Secondly, an improved etching process CSE (Controlled Surface Etching) was developed. It is explained in detail later, in order to uniformly etch the base copper and discard the plated solder.

Figure 4 shows a process flow of the improved "pattern plating" process with the CSE process. The first step is uniformly reducing the surface copper foil from 12 to 3μm with SUEP after drilling. Then, the laminate was plated on a conventional vertical line including desmear, soft etching, electroless plating, and electro plating. After this process, the base copper thickness was 5μm, because it was reduced down to 2μm with soft etching, then increased up to 3μm with electroless Copper, and increased again up to 5μm. Next, 25 micron film type plating resist is applied on the plated copper 110 centigrade, 1.5m/min) after a surface treatment of sulfuric acid/hydrogen peroxide solution, which is used conventionally as pretreatment of etching resist lamination. Then, positive pattern was imaged to the plating resist by UV exposure (60mJ/cm2), and this was developed with a conventional developing line. The traces are plated up to 20 to 25 microns height at the next step. For the striping solution, conventional sodium hydroxide is available, and a kind of organic amine solution would be better for productivity as mentioned below. After removing the resist, about 5 microns of the copper layer was uniformly etched out by the CSE process (35 centigrade, 2min). With this improved process, 25/25 was obtained

approximately, with a rectangular cross section as shown in Figure. 5

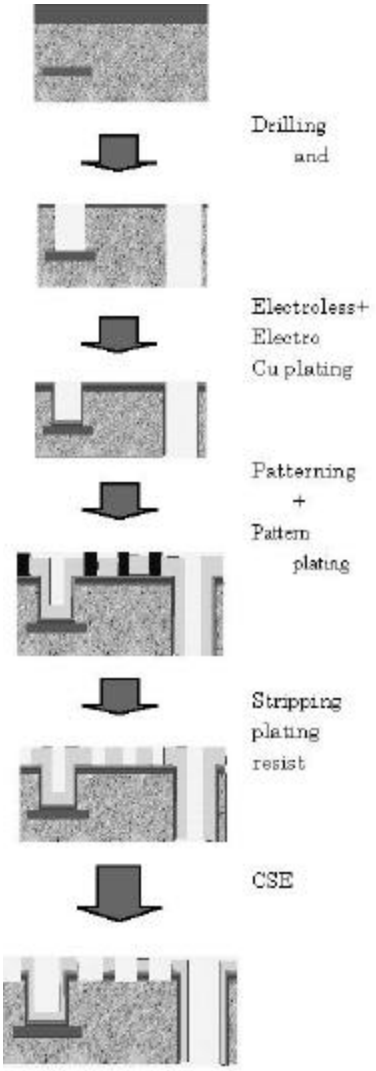

Figure 4 - Process Flow of Improved "Pattern Plating" Process

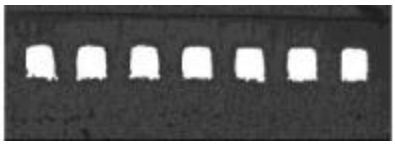

Figure 5 - Cross-Section View of After CSE Process (Line/Space=25/25)

Base Materials for the CSE Process

When using this process, it is very important to select a suitable copper foil in order to avoid remaining copper between the lines, which causes insufficient insulation resistance. The copper foil should have a fine and lower profile, which is easily removed uniformly and keeps enough adhesion strength. Some foils have alloy profiles to increase the adhesion strength, which has a lower dissolubility than copper and could result in remaining copper.

SUEP

To achieve finer line/space, a uniform base copper thickness is necessary, as remaining copper could occur if the copper is thick. In other words, the thinner and more uniform thickness copper foil is more advantageous for forming fine line/space. Therefore, SUEP is also effective at this process. In addition, the equipment of SUEP was adjusted to improve thickness accuracy, and the resulting thickness range is ±0.8 microns with a standard panel size. The thinner base copper is better, but considering the margin of other processes like pre-treatment of the copper plating, 3-micron thickness after SUEP was selected. SUEP should be applied after direct laser drilling and before mechanical drilling. This is because SUEP must remove burrs around the vias after direct laser drilling and prevent etching copper just around the PTH.

Resist Stripping

In the subtractive process, the etching resist film was on the pattern. However, the plating resist in this process is buried between the plated traces. Therefore, it is harder to strip the resist using a conventional solution, 3%- sodium hydroxide (NaOH) at 50 centigrade, than with the subtractive process. Actually, it takes 2 to 3 times longer than that process to complete the strip resist. For example, it takes around 3 minutes for 25µm plating resist dry film. On the other hand, organic amine solution would be better for productivity, since it's stripped out within around 10 to 20 seconds.

CSE (Controlled Surface Etching)

After removing the plating resist, about 5 microns base copper between traces should be uniformly etched out on a whole panel. Soft etching solution was chosen, not conventional etching solution to remove the base copper, since that etching solution has too fast etching speed. As a soft etching solution, a kind of a hydrogen peroxide sulfuric acid was selected, because this kind of soft etching solution performs well for uniform etching. However, using the conventional soft etching solution, lines had under cut at electroless copper layer as shown in Figure 6. To prevent such undercut, the conditions of the components and additives were studied, and found a suitable additive, which does not cause undercut. For example, Figure 7 shows the relation of undercut and kinds of additives. By modifying such factors, undercut was rapidly decreased, and lines were obtained without undercut with the suitable additive as shown in Figure 8.

Figure 6 - Under Cut with Conventional Soft Etching Solution

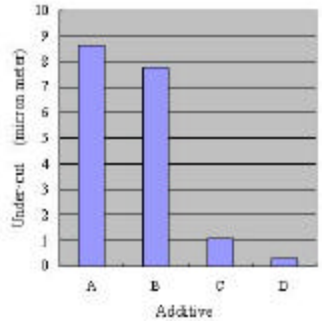

Figure 7 - The Relation of Under Cut and Additives

Figure 8 - Under Cut with Improved Soft Etching Solution

In addition, it was confirmed that plated copper in PTH and BVH has enough thickness after CSE as shown in Figure 9 and 10. Before CSE, plated copper thickness in PTH and BVH was around 19µm, which is almost the same as surface copper thickness, 20µm. Though the plated copper was etched down to around 14µm with CSE, it appears that the thickness is enough to keep the conductivity. With CSE, lines are also etched out by the same thickness as the base copper. When the base copper is 5µm thickness, line width reduces by 10µm. Therefore, tooling compensation should be necessary to get the exact designed dimension. Actually, traces are bigger by a few microns at a plating process, which seems to be negligible.

Figure 9 - Cross Section View of BVH after CSE Process

Figure 10 - Cross Section View of PTH after CSE Process

Conclusion

The CSE process is an improved and simplified pattern plating process and is useful for making fine line/space circuits of around 25/25 microns.

The main points of the process are as follows:

1. The materials, processes and machines used in pattern plating are similar to those used in the subtractive process.
2. The electrical and physical properties of plastic packages made with the pattern plating process are similar to conventional subtractive process plastic packages, except for finer line and space circuits.
3. There is no limitation on insulation materials selection for build up layers.

This fine line/space forming process offers a promising solution to the problems of making higher density circuit boards. With further studies on base copper thickness, plating conditions and plating resist, it should be possible to make line/space even finer than 25/25.

Reference

1. Kaoru Kobayashi, Kimihiro Yamanaka, Hiroyuki Mori, and Yutaka Tsukada, "Requirements of Build-Up Material for the Next Generation High Performance Chip Carrier", 11th Micro Electronics Symposium in 2001, pp 355-358.