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Design Considerations Affecting the Measured Capacitance of Embedded Singulated Capacitors

David R. McGregor
E.I. du Pont de Nemours and Co.
Research Triangle Park, NC

Abstract
The physical placement of embedded singulated capacitors in relation to one another and to other board structures could have an impact on the measured capacitance of individual capacitors. For board designs requiring tight tolerance of an embedded singulated capacitor, knowledge of the influence of board design on the measured capacitance would be of interest. A designed experiment tested the effect of 3 factors: distance between capacitors (capacitator spacing), the presence of an additional ground plane in the board, and having a common ground for the adjacent capacitors. Test design, board construction, and resulting capacitance measurement data will be presented. The results showed that all 3 main factors and 1 interaction term were significant. The significant interaction was between capacitor spacing and common ground.

Introduction

A singulated capacitor embedded in the printed wiring board substrate will in general have a capacitance that can be calculated; however, the actual measured capacitance may differ depending on other features within the board and their proximity to the embedded capacitor. Depending on the tolerance desired, the difference between calculated and measured capacitance may be of interest to the circuit designer, especially in the case of filter networks.

Most CAD software systems used for circuit design and printed wiring board layout have not been up-dated to include routines for handling embedded singulated capacitors. The issues include making sure a via hole is not placed in the same location as the capacitor as well as taking into account effects that other features in the substrate may have on the actual capacitance.

Clearly this paper does not provide sufficient information to be able to predict the measured capacitance in all cases nor does it provide sufficient information for CAD developers to write capacitance prediction software routines. Yet, it does show that the proximity of other features within the board will have an effect on the measured capacitance and it points the way toward further research needed to gain a better understanding of the behavior of embedded capacitors.

Potential Factors Having an Influence on Measured Capacitance

Upon reflection, there seemed to be three obvious factors that could have some effect on the measured capacitance of an embedded singulated capacitor. Figure 1 illustrates these.

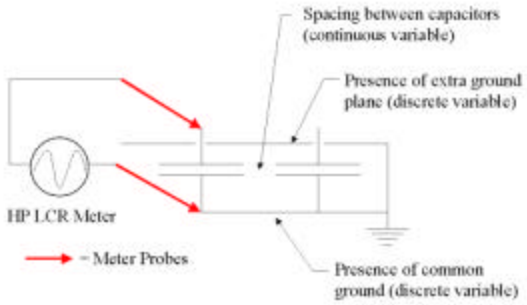

Figure 1 - Illustration of Tested Factors

The first factor considered was the physical spacing between adjacent singulated capacitors. By the nature of the fabrication processes, embedded capacitors are usually made on the same layer pair as opposed to one or two capacitors made on every layer pair. In addition, embedded real estate will be somewhat at a premium since space will be needed for via holes. Therefore, wise use of real estate would suggest that designers may want to place embedded capacitors close to one another. In Figure 1 assume that the 2 capacitors exist in close proximity without a common ground or an additional ground plane in the board. When a varying signal is placed on the capacitor on the left, the plates of the adjacent capacitor could have charges induced on its plates effectively increasing the overall plate area and the measured capacitance of the capacitor on the left.

It is not necessary that two capacitors have a common ground but it is likely that many will. The second factor that seemed reasonable was that of 2 or more capacitors having a common ground. This condition would also tend to have the effect of increasing the total plate area and increasing the measured capacitance.

Many multilayer printed wiring boards have more than 1 ground plane. If a ground plane is placed in the printed wiring board in a manner shown in Figure 1 and the spacing is relatively close, it will in effect create two capacitors in parallel, causing an increase in the measured capacitance.

These 3 factors, capacitor proximity, presence of a ground plane in the board and presence of a common ground were selected for testing the hypothesis that 1 or more would have a statistically significant effect on the measured capacitance of an embedded singulated capacitor.

Test Design

A simple 2 level, 3 factor factorial design could have been used as a screening test but, since the spacing between adjacent capacitors is a continuous variable, a more sophisticated design could be used to determine whether there may be curvature within the design space. In addition, thought was given to the ever-present trade-off when deciding on how many test runs to conduct.

A D-Optimal design was chosen and the test was designed and analyzed with Design-Expert® by Stat-Ease, Inc.[1] The basic test design is shown in Figure 2.

Five replicates were run making a total of 80 runs. The use of 5 replicates made detection of a significant effect within one standard deviation very likely.

Standard Order	Run Order	Space Width (mils)	Ground Plane Above	Common Ground
1	10	10.00	no	no
2	3	100.00	yes	yes
3	2	78.00	no	yes
4	14	100.00	yes	no
5	13	100.00	no	no
6	15	32.00	yes	yes
7	9	10.00	yes	no
8	4	10.00	no	yes
9	16	55.00	no	no
10	6	55.00	yes	no
11	11	10.00	yes	yes
12	5	100.00	no	yes
13	7	10.00	no	yes
14	8	100.00	yes	yes
15	1	100.00	no	no
16	12	10.00	yes	no

Figure 2 - Basic Test Plan

Test Panel Construction

The embedded singulated capacitor design is shown in Figure 3.

A grid of 36 individual capacitors was created for each test condition and is shown in Figure 4. The spacing between singulated capacitors varied from 10 mils to 100 mils.

The 16 interior capacitors, B2 through E5 were measured and the average used as the response for each test condition.

The 16 different test conditions shown in Figure 2 were laid out randomly on an 18-inch by 24-inch panel. In addition, 6 individual capacitors were spaced around the periphery of the board away from other features. The intent was to use these isolated capacitors in a Gauge R&R study to verify that the measurement system was capable of being used. The test panel layout is shown in Figure 5.

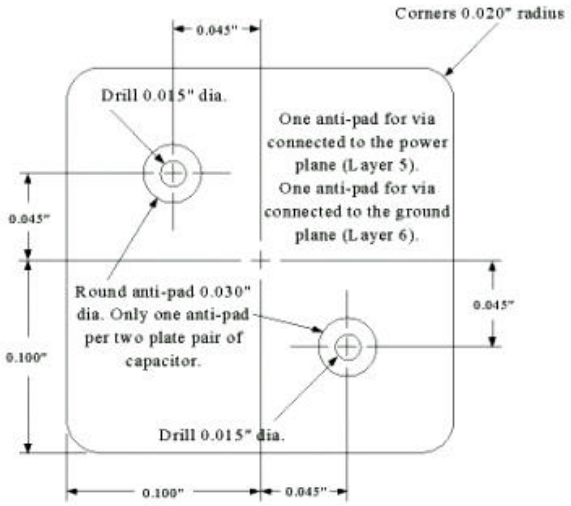

Figure 3 - Embedded Singulated Capacitor Dimensions

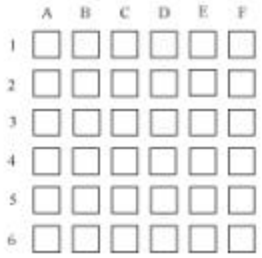

Figure 4 - Grid Layout of Individual Capacitors

Each of the 16 blocks in the interior of the panel represents a 36-capacitator grid and the number in the block is the centerline distance between capacitors in mils, defining the spacing between individual capacitors.

The layer stack-up is shown in Figure 6.

Layer 1 was used to image the grid nomenclature and the test pads for each capacitor. Layer 3 was used to image the additional ground plane test conditions. The combination of an 8-mil core laminate and 2 layers of epoxy prepreg resulted in a measured 14-mil spacing between the "extra ground plane" and the capacitors. The goal was to shoot for something

reasonable. In hindsight, the spacing could have been varied without significant difficulty, making the test even more informative. Individual capacitors were imaged on layers 5 and 6. A thin, ceramic filled polyimide laminate having a capacitance density of 2.0 nF/in^2 was used to create the embedded singulated capacitors. Layer 8 was used to image common ground connections where called for in the test plan.

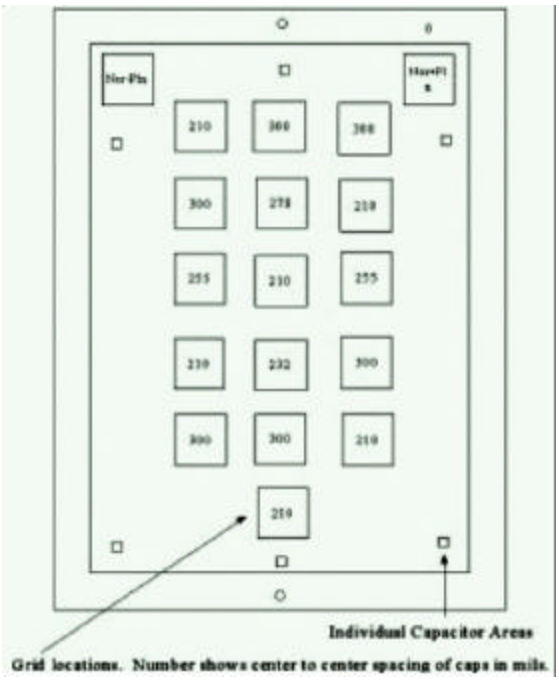

Figure 5 - Test Panel Layout

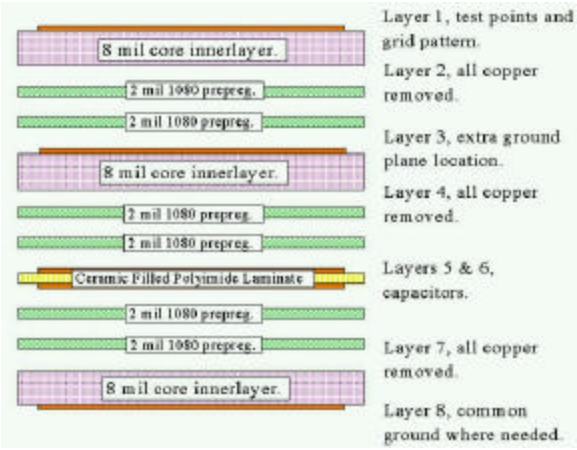

Figure 6 - Test Panel Stack-up

Gauge R&R Results

A recently calibrated Hewlett-Packard 4284A Precision LCR Meter was used to measure individual capacitors. The 4284A is capable of measuring capacitance from 20 Hz to 1 MHz. For this test we measured the capacitance at 1 MHz with the meter set to 1 volt AC. A Hewlett-Packard 16334A probe was used in conjunction with the LCR Meter. Calibration of the probe and meter was done before each measurement session.

The measurement system was validated using a Gauge R&R analysis. Two different operators measured the 6 individual capacitors on 3 different panels 5 times in random order (ninety measurements for each operator). The Gauge R&R analysis results are shown in Figure 7. Even though the LCR meter reported capacitance in fractions of a pico Farad, all measurements were rounded to the nearest pico Farad.

The results show that the variation observed was in the individual capacitors and not in the measurement system. In fact of the 180 measurements only 2 varied by a pico Farad. This is understandable since all measurements were rounded and the difference of a few tenths of a pico Farad could change the recorded value.

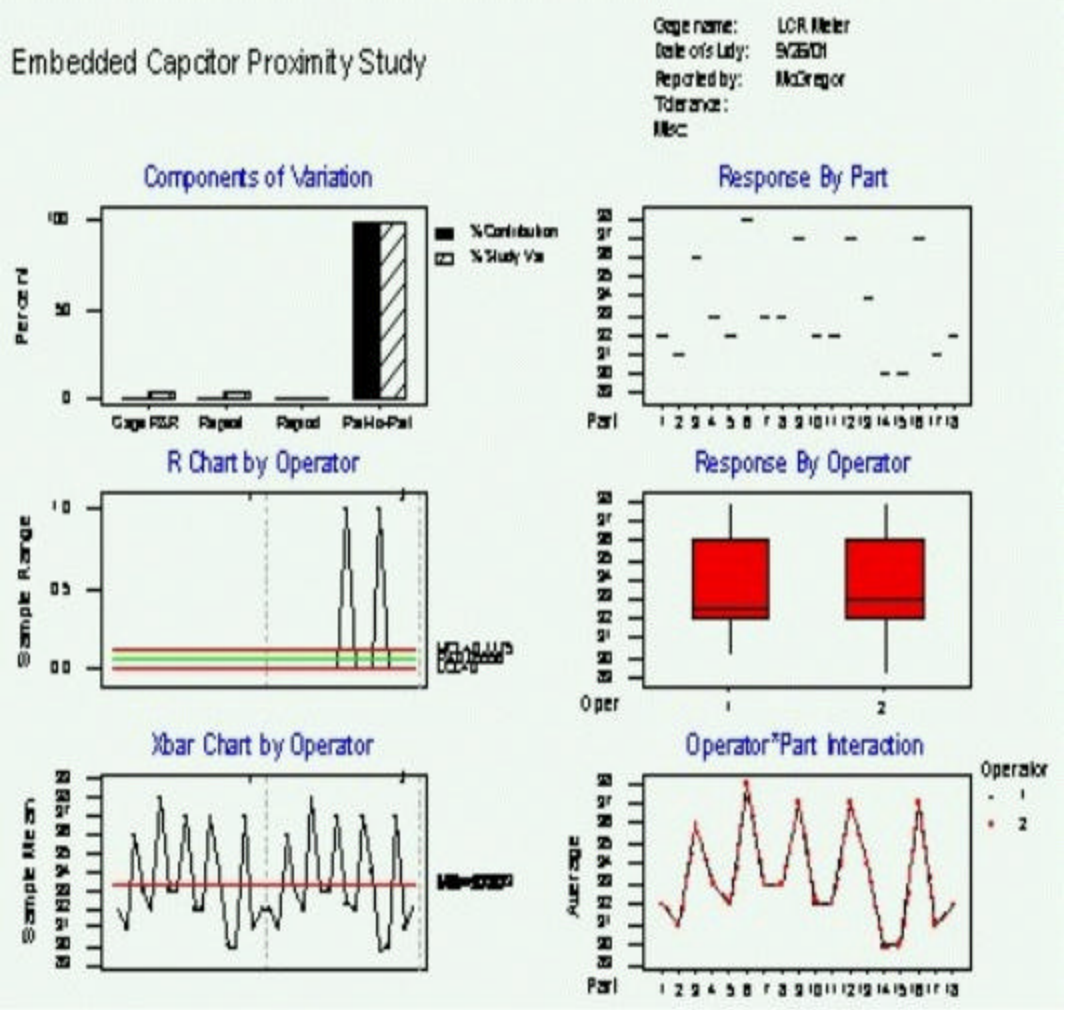

Figure 7 – Results of Gauge R&R Study

Test Results

Sixteen singulated capacitors were measured and the average used as the data point for each test condition. Test conditions from 5 panels resulted in 80 data points. The analysis software suggested a linear model with interactions be used for the ANOVA analysis. The half-normal probability plot of residuals shown in Figure 8 indicates a normal distribution of the data, meaning that proceeding with the analysis was acceptable.

The ANOVA table shows that all 3 main factors and 1 interaction term are significant (Table 1). The significant interaction was capacitor spacing and presence of a common ground.

When a capacitor does not share a common ground with another adjacent capacitor and there is no ground plane above them, the spacing between capacitors does not have any significant effect, but when they do share a common ground the spacing does have a significant effect. This can be seen in Figures 9 and 10.

Comparing Figures 9 and 10, the capacitance of the closely spaced capacitors increases when the capacitors are connected with a common ground. Capacitive coupling from one plate of the capacitor being tested to the common ground plates of adjacent capacitors would be additive since they would be capacitors in parallel. This could easily explain the observed increase. However, again comparing Figures 9 and 10, notice that the capacitance drops as the spacing increases. This observation is difficult to explain unless at the test frequency of 1 MHz there is a periodicity in the capacitance that could reinforce positively at some distances, and destructively at other distances. Additional testing at lower frequencies is needed to confirm this hypothesis.

Figure 11 shows a cross-section of one of the embedded singulated capacitors and the presence of a ground plane in the board. The cross-section was made at the point where one of the through holes passes through the antipad in the top capacitor plate. The bottom capacitor plate was intended for connection to ground and that is why it is connected to the ground plane.

The interaction between capacitor spacing and common ground when an additional ground plane is present is shown in Figures 12 and 13. Figure 12 shows the results when an additional ground plane is NOT present. Figure 13 shows the results when an additional ground plane IS present. The measured capacitance is higher when the additional ground plane is present. The average increase is not as high as expected. It is only about 61% of the calculated value. Therefore, while the addition of the ground plane has a real effect, it is on average not the same as the calculated value, at least not in this experiment.

This observation suggests that predictions of embedded capacitance values should be based on collecting additional data to model behavior rather than relying solely on the conventional capacitance calculation.

The effect of spacing between capacitors is linear. The minimum and maximum spacings were 10 mils and 100 mils respectively. Results from the intermediate spacings of 32 mils 55 mils and 78 mils show this linear behavior.

Finally, the error that was unaccounted for in the test was quite small. The mean square of the pure error from Table 1 was 3.5. This is the variance, so the standard deviation of the error unaccounted for is the square root, or 1.9. This agrees well with the average standard deviation from the individual capacitors spaced around the periphery of the boards. The average standard deviation of these individual capacitors was 2.2.

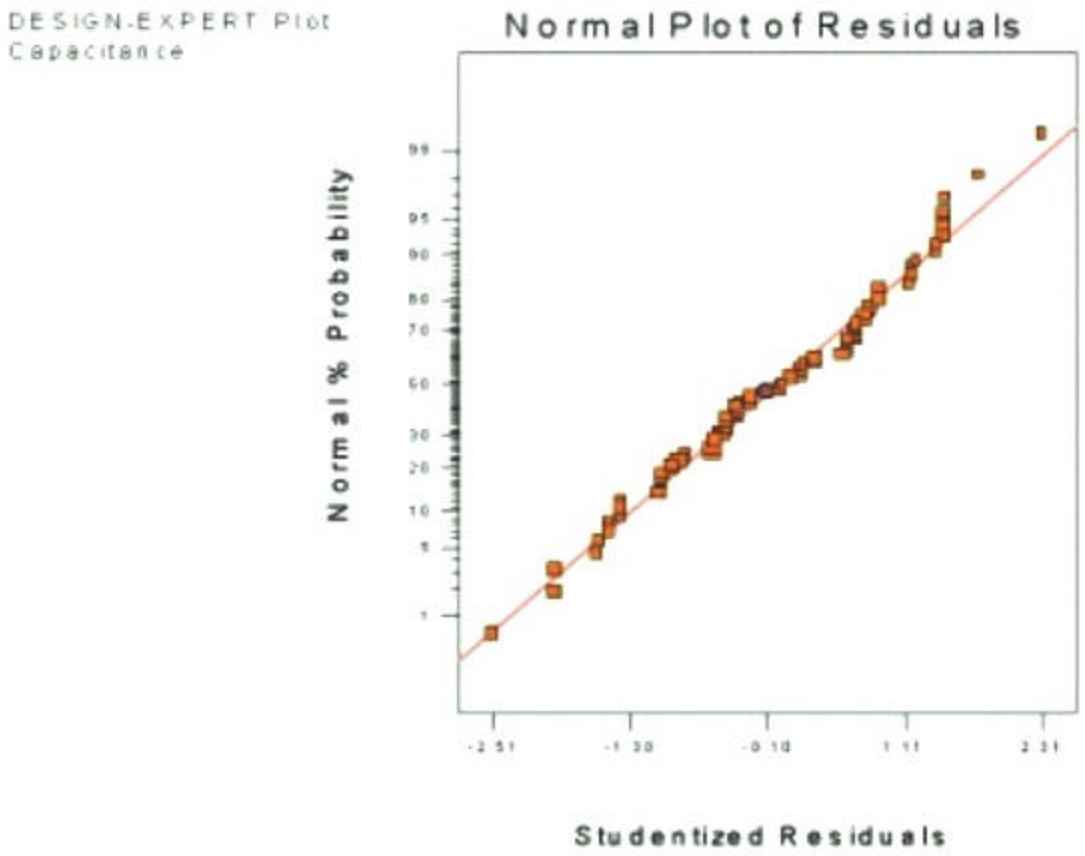

Figure 8 - Normal Plot of Residuals

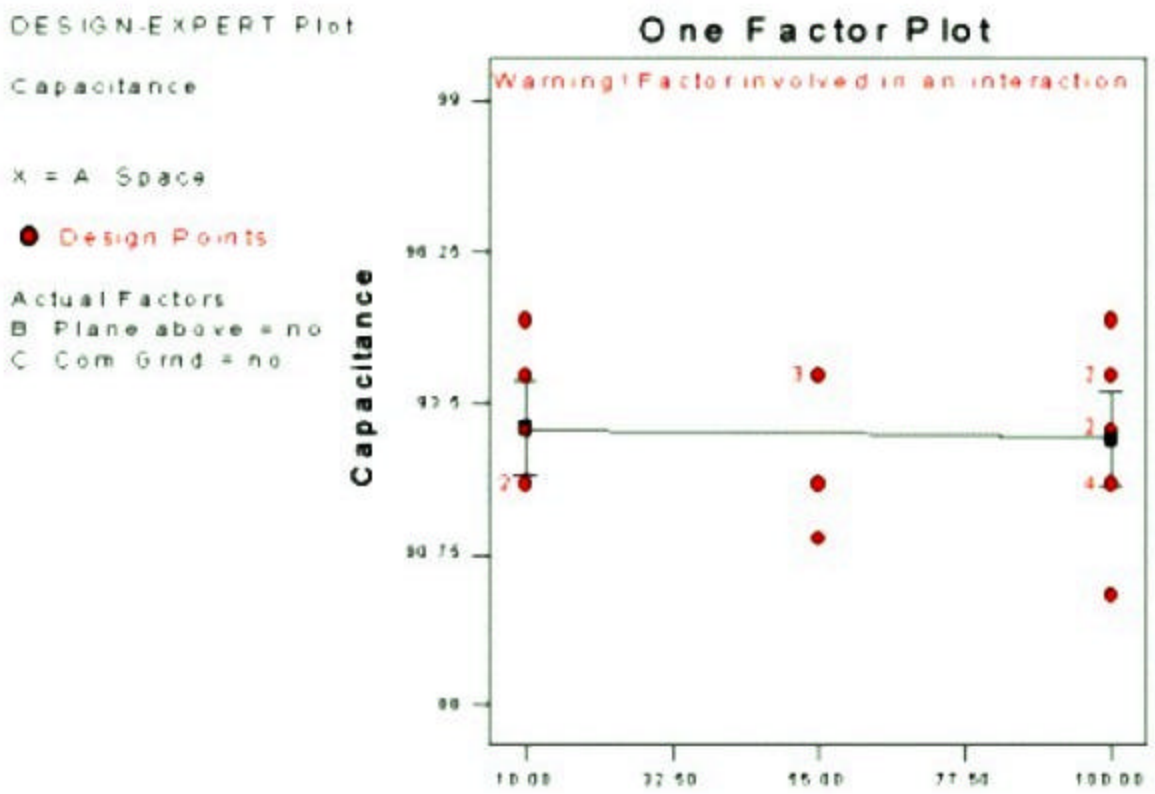

Figure 9 - Effect of Capacitor Spacing with <u>No</u> Common Ground

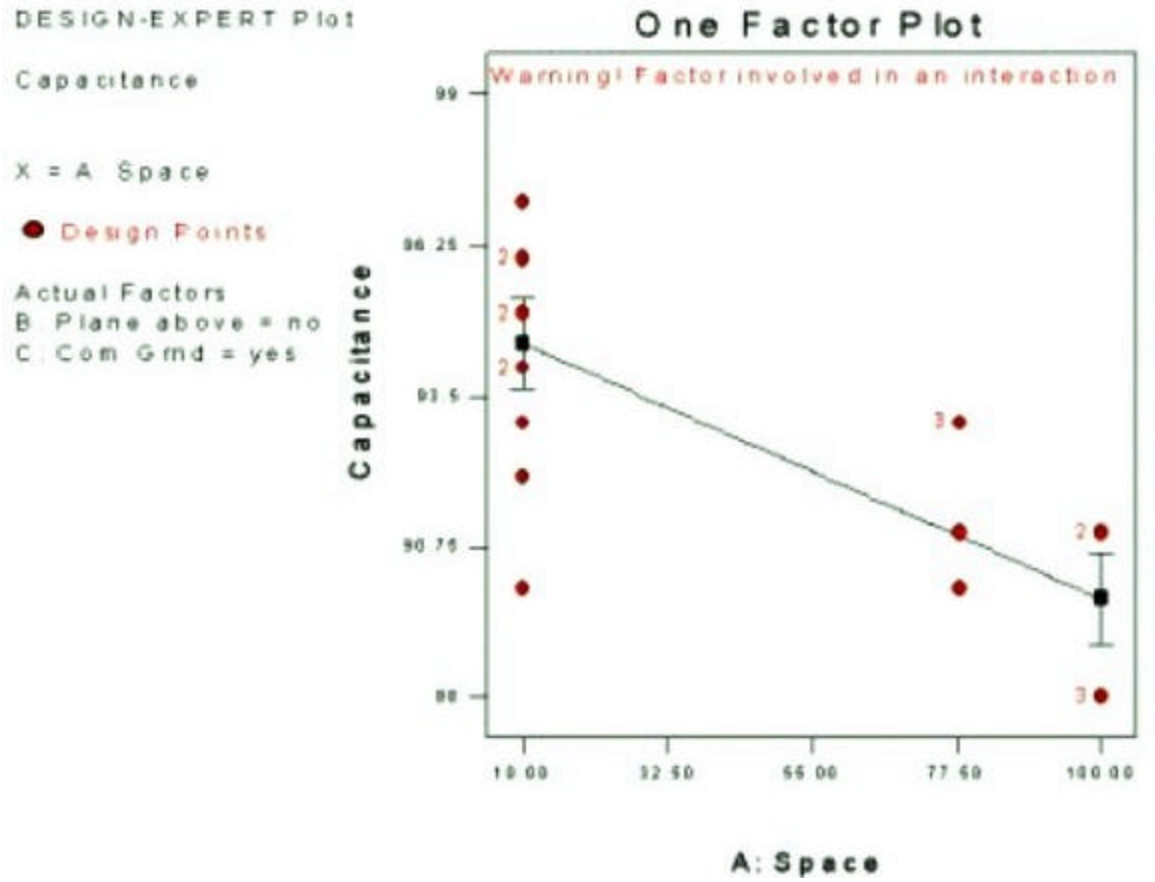

Figure 10 - Effect of Capacitor Spacing <u>with</u> a Common Ground

Table 1 - ANOVA Result Table

Response:	Capacitance					
ANOVA for Response Surface 2FI Model						
Analysis of variance table [Partial sum of squares]						
Source	Sum of Squares	DF	Mean Square	F Value	Prob > F	
Model	216.0	6	36.0	10.52	< 0.0001	significant
A	69.4	1	69.4	20.27	< 0.0001	
B	51.7	1	51.7	15.11	0.0002	
C	21.3	1	21.3	6.21	0.0150	
AB	0.9	1	0.9	0.25	0.6170	
AC	71.7	1	71.7	20.95	< 0.0001	
BC	1.2	1	1.2	0.34	0.5602	
Residual	246.3	72	3.4			
Lack of Fit	12.6	5	2.5	0.73	0.6070	not significant
Pure Error	233.7	67	3.5			
Cor Total	462.4	78				
• The Model F-value of 10.52 implies the model is significant. There is only a 0.01% chance that a "Model F-Value" this large could occur due to noise.						
• Values of "Prob > F" less than 0.0500 indicate model terms are significant.						
• In this case A, B, C, AC are significant model terms.						
• Values greater than 0.1000 indicate the model terms are not significant.						
• If there are many insignificant model terms (not counting those required to support hierarchy), model reduction may improve your model.						
• The "Lack of Fit F-value" of 0.73 implies the Lack of Fit is not significant relative to the pure error. There is a 60.70% chance that a "Lack of Fit F-value" this large could occur due to noise. Non-significant lack of fit is good -- we want the model to fit.						

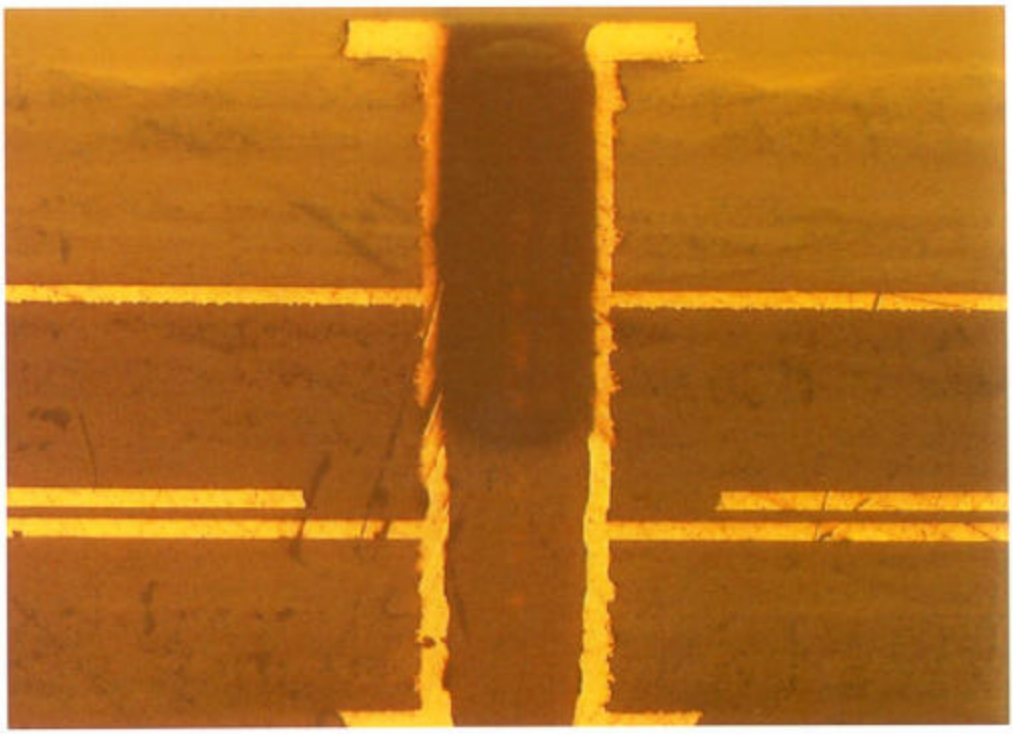

Figure 11 - Cross-section View of Embedded Singulated Capacitor and Ground Plane in Board

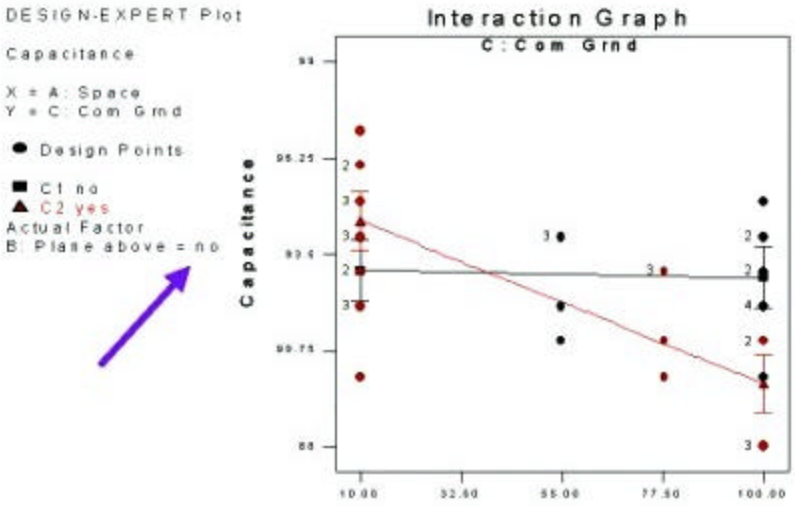

Figure 12 - Interaction Between Spacing and Common Ground Without an Additional Ground Plane

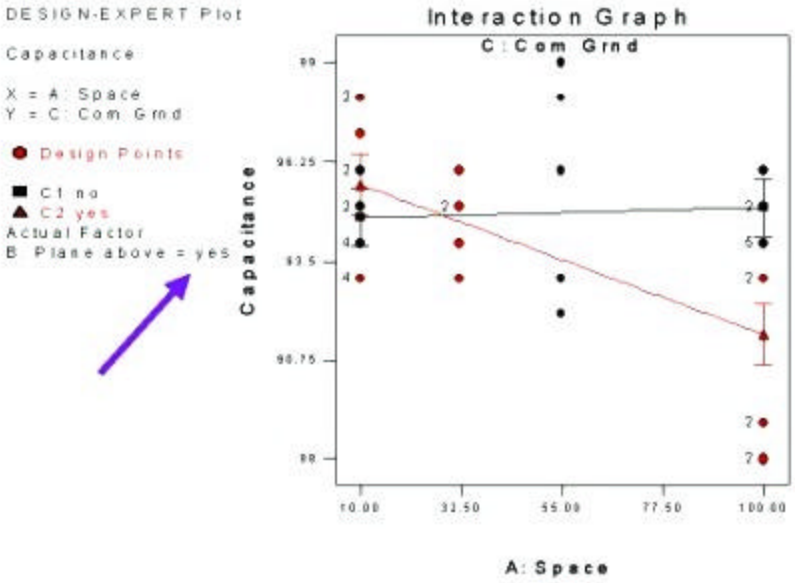

Figure 13 - Interaction Between Spacing and Common Ground With the Presence of an Additional Ground Plane

Summary

The original hypothesis that board design features would have an effect on the measured capacitance of singulated embedded capacitors has been shown to be correct based on the test results. Three factors were chosen based primarily on thinking about how conventional boards are constructed and how capacitors are used in circuit designs. Space between singulated capacitors, whether or not another ground plane exists in proximity to the capacitors and whether or not the capacitors have a common ground were the factors of interest in the experiment. A D-Optimal response surface test design was used for the test.

A test vehicle was designed and boards fabricated for the test. Five replicates in the form of 5 boards were tested for a total of 80 test runs. The results showed that all three main factors were significant and that there was one significant interaction term.

When only individual capacitors were measured, meaning each had no other electrical connection to any other, the spacing between the capacitors did not influence the capacitance. When an individual capacitor was connected to adjacent capacitors by means of a common ground, the spacing had a strong effect, leading to the significant interaction between spacing and presence of a common ground. Interestingly, the common ground affected the widely spaced capacitors in a way the author did not expect. The capacitance of widely spaced capacitors having a common ground dropped below that of those that did not have a common ground. It is possible that this

was caused by using 1 MHz as the frequency for measurement. A different frequency might or might not show this effect.

The presence of a ground plane in the board also had a significant effect, although it was somewhat less than what the author would have predicted based on calculation.

The residual error in the test was quite low meaning that the observed variation was almost completely explained by the model. The variance in the test was close to the variance observed on six individual capacitors embedded around the periphery of each test board.

It is obvious from the results, considering the small physical size and low capacitance of the capacitors used in this test, that some circuits could tolerate the observed differences. Proper functioning of circuit designs requiring tight tolerance of capacitance, on the other hand, might be adversely affected. The magnitude of these effects on embedded capacitors having significantly higher capacitance would be informative. In any case, the results point to the fact that gaining an understanding of the behavior of embedded capacitors would be useful to circuit designers, board fabricators and CAD software developers.

Capacitance for this test was measured at a frequency of 1 MHz. Most circuit designs that will benefit from embedding capacitors will be operating at frequencies in the GHz range. The behavior of embedded capacitors and the effects of other board features need to be evaluated at these frequencies. In addition, there may be other factors existing in some circuit designs that should be investigated in future research.

Acknowledgements
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References:

1. Stat-Ease, Inc.
   2021 East Hennepin Avenue, Suite 191
   Minneapolis, MN 55413-2723