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Direct Laser Drillable Ultra Thin Copper Foils for Advanced PCB Manufacture

Mike Hacker
Circuit Foil Luxembourg
Thursby, Cumbria, UK

Introduction

The demand for small packaging for portable electronic equipment and reduced chip form factor with higher interconnect fan-out, is driving printed circuit substrate technology rapidly forward. The demand is for smaller, thinner, lighter, more reliable and, of course, cheaper devices. Just consider the paradigm provided by the cellular phone, the laptop or the PDA in less than a decade.

At the interconnect level this means ultra thin high layer count PCBs, densely populated on both sides, maximizing surface mount 'real-estate' and that requires high density interconnectivity.

Reducing PCB line and space widths is certainly a proven method for increasing circuit density, but further reductions will demand significant process control improvements to prevent yield losses from driving production costs up.

Enhanced interconnectivity is a second important driver. Today's 'state-of-the-art' boards call for a rapid growth in this. This demand, for escalated pad density, is being met by a variety of techniques with every increasing hard to remember acronyms, most of which require high density interconnect structures.

A better target for major leaps in connectivity improvement comes from a reduction in the size of via holes and their associated lands, which per se immediately creates more routing tracks between pads. The HDI PCB in 1997 averaged ~ 485 I/O's per square inch, in 2001 it was closer to 1,800. As device form factors shrink and I/O density mushrooms, the size of vias must fall and their number increase. Expressed in another way, the typical '97 PCB via count of 20,000 has increased by more than a magnitude to closer to 250,000.

Currently there are several entry routes for the manufacture of PCBs with laser drilled micro via interconnect features:
1 "Half-Etch" route
2 "Conformal Mask" route
3 Thin Foils + Oxide Conversion route

We will describe the key features and disadvantages of each of the current production techniques.

Here the first step involves the lamination of a conventional unsupported copper foil, typically 18µm or 12µm thick, to the etched outer layer of a multi-layer PCB. "Laser drillable" prepreg, aramid reinforcement and increasingly regular "FR4/glass epoxies" are typical dielectric substrates. Alternatively resin coated copper foils with a thick layer of chemically compatible resin, which provides the required dielectric separator, may be used. (See Figure 1a.)

While the 18 or 12µm copper layer could be ablated by a UV laser this would take an unacceptable time since the small beam needs to be trepanned to achieve the required aperture size - hence the complete PCB is 'panel etched' to reduce the outer layer copper thickness to a nominal thickness of ~ 7 µm or less. (See Figure 1b.)

Using a UV laser, an opening can now be ablated in the copper surface. (See Figure 1c.). Final removal of the underlying dielectric material is then made using a CO_2 laser to produce the blind micro via. (See Figure 1d.)

The major disadvantages of this route are:

- The necessity of a panel etching operation reducing the capacity of any existing etch lines.
- Additional cost and time.
- Precise and uniform etching of large panels is difficult and final copper layer thickness may vary by ±2µm.
- Variation in copper thickness affects the reliability and quality of micro vias for the established power and pulse duration cycle of the UV laser.
- Poor etching will affect the overall planarity and uniformity of the final etched outer layer circuitry and may compromise the accuracy and reliability of fine pitch surface mounting of components.
- A more expensive dual head CO_2 + UV laser is required.

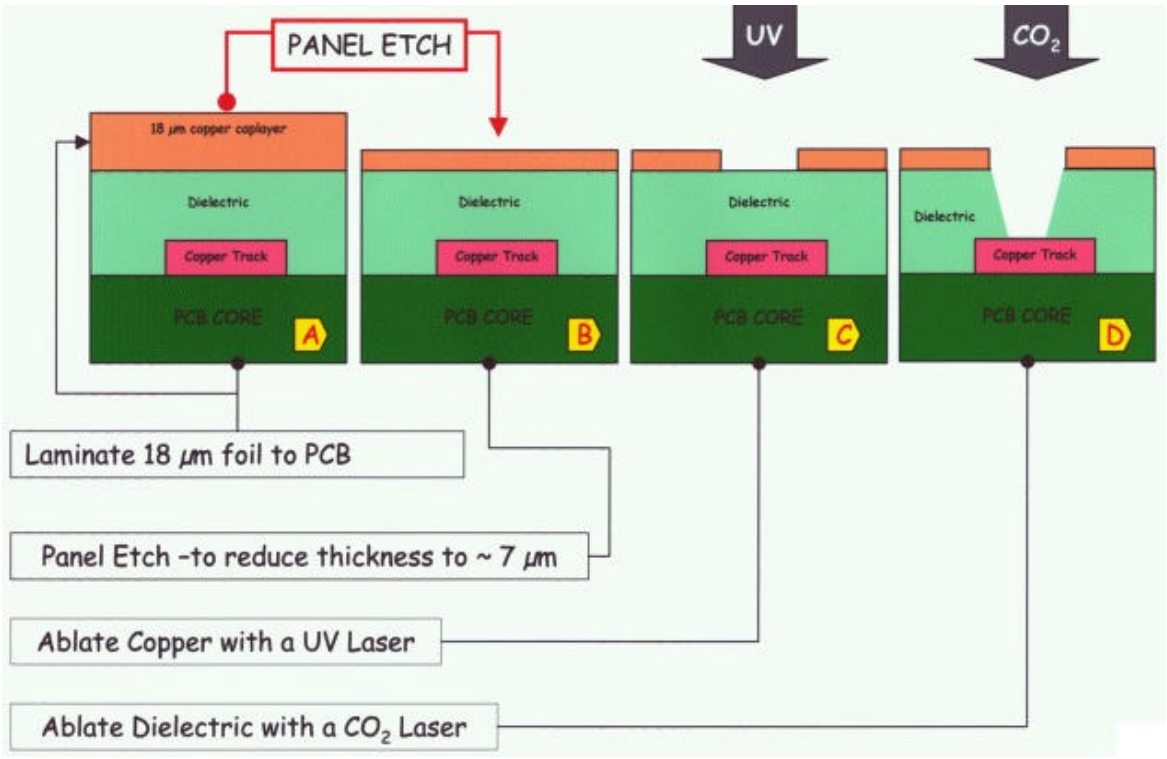


Figure 1 – Micro Via Formation – "Half-Etch" Route

As for the "Half-Etch" route, the first stage involves the lamination of a conventional 18µm or 12µm outer PCB cap. (See Figure 2a.)

Using this route the constraints of direct laser ablation of the thicker copper is overcome by chemically etching "windows" using conventional photochemical and pattern etching techniques. (See Figure 2B.) These windows , centered on the site of the micro via, then provide access to the underlying dielectric substrate, which can be easily ablated using a CO_2 laser. (See Figure 2C.)

The major disadvantages of this route are:

- The necessity for multiple stage photomechanical and etching process to create "windows"
- Increasing difficulty of maintaining inner layer registration.
- Additional cost and time.

For the first stage of this route the laminated outer layer cap is already a thin and a mechanically supported 5µm layer on a 35µm copper carrier. (See Figure3a.)

Ultra thin supported foils provide a user friendly easy-to-handle product, and are available with a functional layer of copper down to 3 µm on both one and two ounce (35µm & 70µm) mechanically peelable copper carriers.

Copper foils in this range of thickness can be ablated using a CO_2 laser, providing the copper surface is treated to increase its energy absorbing characteristics. This is normally achieved by wet panel chemical processing through a "brown or black oxide" conversion process to provide a thin layer of oxidized copper over its entire surface. (See Figure 3b.)

Once the thin copper has been ablated, subsequent removal of the contiguous under layer of dielectric substrate by the CO_2 laser follows in a single pass operation, completing the final blind micro via structure with a minimal footprint. (See Figure 3c.)

While the initial use of an ultra-thin foil eliminates many of the disadvantages of the previous two manufacturing routes, the PCBs still have to pass through wet chemical processing to achieve the required energy absorbing characteristics to allow direct copper ablation with a CO_2 laser.

We have developed an enhanced version of a peelable copper foil which, after easy mechanical removal of the supportive and protective 1 or 2 oz. copper carrier, can be directly processed and drilled using a CO_2 laser.

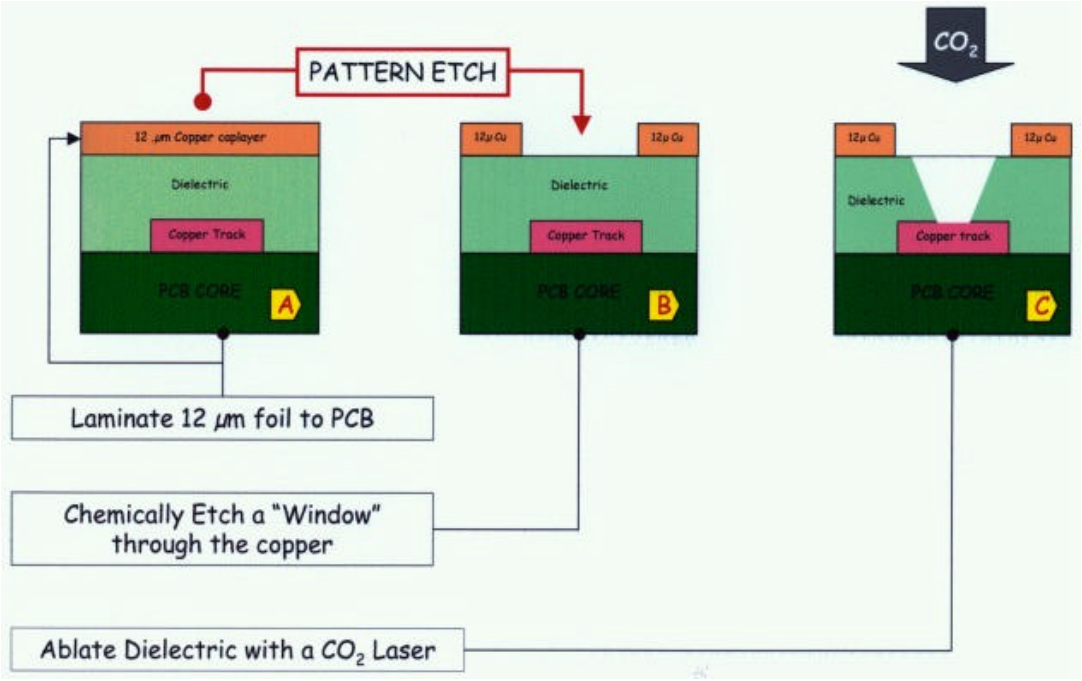


Figure 2 – Micro Via Formation – "Conformal Mask" Route

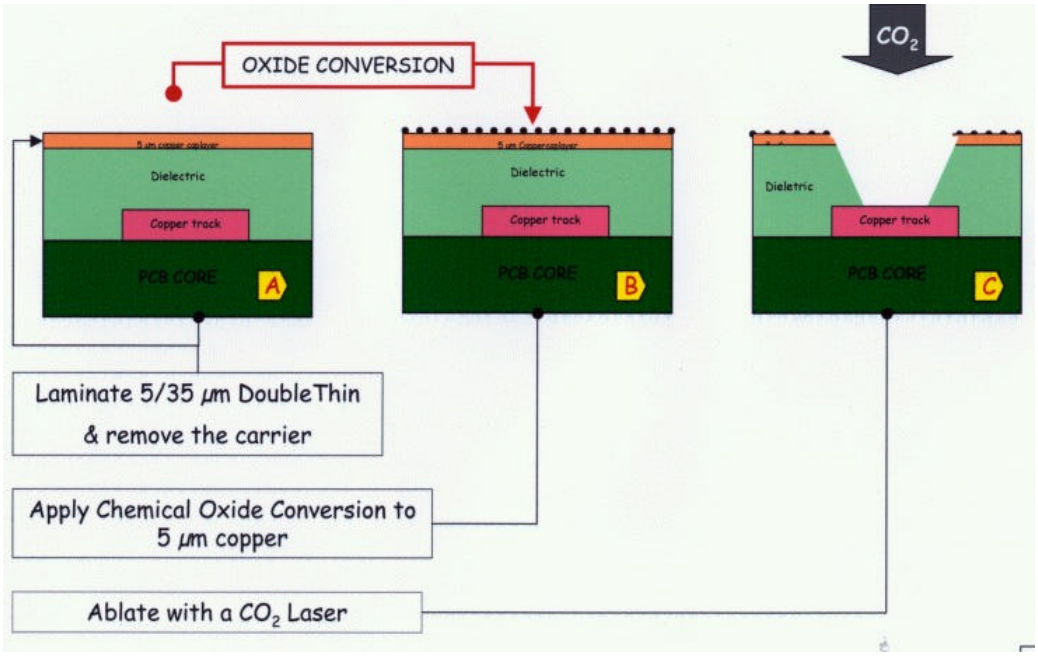


Figure 3 - The "Thin Foil + Oxide Conversion" Route

Laser Direct Drilling product is a mechanically peelable ultra thin 5µm copper layer, supported on a 35µm copper carrier, which after lamination and separation, provides an 'as received' blackened surface with improved energy absorption characteristics in the far infra-red spectrum.

The product is intended to be used in the manufacture of high density interconnect multi-layer printed circuit boards utilizing laser drilled buried and blind via manufacturing techniques.

This product brings together a range of key technical and manufacturing advantages to both the laminator and final user.

For the laminator, producing ultra-thin clad laminates; the composite foil is easy to mechanically handle during sheeting and lay-up operations due to the support of the 35µm carrier foil. For subsequent post-lamination operations such as breakdown, paneling and edge routing, the carrier continues to provide protection from mechanical handling damage.

For the end-user, damage to the ultra-thin functional surface from initial handling and storage is likewise eliminated while the carrier remains in place.

For the PCB manufacturer, laminating external caps for BUM construction, the copper carrier protects the ultra thin functional layer from mechanical damage and totally eliminates the risk of contamination from resin dust or other airborne particulates during the lamination cycle.

Ultra-thin foils provide 'per-sec', through semi-additive and 'flash etching' techniques, the ability to replicate very demanding features and fine track-to-space ratios.

The 'as received' blackened copper surface of the copper provides direct entrée to direct laser drilling. It eliminates the necessity for the use of chemical conversion coatings to achieve photo-thermal copper ablation.

The precise thickness control of the electroplated functional 5 µm layer ensures foil contributions to the non-planarity of the laminate surface, critical for surface mount applications, are minimal and significantly less than those produced from 'half - etching' of 18 or 12 µm foils

Product Architecture

The basic structure of the product (Figure 4) is described below:

1. The Carrier Foil is an 'in-house' electrodeposited 35 µm (1oz./ft.2) copper foil with a precisely controlled roughness (Ra ~ 0.3 µm).
2. The Release Layer (Figure 4a) is a very thin (~ 0.1 µm) layer of Chromium deposited onto the shiny side of the carrier foil, allowing the physical separation of the ultra-thin copper layer from the carrier foil after lamination. This layer is totally free of all organic materials and remains on the carrier foil after separation. The 'release bond' obtained is very low, typically 0.1lb./inch (~ 15 N/m.) and independent of lamination time and temperature constraints. Extended thermal exposure, as a consequence of the higher temperature and/or extended lamination times, cause no change to this value (Figure 11), even for the thermal rigor of a PTFE lamination cycle.
3. The energy absorption layer (Figure 4b) is a thin (~ 1 µm) proprietary ´darkened´ energy absorbing layer, deposited onto the chromium release layer, designed to maximize infra red absorption produced by CO_2 lasers (= 9400 nm). Its electrochemical application ensures both chemical consistency and uniformity of coverage ensuring reliable energy absorbing properties.
4. The 5µm Functional Layer consists of two parts. A nominal ~3.5µm of "base foil" (Figure 4c) and a "nodularisation/bonding layer" (~ 1µm) (Figure 4d) providing an increased micro roughness (Rz ~ 3.5 - 4.0 µm) and enhanced surface area to achieve the required laminate bonding characteristics. The overall uniformity of the ultra thin functional layer is illustrated by the very narrow area weight distribution data. Typical values for the laminate bond onto conventional FR4 (after 'copper build-up' to 35µm) are > 8.0 lb./inch (> 1.4 N/mm.). SPC data for both the area weight and laminate bond distribution is shown. (See Figure 5.)
5. The Barrier Layer (Figure 4e) is a thin (~0.2µm) layer of Zinc, plated onto the laminate bonding surface of the 5µm copper. During the lamination cycle, thermal diffusion of copper converts this to a layer of brass, providing a permanent diffusion barrier between the copper and chemically active constituents of the dielectric substrate, guaranteeing long term laminate bond integrity.
6. The passivation layer (Figure 4f) is a very thin (~ 100 A) organic free proprietary chromium based layer designed to prevent oxidation and chemical/electrochemical corrosion. A final process applies an extremely thin layer of 'silanes' to the bonding surface to enhance the laminate bond strength. (See Figure 4g.)

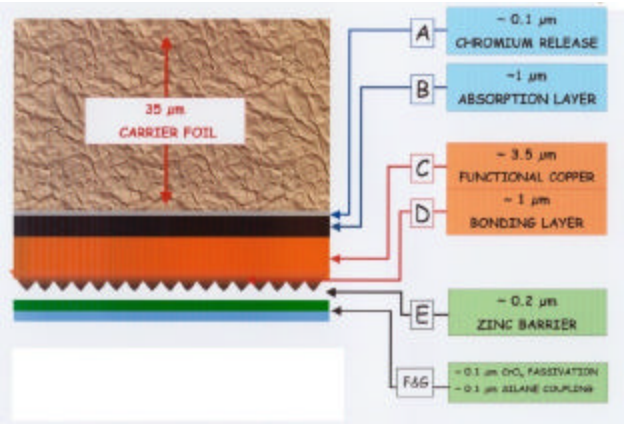
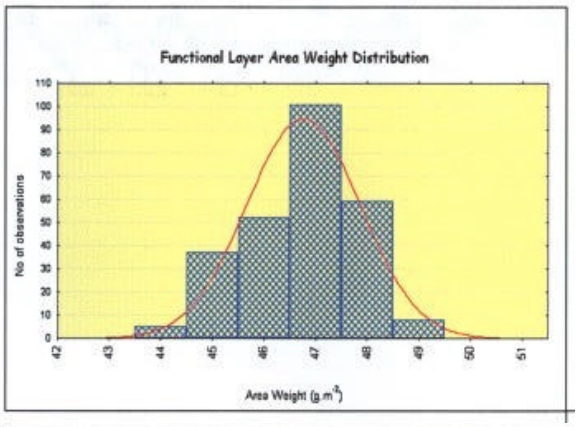


Figure 4 – Laser Direct Drill Product Architecture

Key product parameters are summarized in Figure 6.



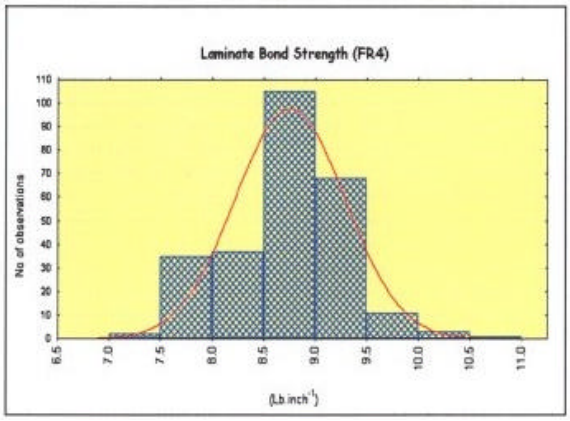


Figure 5 – 5/35 LDD Area Weight and Laminate Bond Data

MEASURED PARAMETER	units	value
Area Weight (functional layer)	oz/ft² g/m² g /254 in²	~ 0.15 ~ 45 ~ 7.4
Carrier Bond Strength	N/m Lb/in²	~15 ~ 0.10
Laminate Bond Strength (on FR4)	N/mm Lb/in²	~ 1.4 ~ 8.0
Shiny Side Roughness [Ra]	µm µ.inch	~ 0.6 ~ 24
Matte Side Roughness [Rz]	µm µ.inch	4 - 5 150 - 200

Figure 6 – Key Product Parameters Characteristics of the "Energy Absorbing Layer"

The typical appearance of the final laminate working surface of both the normal (pink copper color) and the 'LDD' (darkened) version of the peelable 5/35 ultra-thin products with their protective copper carrier partially removed, are shown in Figure 7. SEM photographs at x1000 and x5000 illustrate the topography of the 'darkened' energy-absorbing surface of the LDD product. (See Figure 8.)

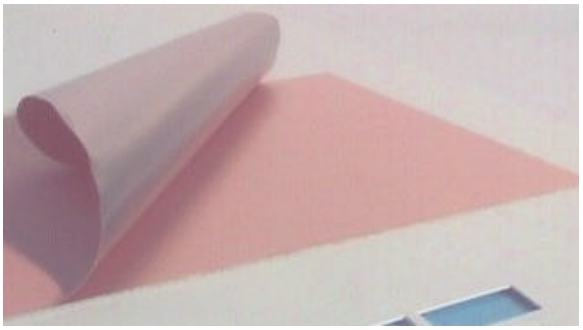


Figure 7a – Normal 5/35㎜ Double Thin

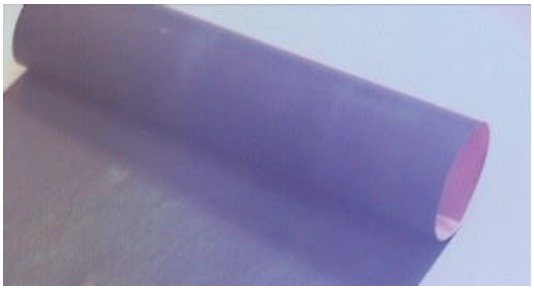


Figure 7b – Laser Direct Drill 5/35㎜ Double Thin

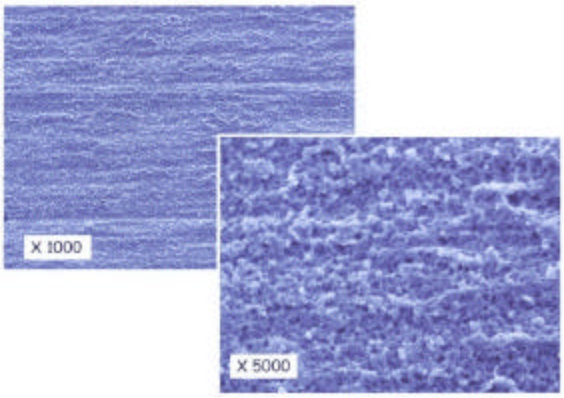
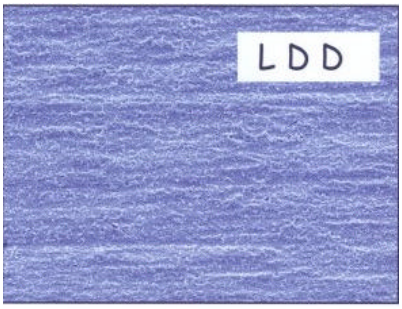


Figure 8 – LDD Energy Absorbing layer Topography

Longitudinal and transverse roughness data (Ra and Rz) compare the surface topography of the 'LDD and 'normal' versions of the 5/35µm products. (See Figure 9.) The LDD product shows slightly higher value.



5 / 35 µm LDD		
[µm]	Long	Trans
Ra	0.60	0.70
Rz	3.50	4.00

(a)

5 / 35 µm DoubleThin		
[µm]	Long	Trans
Ra	0.45	0.60
Rz	2.50	3.20

(b)

Figure 9 – Micro Roughness Comparison

Typical cross sections of laminated LDD product with the one ounce copper carrier in place and after its removal, (Figure 10) illustrate the structural relationship between the carrier, 'energy absorbing' and functional copper layers.

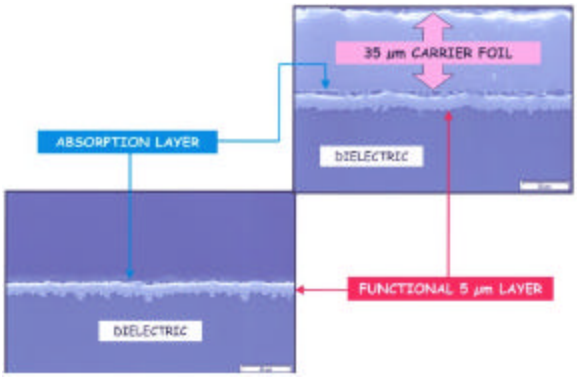


Figure 10 – Laminated LDD (with and without the Carrier Foil)

The unique energy absorbing characteristics of this darkened layer are key to the successful laser drilling characteristics - eliminating the necessity to use a more complex and costly dual system CO_2/UV-YAG laser.

$C0_2$ lasers, operating at 9400 nm, provide energy in the far IR region. The higher energy absorbing characteristics (Figure 11) of the 'darkened layer' of the LDD product compared to a 'chemical oxide treated' and untreated shiny copper, shows a typical x 2.5-3.0 increase in absorption at the lasing wavelength.

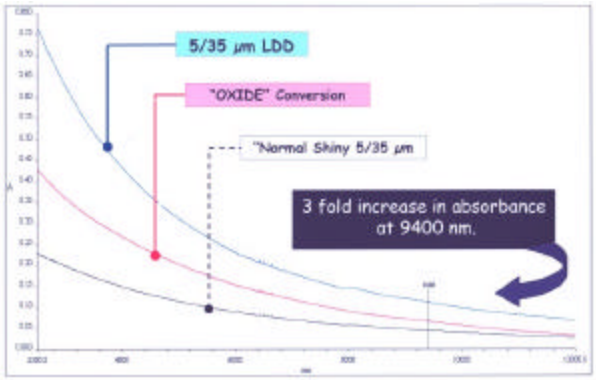
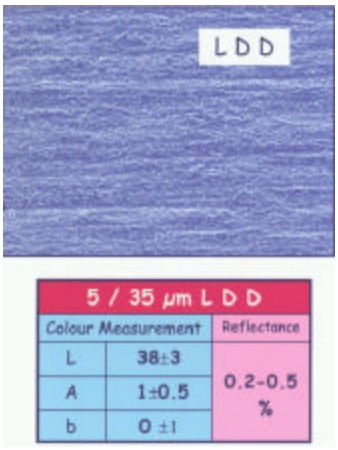


Figure 11 – FTIR Absorption Spectra Comparison

Corresponding comparative data for the LDD and 'normal' 5/35µm products for both surface gloss/reflectance and "CIE-LAB" color system information, clearly illustrate the significantly reduced 'reflecting power' of LDDs treated surface in the visible spectrum. (See Figure 12.)



(a)

(b)

Figure 12 – Color and Gloss/Reflectance Comparison

After formation of the micro vias, the energy-absorbing layer needs to be removed prior to subsequent de-smearing and conventional 'PTH' metallization process chemistries. Simple chemical removal using standard non-proprietary micro etchants, such as Sodium Persulphate, can be rapidly achieved (Figure 13). The reliability of both the composition and thickness of the layer ensures consistent uniform removal without affecting the underlying ultra thin functional copper layer. This can be seen from a comparison of the surface topography SEMs (Figure 14) of the LDD and the 'normal' (untreated shiny) copper surfaces after micro etching.

Historically, mechanically peelable ultra thin foils may, in certain circumstances of extensive thermal exposure (high and/or prolonged lamination or laminate 'post-bake' cycles), show an increase in the carrier peel strength compared to the 'as-received' values. (See Figure 15.) For the "normal" 5/35µm product, the effect of this can be limited by providing product with an initial "low-range" starting release bond. However, the LDD product shows no change at all to its release bond after very severe thermal cycles, retaining its initial low value of ~ 0.1b/inch, even after a very long and high temperature PTFE lamination cycle.

Examples of micro vias created using this product are shown in Figure 16 and 17.

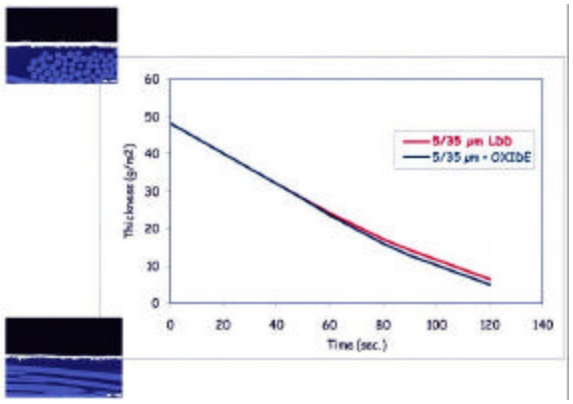


Figure 13 – Removal Rates for Surface Treatments

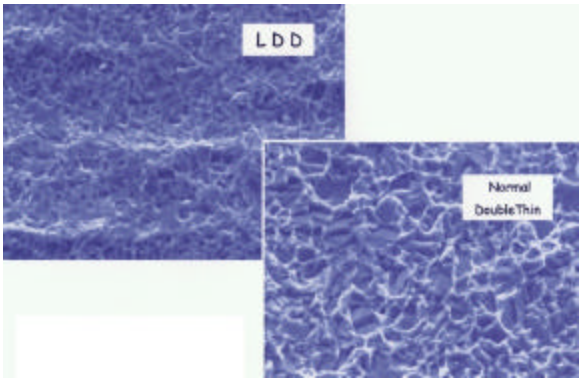


Figure 14 – Effect of Micro Etch (130g/l Sodium Persulphate + 70g/l H_2So_4 at 30 °C)

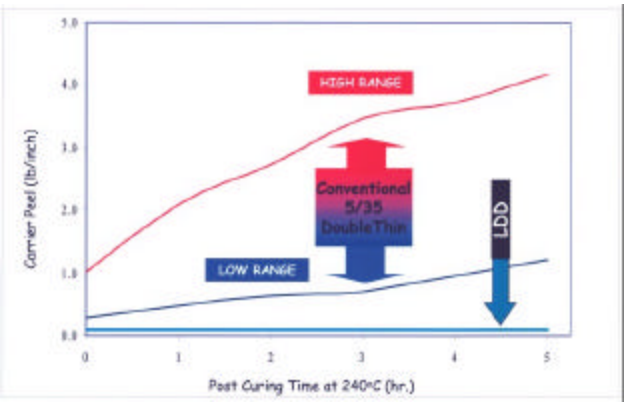


Figure 15 – Effect of Thermal Cycle on Carrier Bond

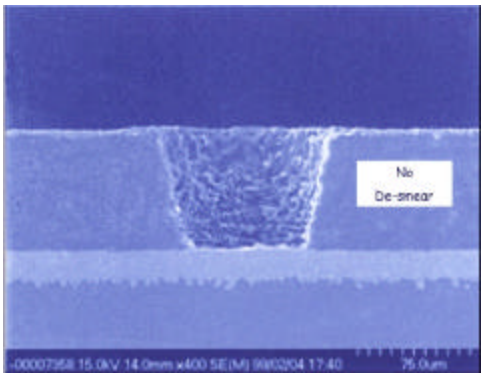


Figure 16 – Micro Via in 5mm LDD (Resin Coated Copper)

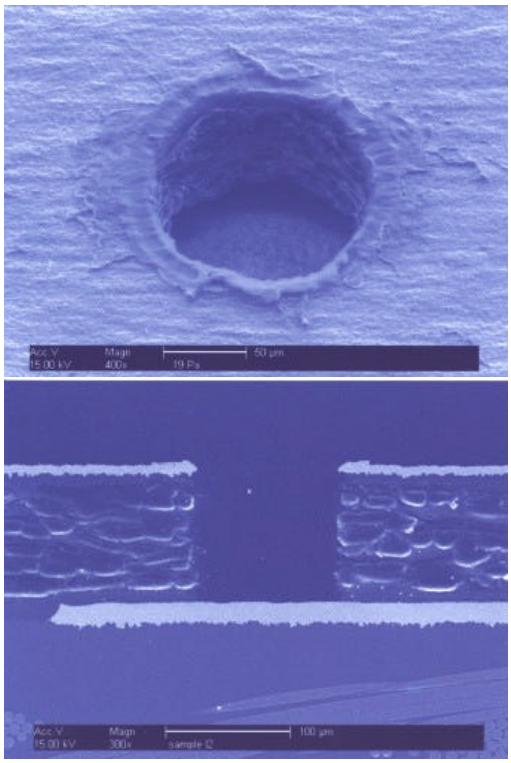


Figure 17 – Micro Via in 5mm LDD (Thermount)

Summary

The unique features of Circuit Foil's LDD product coalesce all of the vital raw material features required for a successful and cost effective entrée into advanced PCB manufacturing arenas. The product, in tandem with a range of dielectric substrates, is intended to be used for the manufacture of high density interconnect multi-layer printed circuit boards, utilizing laser drilled via manufacturing techniques.

The ability to 'Flash Etch" the ultra thin 5µm layer results in reduced etch times - the pre-requisite for producing fine line-to-track spacing and sub millimeter high definition surface mounting features.

Direct single pass laser ablation of both outer layer copper and the underlying dielectric, creating blind and buried vias using just a CO_2 laser, without any wet chemical pre-processing, brings significant manufacturing and cost advantages.

Pre processing operations and the costs of "Half-Etching", "Conformal Masking" and "Oxide Conversion" stages are eliminated.