Presented at IPC Printed Circuits Expo® 2002
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Electrically Mediated Pulse Reverse Copper Plating of Electronic Interconnects without Brighteners/Levelers

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Abstract
This paper describes a process for plating of interconnects for advanced electronic modules. In contrast to traditional chemical mediation of plating processes, this process is electrically mediated and does not rely on difficult to control brighteners/levelers. The methodology for selection of the electric mediation parameters is based on considerations of mass transfer and microprofiles/macroprofiles related to current distribution. This paper builds on earlier work by incorporating plating cell/tank design issues including air agitation, eductor agitation, eductor orientation, back and forth panel movement and knife-edge panel movement. Data for plating industry test panels containing microvias and PTHs of approximately 4:1, 10:1, and 20:1 aspect ratios are presented.

Introduction
The continuing trend towards miniaturization of consumer electronics is placing considerable technological challenges to all segments of the electronics industry. Specifically, the performance capabilities and miniaturization of integrated circuit (IC) devices are proceeding at a rate significantly faster than the printed wiring board technology required to interconnect them,[1] the need for chip scale packages (CSPs) and high density interconnect printed wiring boards (HDI-PWBs) has emerged. The CSP and HDI-PWB provide the z-axis interconnection between the IC and the PWB.

The challenge of plating electronic interconnects is one of leveling or throwing power, i.e. the uniform deposition of a conductor into the interconnect feature.[2] There are two types of leveling; geometric leveling and true leveling.

Geometric leveling results from a uniform or primary current distribution; consequently the plating rate must be very slow. Geometric leveling only occurs when the deposit is at least as thick as the depth of the interconnect feature; consequently the overplate is considerable. Geometric leveling is impractical for fabrication of electronic interconnects.

True leveling results from the preferential adsorption of a specific leveling additive or additives on the high current density areas, e.g. peaks or corners of the interconnect feature. True leveling requires precise control of these additives; also known as levelers and brighteners.

In conventional direct current (DC) plating of plated through holes (PTHs) for the PWB industry, leveling additives are incorporated in the plating bath to improve the throwing power and to yield a fine-grained deposit.[3,4] However, considerable challenges exist for extension or insertion of PTH electroplating processes to smaller and higher aspect ratio interconnect features Specifically, the proprietary chemistries used in “conventional” and “high throw” baths do not necessarily provide acceptable results for smaller interconnect features[5] and proprietary chemical formulations must be optimized for different feature sizes.[6] Furthermore, bath maintenance and control issues associated with the leveling additives are exacerbated at HDI, CSP and IC feature sizes.

To meet the plating challenge of advanced electronic interconnects, non-DC plating processes have recently received considerable interest[7-11]

While these non-DC processes have been referred to by a variety of names, eg. periodic reverse plating and pulse reverse plating, they all utilize brighteners and/or levelers and are therefore a form of true leveling. Consequently, the challenge of precise control of leveling additives remains. In addition,

these previous studies[7-11] have used one particular subset of waveform parameter space characterized by a long forward or cathodic pulse followed by a short reverse or anodic pulse.

However, as suggested from fundamental considerations,[12] changes in waveform parameters should have a substantial impact on copper plating of interconnect features. In addition, Rehrig and Mandich[13] studied of the effect of pulse plating parameters on throwing power. They suggested that "simple electronic manipulation of the pulse waveform" could be used to "tune" the electrodeposition process and replace the complicated brightener/leveler chemistries.

Recently, copper plating for electronic applications, **without brighteners and levelers**, has been reported.[14-16] This process is termed electrically mediated copper plating in contrast to the conventional chemically mediated approach using leveling additives. Below we present further results using electrically mediated copper plating of electronic interconnects.

Approach

In the electrically mediated approach, the forward on-time/peak current and reverse on-time/peak current are tuned to plate specific electronic features. The rationale basis for selecting the process parameters is derived from the influence of a pulsating current on the hydrodynamic diffusion layer. As shown in Figure 1.

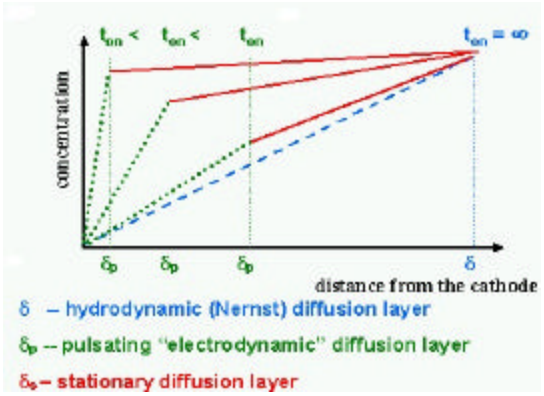

Figure 1 - Schematic Representation of the Duplex Diffusion Layer

during pulse plating a "duplex diffusion layer" develops. The duplex diffusion layer consists of a stationary layer and an inner pulsating layer. By assuming linear concentration gradients, Ibl[17,18] derived the following relationship between the pulsating diffusion layer and the on time of the pulse

$$\delta_p \approx (2Dt_{on}) \qquad (1)$$

where "D" is the diffusion constant, "t_{on}" is the on time of the pulse and "δ_p" is the pulsating diffusion layer. More recently, using a similar duplex diffusion layer approach the same relationship was derived for "pulse-with-reverse" plating.[19] Since the pulsating diffusion layer is determined by the on time of the pulse, we refer to it as the "electrodynamic diffusion layer." As shown in Figure 2, proper selection of the electrodynamic diffusion layer can convert a macroprofile to a smaller macroprofile or convert a microprofile to a smaller microprofile.

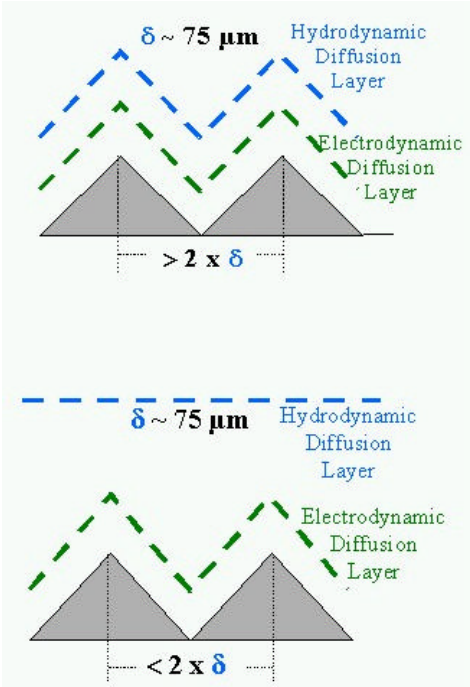

Figure 2 - Relationship Between the Hydrodynamic Diffusion Layer and the Electrodynamic Diffusion Layer for (a) Macroprofile (b) Microprofile

However, in order for diffusion processes and hence the electrodynamic diffusion layer to influence the plating process, mass transport effects must be significant during the duration of the pulse. The time required for the concentration of reacting species at the interface to be depleted to zero is know as the transition time, τ, and is given by the Sand equation

$$\tau \approx ((nF)^2\ C^2D)/2i_{on}^2 \qquad (2)$$

where "n" is the number of electrons, "F" is Faraday's constant, "C" is the bulk concentration of reacting species, and "i_{on}" is the pulse current. Consequently, mass transport effects influence the plating process when the transition time is significantly less than the on time,

$$\tau << t_{on} \qquad (3)$$

While the theoretical framework is not sophisticated enough to allow *a priori* determination of waveform parameters, the above discussion and previous work[14-16] provides substantial guidance. Specifically, low aspect ratio PTHs are macroprofiles and require a relatively long forward on time followed by a relatively short reverse on time. The sum of the forward on time and reverse on time, as well as any off-times, is approximately 10 to 20 msec, or 50 to 100 Hz. The general form of the electrically mediated process waveform for low aspect ratio PTHs is presented in Figure 3.

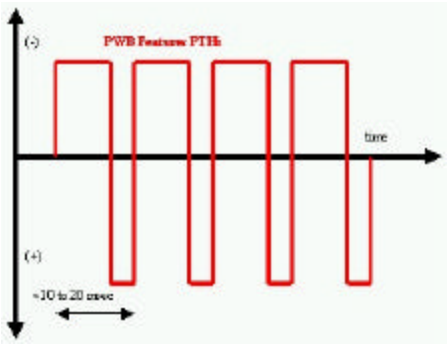

Figure 3 - Generalized Waveform for a PTH

High aspect ratio PTHs and microvias are hydrodynamically inaccessible macroprofiles and microprofiles, respectively. These interconnect features are expected to require short forward on-time/high forward peak current followed by a relatively long reverse on-time/low reverse peak current. For high aspect ratio PTHs and microvias, the sum of the forward on time and reverse on time, as well as any off-times, is approximately 1 to 2 msec, or 500 to 1000 Hz. The general form of the electrically mediated process waveforms for high aspect PTHs/microvias is presented in Figure 4.

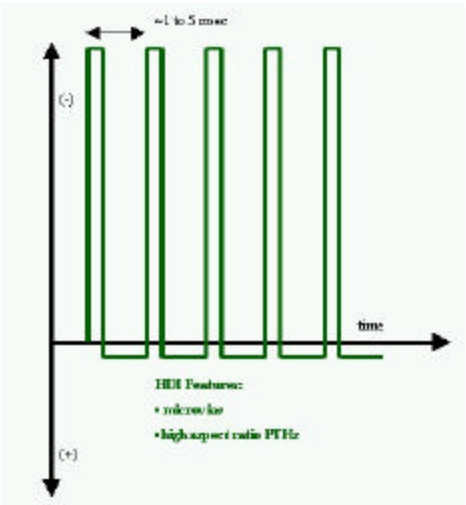

Figure 4 - Generalized Waveform for High Aspect Ratio PTHs and Microvias

Experimental

An acid copper sulfate solution containing 60 g/L $CuSO_4$, 9% by volume of H_2SO_4, 60 ppm Cl^-, and 350 ppm polyethylene glycol (PEG) was used as the copper-electroplating bath for all experiments. The chloride/PEG acts as a suppressor and is not difficult to control.[20] The plating bath does not contain difficult to monitor/control additives such as brighteners and/or levelers. The plating bath temperature was 25 °C.

Plating experiments were conducted on 8"x18" test panels of 0.260" thickness depicted in Figure 5. The test panels contained microvias (75µm), PTHs (4:1 and 10:1 aspect ratios), and ball grid arrays BGAs (20:1 aspect ratio). The plating line (vertical) consisted of a single panel flight bar with eductors oriented at 90° perpendicular, knife edge agitation, soluble anodes, and in a subsequent experiment flight bar vibration.

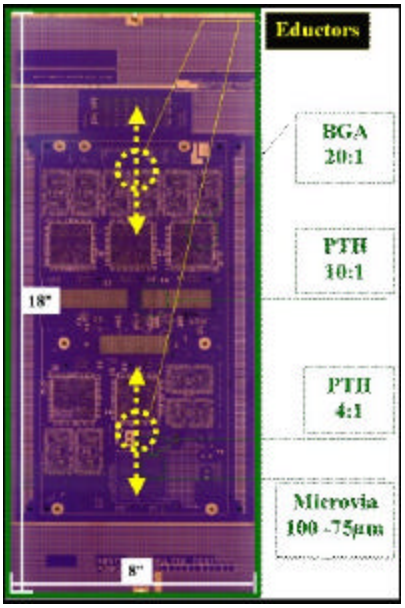

Figure 5 - Picture of Test Panel

Results

The target performance criteria was to plate approximately 1 mil of copper in the interconnect feature in approximately 180 minutes. (Note, a later target was to plate approximately 1 mil of copper in approximately 120 minutes.) To quickly access the efficacy of the electrically mediated approach, our target was ratio to plate 0.3 mil of copper in 60 minutes. An additional target was to achieve a high throwing power of approximately 70% or higher. This criteria was to keep the amount of copper plated on the surface manageable. In fact this is less of a concern for the electrically mediated process because excess copper may easily be removed with a DC etch in the same additive-free plating solution.[21]

In Table 1 are data for copper plating for 60 minutes using electrically mediated process parameters Test 1-7. The BGA (20:1 A/R) and PTH (10:1 A/R) meet the target criteria of 0.3 mil in the interconnect feature center with 100% throwing power. The PTH (4:1 A/R) exceeds the target criteria with 1.2 mil of copper in the interconnect feature center with 100% throwing power. In addition, the BGA and PTHs exhibited uniform copper plating within the barrel and no tapering of the deposit or dog boning effects were observed. The microvia was filled with copper with 2.5 mil of surface copper.

Table 1 - Copper Deposit Thickness in Interconnect Feature with Electrically Mediated Plating (60 minutes)

	BGA (20:1 A/R)	PTH (10:1 A/R)	PTH (4:1 A/R)	Microvia
Surface	0.0003"	0.0003"	0.0012"	0.0025"
Center	0.0003"	0.0003"	0.0012"	Filled

In Figures 6 through 8 the amount of copper deposited as a function of time in the center of the interconnect feature and on the surface of the interconnect feature, respectively, is presented. For the low aspect ratio PTH (4:1), the copper deposition proceeds approximately linearly with time for both the surface and feature center. However, the throwing power, i.e. the ratio of the copper deposit thickness in the center to the copper deposit on the surface, decreases with plating time. For the higher aspect ratio PTH (10:1) and BGA (20:1), the copper deposit thickness on the surface is approximately linear with time. However, the copper deposit thickness in the center effectively stops after 90 to 120 minutes for the BGA (20:1) and PTH (10:1), respectively.

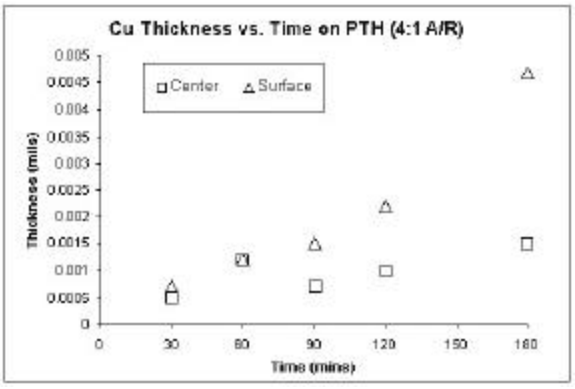

Figure 6 - Copper Deposit in the Center of the PTH (4:1 A/R) Interconnect Feature as a Function of Time

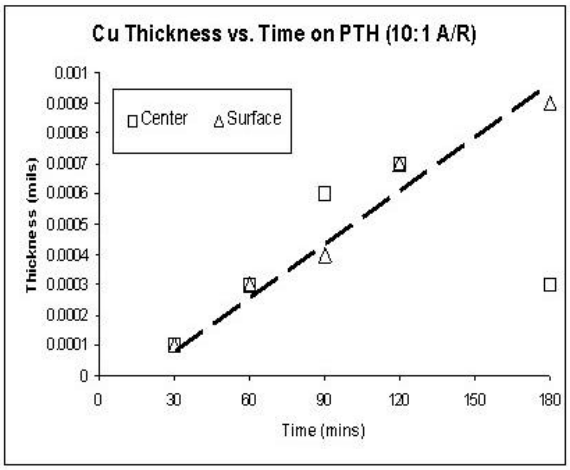

Figure 7 - Copper Deposit on the Surface of the PTH (10:1 A/R) Interconnect Feature as a Function of Time

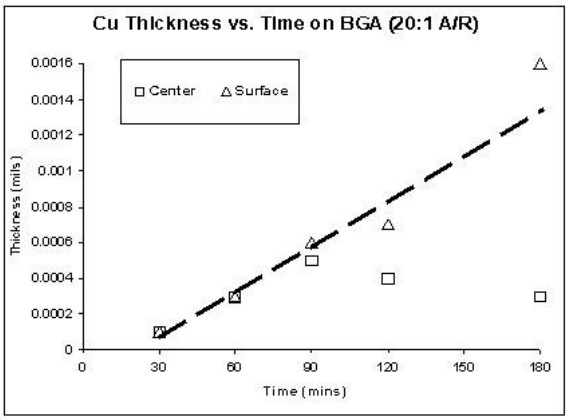

Figure 8 - Copper Deposit on the Surface of the PTH (20:1 A/R) Interconnect Feature as a Function of Time

It was hypothesized that the limitation to copper plating in the center of the smaller interconnect features may be attributed to plugging of the features with a precipitate or hydrogen gas bubbles. An additional rationalization to explain the limitation to copper plating could include the depletion of copper ions within the interconnect feature.

To address these possible explanations for the limitation of copper plating within the interconnects, the timing of the electrically mediated process waveform was modified (Test 1-46) and a vibration device was added to the test panel flight bar. In addition, the plating time was reduced from 180 to 120 minutes. The results of these experiments are presented in Table 2. The microvia was filled and the PTH (4:1 A/R) was plated with 1.5-mil copper in the center and 2.6-mil copper on the surface. Of significant note is the copper deposited in the center and on the surface of the BGA (20:1 A/R) was 0.8 mil and 0.8 mils, respectively. In addition, the copper

deposited in the center and on the surface of the PTH (10:1 A/R) was 0.93 and 0.9 mils, respectively.

Table 2 - Copper Deposit Thickness in Interconnect Feature with Electrically Mediated Plating and Vibratory Flight Bar (120 min)

	BGA (20:1 A/R)	PTH (10:1 A/R)	PTH (4:1 A/R)	Micro via
Surface	0.0008"	0.0009"	0.0026"	0.0055"
Center	0.0008"	0.0009"	0.0015"	Filled

A final question regarding the electrically mediated process control with an electrolyte devoid of brighteners and levelers is the mechanical properties, specifically ductility, of the copper deposit. To obtain preliminary data regarding the mechanical properties of the electrically mediated copper deposit, a sample was subjected to a 10X solder shock. After the 10X solder shock test, the copper deposit maintained its' integrity and did not exhibit any signs of cracking or failure.

The fact that the good ductility is obtained without brighteners and levelers using the electrically mediated process is easily rationalized. Improved ductility is related to smaller grain sizes, which is inturn, related to the nucleation density during copper deposition. The nucleation density, ? , is related to the current density, i, on-time, t_{on}, and nucleation constant, k, by

$$(4) \quad ? \approx i/(k(t_{on})^3$$

Consequently, the higher peak currents and short on-times utilized in the electrically mediated process compared to the DC process would be expected to increase the nucleation density and hence the ductility. Consequently, the need for brighteners and levelers to achieve the required mechanical properties for electronic interconnects is not required for the electrically mediated process.

Future activities will focus of evaluating the electrically mediated process under production conditions, specifically, using production scale rectification and production tank configurations. In addition to copper deposit distribution, the mechanical properties of the copper deposit will be evaluated using IST coupons.

Summary

An electrically mediated process for copper plating of electronic interconnects is described[22-26]. In contrast to conventional plating art based on brightening/leveling additives, the electrically mediated process is based on predictable knowledge.

The critical parameters of the electrically mediated process are forward and reverse on-times and forward and reverse peak currents. By understanding the influence of the electrodynamic diffusion layer on macroprofiles and microprofiles, The process parameters are tuned to the electronic interconnect feature size of interest. As additional knowledge and experience is derived from the electrically mediated process, a library of process parameters will be developed. Consequently, as new electronic packages are required, the electrically mediated process parameters will be selected from a library of process parameters.

Acknowledgement

The authors acknowledge the efforts of P. Miller for technical editing of the manuscript. The financial support of the U.S. Army Space and Missile Defense Command (Contract DASG60-01-C-0056), Faraday Technology, Inc., and Multilayer Inc. are gratefully acknowledged.

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