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Electrochemical Migration Testing Results - Evaluating PWB Design, Manufacturing Process, and Laminate Material Impacts on CAF Resistance

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Abstract
Various requirements have developed for printed wiring boards regarding the minimum spacing between features. Creepage distances per UL-60950 call out 1.2mm for voltages up to 50v, and call out 1.4mm for voltages up to 100v, for products classified under pollution degree2 material group IIIa. IEC-664 has an altitude factor that needs to be added for any product that is designed to go over 2000m altitude (for 3000m product there is an additional 14 percent). Tyco has established rules, which do not allow spacing on a product to go below certain minimums, depending upon the class of product. The UL-1012 sets spacing limits for power supplies. Telcordia GR-78, Section 13.1.5, specifies minimum 10 megohms (10E+10 ohms) after 1,000 hours at 85 °C, 85% RH, and 100 VDC bias as their minimum standard for electrochemical migration resistance testing for an expected 25 year minimum product life requirement.

For many years Sun Microsystems has required a minimum 0.035 inches from drilled hole wall edge to drilled hole wall edge for adjacent component holes, and minimum 0.025 inches from drilled hole wall edge to drilled hole wall edge for adjacent through-hole vias, for certain standard voltage requirements. These standards for electrochemical migration resistance between internal features or the printed wiring board, also known as resistance to conductive anodic filament growth or "CAF" resistance, were based upon earlier AT&T data and actual experience by Sun Microsystems with products in the field. Today more and more boards are being designed with relatively high I/O PBGA packages, and associated with these devices are fairly dense arrangements of through-hole vias. The increases in trace routing density are also driving higher via density. New connectors are being developed which have higher pin density and/or need to carry higher voltages. As a result of these trends, there is strong interest in more accurately evaluating the corresponding electrochemical migration or CAF reliability risk for a variety of component and via plated-through hole-to-hole spacing.

The following paper documents some of the difficulties faced in developing a temperature/humidity/bias test and data analysis methodology for comparing the electrochemical migration or CAF resistance of various standard and alternate printed wiring board (PWB or PCB Fab) laminate materials. These findings should be of interest to those evaluating material, design, and process effects on electrochemical migration resistance. Please note that this electrochemical migration paper focuses on CAF formation, not surface dendritic growth.

Conductive Anodic Filament (CAF) Growth: Definition

Conductive anodic filament (CAF) growth is a type of electrochemical migration (ECM), which can consist primarily of metallic conductive salts being transported across a nonmetallic substrate under the influence of an applied electric field. In standard FR-4 laminate materials, electrochemical migration failures within printed wiring boards have been characterized as CAF leakage paths forming along the glass fiber reinforcement at the epoxy-fiberglass interface due to chemical hydrolysis of the silane coupling agent. Sufficient moisture/vapor pressure, but not voltage bias or current, is necessary for the first stage in forming of these leakage paths. The second stage of conductive anodic filament growth (See Figure 1) then occurs when a voltage potential or bias voltage is applied.

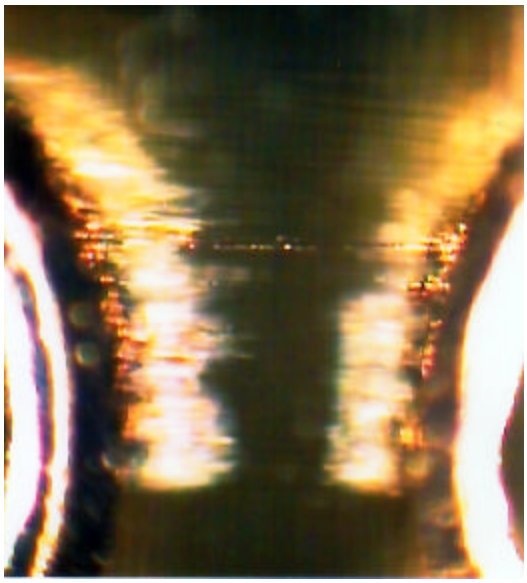

Figure 1 – Conductive Anodic Filament Growth

CAF growth between plated-through holes or from a plated-through hole (PTH) to an otherwise isolated plane layer, trace, or other feature is also affected by mechanical stresses causing delamination that promotes formation of CAF leakage paths along the interfaces of glass fibers with the polymer matrix. These mechanical stresses can be from the initial drilling of a PTH (may include some glass fibers being ripped out of the epoxy polymer matrix surrounding the hole perimeter), CTE mismatch during thermal cycling, etc.). Although CAF failure can also occur trace to hole, trace-to-trace, and layer-to-layer, the most common CAF failure mode is hole to hole.[4]

Background Of Conductive Anodic Filament Growth and Literature Search

Early research done by Bell Labs showed epoxy to glass debonding with moisture. If the glass treatment was poor (inadequate wetting of resin with the fiber reinforcement) then there was fast failure. If the glass treatment was good, then the "slow" hydrolysis of the silane treatment was seen, and was apparently reversible by baking. Foreign material on the glass or in the epoxy was also shown to cause fast failure.

Later research P. Mitchell, T.L. Welsher, and others has further developed what is known and understood about CAF failure mechanisms for various laminate materials. Some resin systems are more prone to CAF failure, and in those resin systems where woven glass is the reinforcement, the CAF failure risk is greater than if the reinforcement were chopped glass. The rate of moisture absorption in laminates increases as the temperature increases, and so does the risk of CAF failure. For FR-4 laminate material, the glass finish, resin purity, the resin/glass cross-linking agent, and resin wet-out characteristics as well as resin moisture absorption characteristics can have an effect. In addition, greater degradation along the epoxy resin/glass interface can occur during "normal" thermal cycling (20-200°C) due to stresses caused by the CTE mismatch between materials.[1]

Theoretical models for the CAF failure mechanism have also been developed. Although the Bell Labs and CALCE (Univ. of MD) models appear quite different, the Bell Labs model and the adjusted CALCE model predict a very similar 8X increase in CAF failure risk for a design change from plated-through holes 0.050 inches (1.27 mm) apart with 0.014 inches diameter to plated-through holes 0.0315 (0.80 mm) inches center-center with 0.0127 inches diameter (as drilled).

RESIN	REINFORCEMENT	H-H CAF RESISTANCE
Triazine	Woven glass	Excellent
Bismaleimide Triazine (BT)	Woven glass	Excellent
Polyimide	Woven glass	Excellent
Polysulfone	Chopped Glass	Excellent
Polyphenylene-sulfide	Chopped Glass	Good
Polyester	Chopped Glass	Good
	Woven & Chopped Glass	Low
Epoxy, flexible	Non Woven Polyester	Good
	Non Woven Polyester & Glass	Good
	Woven Glass	Good
Epoxy, Rigid	Woven Glass	Poor
	Woven Kevlar	Poor

Figure 2 – CAF Resistance

Bell Labs (FR4 Laminate Material):

$$MTF = a(1+bL^n/V)H^d \exp(E/kT)$$

Valid from 50-100°C, 60-95% RH, for a given lot
Lot to lot variation of up to 2 orders of magnitude
Data with L (spacing) from 33 to 58 suggests n ~ 4

If V, T and H are constant then MTF = $a+b(L^n)$ where a and b are constants
If L=36.0 mil for 50.0 mil (1.27 mm) pitch in 1995 : MTF = $a+b(1.7*10^{+6})$
If L=18.8 mil for 31.5 mil (0.80 mm) pitch in 2004 : MTF = $a+b(2.1*10^{+5})$

=> Over 8X Difference

Adjusted CALCE Model (Univ. of Maryland):

$$t(f) = \frac{p\,a\,R\,T}{2\,n\,F\,M\,C'\,H\,V}\,(L-2D)^2\,e^{E/RT}$$

t(f) time to failure
a volume fraction of filament
R gas constant
E activation energy
C' copper ion concentration
H relative humidity
n number of valence electrons (n=2 for Cu2+)
p density of copper
L initial spacing of inter-electrode region
T absolute temperature
M ion mobility constant (FR-4)
F Faraday constant
V voltage (bias)
D readily conductive region around PTH

If L = 36.0 mil (1995)
If L = 18.8 mil (est. 2004)

=> Over 8X Difference

CAF Test Vehicle and Test Plan Development

The standard Telcordia GR-78, Section 13.1.5, specifies a minimum resistance after 1,000 hours at 85 °C, 85% RH, and 100 VDC bias as their minimum standard for electrochemical migration/conductive anodic filament (CAF) resistance when a minimum 25 years of product life in the field is required. Bellcore requires this additional/special testing when plated-through hole wall to plated-through hole wall spacing is less than 0.050 inches and/or higher voltages are used. Further information regarding how this standard is applied has not been made generally available to the industry, including the appropriate design of a CAF test vehicle and how the test bias voltage is most appropriately selected.

It has been reported that some CAF test boards/coupons have been designed containing a designated range of hole-to-hole spacing, some from 0.006 to 0.035 inches, although only a few boards were tested. One CAF test board version has 20 holes and 10 gaps or opportunities for CAF failure per daisy chain tested. In addition to having relatively few opportunities for CAF failure, many of today's CAF test boards for evaluating hole to hole spacing impact on CAF resistance have only a few layers and do not represent well today's higher layer count boards with thinner dielectrics.[12]

The 10-layer test board that Sun Microsystems developed a few years ago for evaluating the insulation resistance between internal conductors within a printed wiring board has the following key features for evaluating hole-hole CAF resistance.

Holes In-Line (in-line with glass fiber direction, see Figure 3):

- for each spacing there are two rows of 42 signal1 vias each
- between three rows of 42 signal2 vias each; for a total of 168
- potential in-line PTH-PTH failures per spacing/test daisy chain.

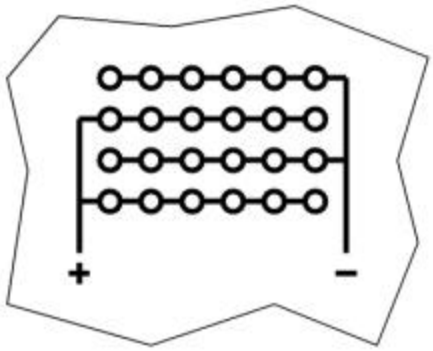

Figure 3 – In-Line Hole-to-Hole

Holes Staggered (closest PTH-PTH spacing in diagonal direction, see Figure 4):

- for each spacing there are three rows of 26 signal1 vias each
- between four rows of 27 signal2 vias each; for a total of 312
- potential diagonal PTH-PTH failures per spacing/test daisy chain.

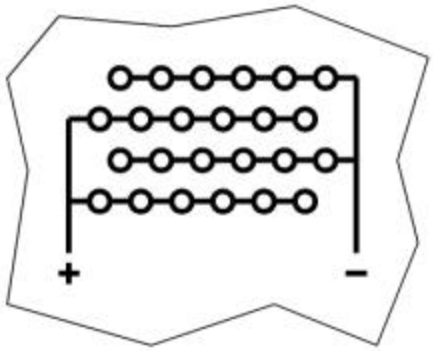

Figure 4 – Staggered Hole-to-Hole

For comparison, on a typical 1,428 I/O BGA device there are about 500 power/ground pins. (See Figure 5.) So with an average of slightly less than two adjacent power/ground pin spacing per pin there are about 1,000 potential in-line hole-hole CAF failure sites per BGA device. For a production board with the equivalent of 3 of these BGA devices and about 1200 passives or other components with close power/ground pin spacing, the total number of opportunities for in-line CAF failure would then be about 4,200 (about the same as the entire CAF test board sample lot of 25 pieces).

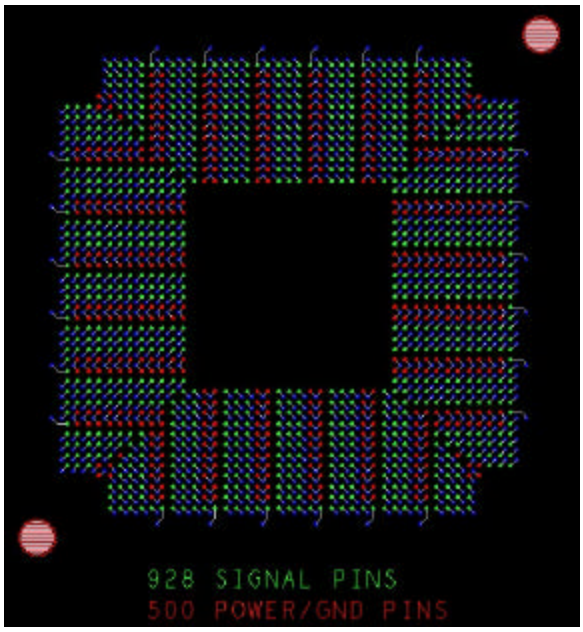

Figure 5 – BGA Device I/O Pin Assignment

CAF Test Circuit Setup

The CAF test circuit set-up used is very similar to that used for SIR testing (reference IPC-TM-650, Section 2.6.14.1), including a one megohm (10E+6) current limiting resistor in each current path/test circuit/daisy chain. The one-megohm resistance value for the current limiting resistor seems based upon best enabling visual confirmation of the failure mechanism. When higher current limiting resistor values are used, reductions in insulation resistance during ECM testing appear more transient. When lower current limiting resistor values are used, the thermal damage to the surrounding epoxy when a failure does occur is more extensive. Therefore care should be taken to ensure that the total resistance for each CAF daisy chain test circuit is consistently the same.

Note: The consistency of CAF test results might be improved by the use of a lower standard current limiting resistor value. The current limiting resistor value, and perhaps other CAF test parameter standards, could be varied in a proposed Round Robin test for improving this CAF test method.

CAF Resistance Test Method

The CAF test method consistently used by Sun Microsystems does differ somewhat from the Telcordia CAF test method and criteria for a 25-year desired minimum product life. Using the Adjusted CALCE Model for CAF failure, a shorter CAF test time was achieved by calculating a 0.0042 inches spacing "safety margin". When added to the 500-hour CAF test results that show a minimum spacing with no CAF failures on ~25 CAF test boards, the 0.0042 inches additional spacing (see safety margin calculation below) is added to determine the minimum design spacing for a 20-year desired minimum product life. The constant K consists of the remaining factors including bias voltage and humidity, which remain essentially the same.

Telcordia	1,000 Hours = (85 °C + 273C)*((.0350"-.010")^2)*K
20-year	800 Hours = (85 °C + 273
Life:	°C)*((.0324"-.010")^2)*K
Sun Micro	500 Hours = (65 °C + 273 °C)*((.0282"-.010")^2)*K

Actual CAF Test Example:
500 Hours =(65 °C + 273 °C) *((.0255"-.010")^2)*K(new material/process)

=> .0255 + .0042 = .0297 inches new 20-year minimum design spacing

In addition to the lower cost achieved by reducing the CAF test time in half, the lower 65C conditioning temperature is used. Using the lower 65C conditioning temperature reduces the excursion from actual board field conditions, and is low enough to not sublimate possible flux or other residues that may remain when certain board finishes are used. Sublimation can artificially reduce the activity of these residues, resulting in inaccurate assessment of CAF reliability risk.

Some report increasing the bias voltage as an alternative method for reducing the CAF test time required. However the higher voltage is not only a greater excursion from actual board field conditions, but also increases the risk of surface insulation resistance failures occurring and contaminating the failure data, potentially rendering the data useless for determining the CAF resistance.

Analysis Methodology

The CAF test pass/fail criteria used consistently by Sun Microsystems and others is a maximum decade drop in the insulation resistance. Sun's use of 25 test boards in a sample lot for CAF testing allows observation of a nearly bell curve distribution for the 96-hour daisy chain test circuit insulation resistance values in the expected region, the average value of which is used as the standard from which to determine whether a decade drop in insulation resistance has occurred for the remainder of the testing. After 500 hours, the test circuits with lower insulation resistance can then have their pass or fail status easily determined. It is important that insulation resistance values of CAF test circuits with larger spacings not be used in calculating the expected insulation resistance for CAF test circuits with smaller spacings.

In addition to what has been described above for

determining the minimum plated-through hole-to-hole spacing rules for achieving a specified minimum product life, this CAF testing can be used to evaluate the effect of alternate materials, designs, and processes on CAF resistance. For example, the company has found that while at larger spacings some laminate materials offer significantly more CAF resistance, that at smaller plated-through hole to hole spacings the CAF failures have increased - perhaps because this laminate material is also more brittle, fracturing more easily and at smaller spacings significantly reducing the area of intact laminate between holes.

The various CAF testing results that our company has now obtained, in combination with company data going back nearly 20 years, apparently allow for the development of a complete model for determining the CAF resistance of a printed wiring board in terms of its expected minimum product life in the field. Altogether the standard CAF Test Board, the CAF test procedure, and the CAF failure risk model developed, enable more timely and cost-effective CAF testing and evaluation of board design, material, and manufacturing process alternates not only for those seeking eventual approval by Bellcore, but also for those seeking assurance that other specified minimum product life requirements in field will be met for a given product.

CAF Electrochemical Migration Test Results

1) The CALCE (Univ. of MD) diffusion controlled reaction model for initiation of the CAF failure mechanism has been adjusted to show the extent of the "readily conductive region" (shown as "D" below) around plated-through holes based on the CAF test data obtained by conditioning 25 samples of standard FR-4 laminate material at 100 VDC bias and comparing the results with samples of standard FR-4 laminate material conditioned at 10 VDC bias.)

$$t(f) = \frac{p\,a\,R\,T}{2\,n\,F\,M\,C'\,H\,V}\,(L-2D)^{\wedge}2\;e^{E/RT}$$

2) Earlier CAF test results which showed no impact on CAF resistance included testing standard FR-4 laminate test boards with standard versus severe (2X) plated-through hole desmear treatment, and extending CAF temperature/humidity/bias testing from 500 to 700 hours. (See Figure 6.)

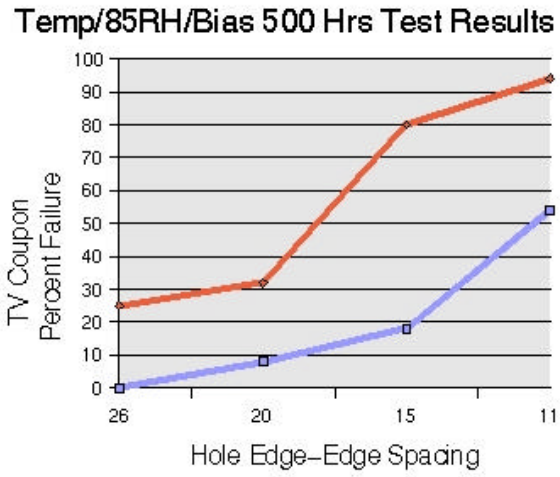

Figure 6 - CAF Test Results Showing D = ~0.005 Inches

3) Recent CAF test results for standard versus high Tg FR-4 laminate material; InLine PTHs: (See Figure 7.)
   - A2 shows effect of more brittle nature of this higher Tg laminate material
   - A3 indicates extent of readily conductive region (D) around PTHs

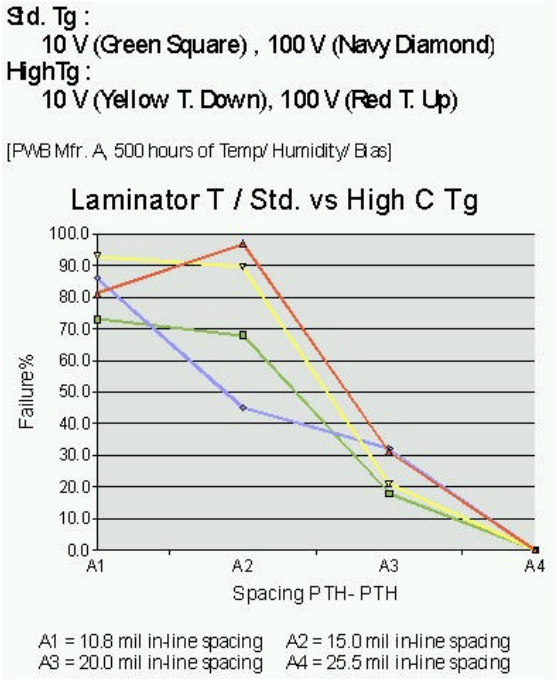

Figure 7 - Std. vs Hi Tg - Laminator T - InLine PTH-PTH

4) Recent CAF test results for standard versus high Tg FR-4 laminate material, Staggered PTHs: See Figure 8.)
   - B1 shows effect of more brittle nature of this higher Tg laminate material
   - B2 and B3 show greater CAF resistance with staggered/diagonal PTHs

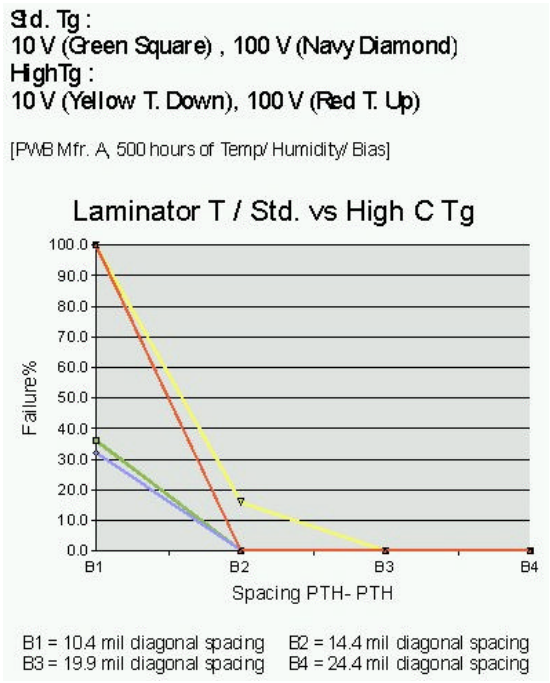

Figure 8 - Std. vs Hi Tg - Laminator T - Staggered (Diagonal) PTH-PTH

5) Recent CAF test results for "new" versus high Tg FR-4 laminate material; InLine PTHs: (See Figure 9.)

– A2 shows equivalent brittle nature of the new (*) laminate material

– A3 shows presence of "readily conductive region" around PTHs

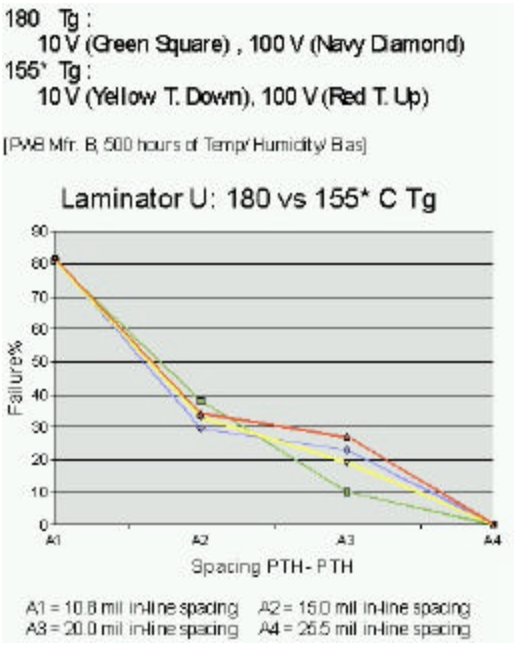

Figure 9 – New vs. Hi Tg – Laminator U – InLine PTH-PTH

6) Recent CAF test results for "new" versus high Tg FR-4 laminate material; Staggered PTHs: (See Figure 10.)

– B1 and B2 show presence of "readily conductive region" around PTHs

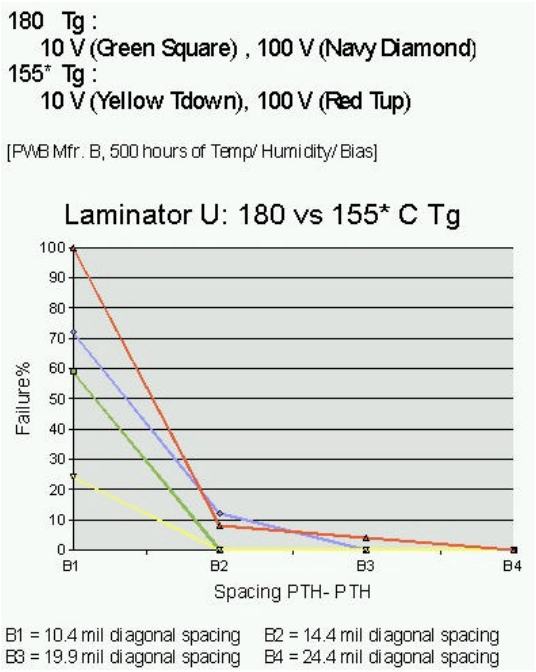

Figure 10 – New vs. Hi Tg – Laminator U – Staggered PTH-PTH

7) Recent CAF test results for experienced versus in-experienced "CAF-Resistant" laminate material user; InLine PTHs: (See figure 11.)

Shows poor new material qualification by PWB manufacturer B affecting CAF results.

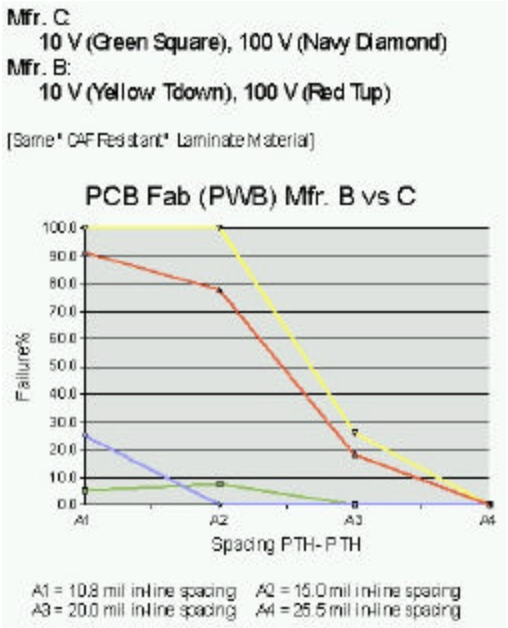

Figure 11 – Inexperienced vs. Experienced PWB Mfr. – CAF-R Laminate – InLine PTH-PTH

8) Recent CAF test results for high Tg versus "CAF-Resistant" laminate at same in-experienced CAF laminate material user; Staggered PTHs: (See Figure 12.)

– B1 shows similar brittle nature of "CAF-Resistant" and this Hi-Tg FR-4 laminate
– B2 shows better CAF resistance for the "CAF-Resistant" laminate at larger spacing

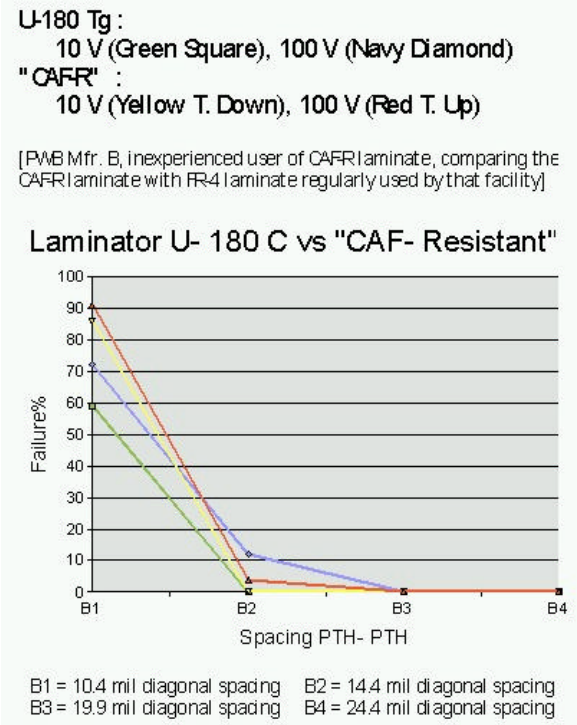

Figure 12 – Hi Tg Laminator U vs. CAF-R Laminator – PWB Mfr. B – Staggered PTH-PTH

Summary and Conclusions

Standard Tg (glass transition temperature) FR-4 laminate materials generally appear to show more resistance to CAF than high Tg standard FR-4 laminate materials. Therefore when high Tg laminate is specified (common on thicker boards) the minimum design requirements based upon maximum voltage differentials may need the spacing design requirements increased further to avoid increased risk of CAF failure.

Reducing the extent of the readily conductive region (D) around plated-through holes should be a key focus of attention by laminators and printed wiring board manufacturers. Several laminators have done a good job of improving the CAF resistance of their laminates if drilled and processed properly, but printed wiring board manufacturers may also need to make certain process improvements in order to realize the full benefit of using more CAF-resistant laminate materials.

The CAF test method used does produce repeatable results, which support the CALCE model for CAF failures. The consistency of CAF testing results using this procedure might be improved by evaluating use of a lower standard current limiting resistor value, alternate board finishes, and/or other parameters of the CAF test procedure. This could be one of the goals for a proposed Round Robin using this CAF test board.

A reliable CAF test method should allow, after additional Round Robin testing (evaluating the effect of overall board thickness, different glass styles, dielectric thickness between layers, various drilling parameters including hole size, permanganate versus plasma desmear, and glass etch versus no glass etch, etc.), developing an industry standard for the CAF resistance of finished printed wiring boards.

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Matsushita	Merix
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Nelco	NPL-UK
Polyclad	Sanmina-SCI
Tyco	Yamamoto

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