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Embedded Ceramic Resistors and Capacitors in PWB- Process and Design

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Summary
Design and processing of ceramic resistors and capacitors fired onto copper foil and embedded into FR4 circuit boards are presented and discussed. Evolution of design guidelines and processing for embedded ceramics is presented and discussed. Design tolerances are slightly larger for embedded ceramics because of the extra firing at high temperatures experienced by the copper foil on which the resistors and capacitors are printed. Scaling of the resistor and capacitor terminations must be done during print-and – etch operations.

Ceramic bodies are weak in tension and very strong in compression, so the most important processing precaution is to minimize tension experienced by the resistors during high temperature firing and lamination. Somewhat reduced lamination pressures is helpful. Limiting the size of resistors and capacitors is also helpful for capacitors. Size of resistors is usually not a problem except for very small resistors below 10 mils in size Designs for these applications include specially formulated pastes with thermal expansion behavior higher than is optimum for ceramic resistors and capacitors on alumina substrates. In addition, protection of the ceramic components from the stress of the lamination steps is desirable for the resistors. This is provided by encapsulating the resistors in a filled encapsulant that reduces the expansion of the epoxy resin, and scatters the laser energy applied during resistor trimming, so that the PWB itself is not harmed while being laser trimmed. Performance after processing appears excellent by usual environmental tests; and board flexure encountered in bend tests does not appear to be a problem. To date, five mil resistors appear too small to be screen printed with good CV and reliability. Ten mil and larger resistors are adequately stable.

Introduction

Design of ceramic resistors and capacitors embedded in PWB's requires adaptation of fabrication processes used on ceramic substrates.[1] Design rules used for filled polymeric resistors and capacitors on PWB's also must be adapted. Considerable effort has already gone into adapting ceramic technology to PWB as the materials characteristics of the ceramic approach became apparent. There are expansion mismatches between the copper foil and the ceramic components; there is some sensitivity of the ceramic resistors to being put in tension during high pressure lamination, and there were initial problems with adhesion of the resistors to the copper foil. This paper will describe the problems that surfaced while developing this approach to embedded passives, and approaches to solving those problems.

Thermal Expansion

Thermal expansion mismatches are due to the different rates of contraction of the ceramic components and the copper foil during the cool down from firing temperatures. Generally, distortion of the copper begins just below the glass transition temperature of resistors and capacitors fired on the foil, and the mismatch grows during cool down to room temperature. Expansion mismatches cause problems in the fabrication of PWB's with ceramic embedded passives. The copper foil is distorted and registration during lamination becomes more difficult, with design tolerances growing larger.

The solution to this problem is to develop glasses for resistors and capacitors that have higher thermal expansion coefficients. Work at embedding ceramics to date has been carried out using compositions optimized for alumina substrates. These have expansion coefficients too low for optimum design leeway on copper foil. Newer compositions will improve the performance of embedded ceramics.

Existing compositions can fortunately be used successfully if proper size and design tolerances are permitted. Figure 1 shows tolerances we have found that allow successful design using currently available capacitor compositions. The physical size of components, especially capacitors, affects their ability to be embedded in PWBs. Resistors and capacitors both should be kept below about 1 cm (400 mils) on a side to minimize foil distortion. Larger capacitors and resistors are made by joining an array of smaller ones, leaving spaces in between for strain relief for the copper foil. Figure 1 illustrates typical clearances for successful capacitor design.

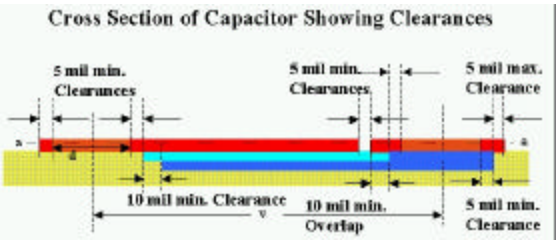

Figure 1 - Capacitor Tolerances Illustrated

Brittleness of Ceramics

The brittleness of ceramics in tension is well known. In early work with embedded ceramics, this property of ceramics surfaced as cracks in resistors, resulting in high resistance values and unstable resistance under stress. These defects occur during the lamination process, both when inner layers are produced, and when multilayer boards are laminated.

Several material innovations and process steps minimize this problem. Design of PWBs with long, wide runners inline with terminations causes reliability to suffer. Redesign using shorter, narrower runners that are not inline with the resistor terminations improves resistor reliability. It has also been found that 5 mil wide resistors are significantly less reliable, using current materials, than wider ones. Also, reliability suffers somewhat in resistors that are very large—over 500 mils in length. This may be due to the previously mentioned expansion mismatch with current materials.

Currently, an epoxy encapsulant that is screen printed over the resistors and cured before each lamination step is used. This is the most significant process step taken to date to protect resistors from damage during lamination. Best results are obtained when the encapsulant is printed over an area that is significantly larger than the resistors. A further advantage of the encapsulant approach is the ability to fill the encapsulant with an inorganic filler to enhance thermal dissipation or to dissipate laser energy applied during trimming of resistors, in order to prevent substrate damage. Currently under investigation is the use of higher Tg encapsulants to enhance protection of resistors during lamination. Figure 2 shows a resistor coupon in a test vehicle inner layer that has a filled encapsulant printed as backing for the resistors.

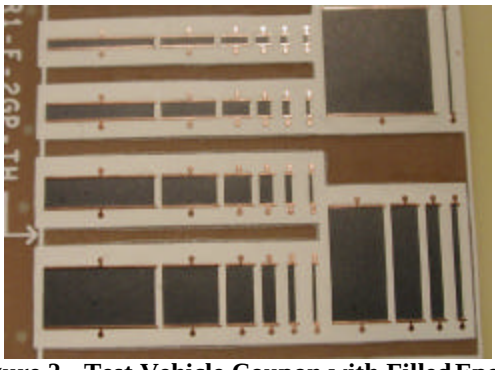

Figure 2 - Test Vehicle Coupon with Filled Epoxy Backing

Figure 3 shows an as-printed (before firing) view of a capacitor test vehicle foil. The capacitors on this foil are designed with adequate clearance and size for firing and laminating into PWB board.

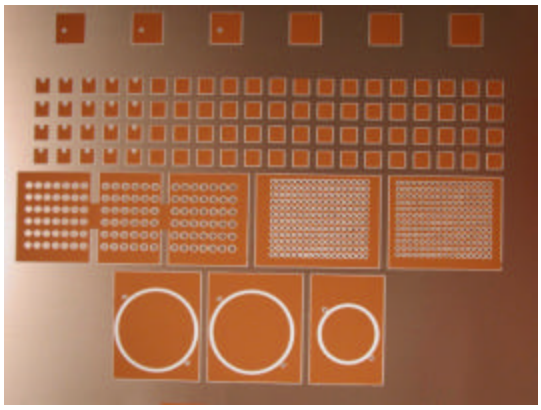

Figure 3 - Capacitor Test Vehicle Foil

The encapsulants permit fabrication of highly reliable resistors using thin cores. Currently, 5 mil thick inner layers are being fabricated with highly reliable resistors resulting. Before using the encapsulant protective layers, inner layers needed to be 8 to 12 mils thick minimum to produce reliable resistors. While 5 mils is not considered a minimum thickness for cores, this facility currently has no experience with inner layers thinner than 5 mils.

Resistor Properties

Table 1 summarizes the resistors' performance. Currently used materials/process give about 99.9% yield of good resistors when optimum materials, design and processing are used. Further improvements on the horizon will provide higher reliability and yields

Table 1 - Typical Resistor Properties

R (Ω/s)	TCR Hot/Cold (ppm)	Solder Dip Test 290 °C	Therm Cycle® (1100 X)	Flex Test (100 X) 36" Rad.
10	80/140	< 1%	~1%	< 0.05%
100	-50/50	< 1%	~0.5%	< 0.05%
1K	50/40	< 1%	~0.5%	< 0.25%
0K	-130/-170	< 1%	~0.5%	< 0.5%

Figure 4 shows the resistance variation of one coupon of a test vehicle with resistor size.

The coupon was printed with 100 ohms/square resistor material The high CV at 10 mils indicates the smaller size relative to screen mesh that results in less precision in depositing paste. An array of 50 or 70 mil resistors of uniform size in a single test vehicle coupon gives a CV of under 3%.

Extensive data is available on resistance and resistor performance over the range of 10 ohms to 10,000 ohms. Tolerances are about equal over the complete range.

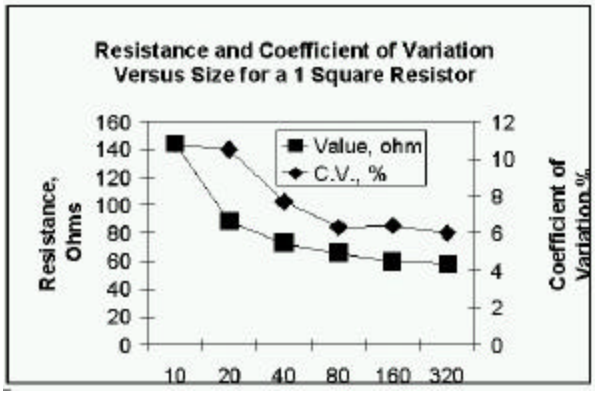

Figure 4 - R and CV vs. Resistor Size

Capacitor Properties

The capacitors exhibit X7R type performance characteristic. Capacitance of about 0.5 microfarad/sq. in. is easily achieved with a two layer structure. Table 2 summarizes the capacitors' performance in PWBs. Figure 3 is a photo of a capacitor test vehicle foil before firing.

Table 2 - Typical Properties of Ceramic Embedded Capacitors

Capacitor Type:	1 Layer	2 Layer
Capacitance Density	250 nF/in^2	500 nF/in^2
Loss Tangent	1-2%	2-3%
TCC	X7R	X7R

Laser Trimming

Laser trimming of resistors can be performed, just as on ceramic substrates. A light absorbent encapsulant to protect the substrate from damage inflicted by the laser during trimming is necessary. Tolerances of 1 to 2% have been achieved in tests of these materials' ability to be trimmed Table 3 summarizes laser trim data taken from the range of resistance from 10 ohms/sq material to 10Kohm/sq material.

Table 3 - Laser Trim Test Results[2]

Resistor Grade	Pre-trimmed Average	Pre-trimmed 3σ	Post-trimmed Average	Post-trimmed 3σ
10Ω/Sq	23.2 Ω	11.6%	30.3 Ω	2.4%
100Ω/Sq	279.2 Ω	12.7%	404.3 Ω	0.3%
1KΩ/Sq	2,210 Ω	13%	3,016 Ω	2.1%
10KΩ/Sq	25,267 Ω	15%	41,570 Ω	1.6%

Resistor Size Limitations and Tolerances

The minimum line width that may be reliably printed using a screen is 5 mils. To produce a resistor of adequately precise width, a practical minimum is 10 mils. One of the characteristics of ceramic thick film is the size reduction between the printed and fired patterns. Typically, a resistor will lose about 1 mil on each side. Additionally we have experienced about 1 mil of undercut in the line width of the etched terminations. This means that a 10 mil wide resistor with 10 mil termination edge spacing will process out to a 8 mil wide, 12 mil long resistor. This will effectively increase the aspect ratio from 1.0 to 1.5. Because it is a fixed reduction, rather that a proportional one, the effect is smaller in larger resistors. Figure IV illustrates this effect in untrimmed resistors with a design aspect ratio of 1:1.

Notice that the effect is most pronounced in resistors less than 20 mils wide. Another factor limiting the minimum resistor size is the initial tolerances. In order to minimize the amount of trim necessary, it is desirable to have the pre-trimmed mean resistor value about 70 to 75% of nominal. This will insure that 99+% of the resistors will have pre-trimmed values lower than nominal. To achieve this goal it is recommended that 20 mils be the minimum fired width of any resistor, though 40 mils will produce significantly lower pre-trimmed tolerance. Choice of size will ultimately be determined by power dissipation and board space requirements.

Board Stack Up /Design File Considerations

Embedded passives will typically be placed on at least 1 of the inner layers of a PWB. Because of impedance considerations, the components and signal lines will typically reside adjacent to a ground plane with clearances for through vias and routing spaces. For ease of processing we recommend that the foil layer(s) containing the passives be paired with such a ground plane as a core or subassembly. Because the components (Resistors, Dielectric/Screen printed Electrodes) reside on the foil, this foil is considered to be the metal layer, and is counted as such in the stack up. In addition to all of the other metal layers and other data, the design file for the board will contain this layer plus all of the layers required to produce the films to make screens for printing the thick film pastes. In addition, some of these layers may be scratch files.

Acknowledgements

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Reference

1. W.J. Borland and S. Ferguson, CircuiTree, March 2001.
2. Table 3 - Courtesy ESI, Inc.