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# Embedded Mezzanine Capacitor Technology for Printed Wiring Boards

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**Abstract**
A novel technology for embedding discrete capacitors in a mezzanine layer of an HDI PWB was developed and implemented by Motorola in partnership with its PWB supply chain. The technology is based on the use of a ceramic-filled positive type photo-dielectric to form discrete, embedded capacitors with capacitance densities ranging from 10 to 30 pF/mm$^2$. Capacitor test vehicles were designed, fabricated at multiple sites, tested, and used to characterize the electrical performance and reliability of embedded mezzanine capacitor structures.

In this paper, the novel ceramic-filled dielectric capacitor fabrication process is outlined. Electrical tests are reviewed, indicating a relative dielectric constant greater than 20, a loss tangent of less than 4%, and breakdown voltages in excess of 100V for 11µm thick dielectrics. For reliability testing, minor variation in capacitance is observable following multiple reflow cycles, liquid-to-liquid thermal shock, or air-to-air thermal cycling. A larger shift in capacitance is observed following temperature-humidity storage, but the change is shown to be reversible. Finally, two case studies are presented for RF modules using this embedded capacitor technology. In each case, area usage is reduced while maintaining or reducing the overall module cost.

**Introduction**
By incorporating embedded passive components (EP) into the printed wiring board, improved performance, better reliability, smaller footprint, and lower cost can be achieved. Although materials exist for embedding virtually any value of resistor in a reasonable space, current material sets severely limit the range of embeddable values for inductors and capacitors.[1] The embedded inductor limits are not of great concern since inductor counts in cost-sensitive designs are already minimized because of their relatively high cost and low-performance issues. Capacitors, on the other hand, are the predominant passive component in most designs. Typical capacitor EP materials, such as reinforced laminates and HDI resins, are limited to a capacitance density of a few picofarads per square millimeter (pF/mm$^2$), restricting the vast majority of capacitors from being embedded into the substrate.
Recently, new embedded capacitor materials utilizing ceramic fillers in polyimide or epoxy resins in thin laminate form have been developed by various parties.[1,2] Some of these materials should make embedding of 500pF capacitors possible in reasonable board areas. However, handling of thin-core laminates has also been reported as a problem by board shops processing these materials.[3] Moreover, discrete capacitor formation is difficult with these laminate materials, as one side must be etched prior to lamination, inherently creating a registration problem in the process. Thus there is a need for an embedded capacitor material with a capacitance density on the order of 10-30 pF/mm$^2$ that is capable of forming discrete embedded capacitors and that is compatible with standard printed wiring board (PWB) fabrication.

Motorola Labs, in partnership with Vantico as a materials supplier and AT&S, Ibiden, and WUS as PWB fabricators, has developed a new, easily processable ceramic-filled photodielectric (CFP) dielectric material for discrete embedded capacitors up to 450pF in areas below 30mm.[2] In the following sections, the material properties and fabrication steps are presented, test vehicles are defined, and electrical test and reliability results are discussed. Useful

device structures incorporating this material are also presented.

**Materials**

CFP is a ceramic filled, positive acting, photo-dielectric that has its composition engineered for optimal electrical performance at high frequencies and robust processing. The ceramic filler is highly purified, and particle size is carefully controlled. The salient mechanical properties are shown in Table 1, and the electrical properties as measured by the manufacturer on the dielectric itself (not capacitor structures) are shown in Table 2.

**Table 1 – CFP Mechanical Properties**

| Test | Unit | Result |
|---|---|---|
| $T_g$/TMA | ºC | 110 |
| Elongation Rt | % | 0.59 |
| E module Rt | Mpa | 8019 |
| S-Breake Rt | Mpa | 51.24 |
| Elongation 80ºC | Mpa | 0.86 |
| E module 80ºC | Mpa | 69.25 |
| s-Breake 80ºC | Mpa | 44.27 |

**Table 2 – CFP Dielectric Properties (Material)**

| Test | Unit | Result |
|---|---|---|
| Dk | # | 25.9 |
| Dk (after 24h/$H_2O$/23ºC) | # | 28.8 |
| Dk (after 48h/$H_2O$/50ºC) | # | 30.9 |
| Df or tan δ | % | 1 |
| Df (after 24h/$H_2O$/23ºC) | % | 5.1 |
| Df (after 24h/$H_2O$/50ºC) | % | 5.1 |
| Volume resistivity | Ω·cm | $4.5 \cdot 10^{13}$ |
| Surface resisitance | Ω | $3.3 \cdot 10^{14}$ |
| Dielectric strength | kV/mm | 71.8 |
| Insulation resistance | Ω | $1.50 \cdot 10^{9}$ |
| E-Corrosion | | Not visible |

**Fabrication Process**

The CFP dielectric is designed to be coated onto a substrate at the board shop using typical board fabrication techniques. The material is coated onto a copper plane using standard coating techniques such as curtain coating or vertical roller coating. The material is dried at 60ºC for 30 minutes, and then a sheet of copper, typically 3/8 oz. or thinner, is laminated onto the CFP dielectric layer. A typical foil lamination profile is shown in Figure 1. Figure 2(a) shows a copper clad laminate with CFP dielectric coated on both sides along with the laminated mezzanine copper sheets. At this point, the mezzanine copper layer is printed and etched, leaving the pattern of the top capacitor electrodes, as shown in Figure 2(b).

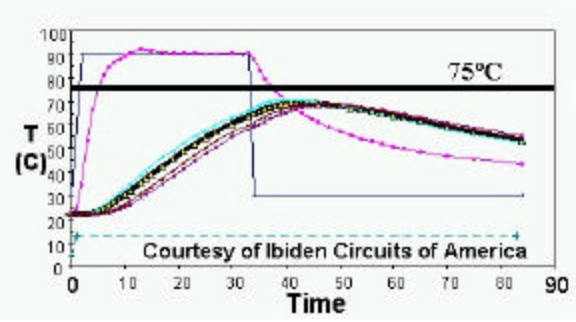



**Figure 1 - CFP Lamination Profile**

Following the mezzanine electrode definition, the CFP material is exposed with UV energy, using the mezzanine copper electrode as a mask. The material is then heat bumped. Afterwards, the CFP dielectric is developed using gamma butyrolactone (GBL), leaving the structure that appears in Figure 2(c). At this point, a final cure for the dielectric is conducted, completing the embedded capacitor process.

Now, the inner layer, *i.e.*, the bottom electrode, must be patterned. This step is accomplished with a standard print & etch step utilizing vacuum lamination of the dry film. A minimum overlap from top capacitor plate to bottom capacitor plate must be specified to allow proper tenting of the dry film over the capacitor stack; otherwise, the capacitor structure would be severely undercut during the subsequent etch step. The capacitor structure following this step is depicted in Figure 2(d).

At this point, the substrate undergoes the typical HDI process flow, resulting in a completely buried structure, hence the name "mezzanine" capacitors, as they are constructed on what becomes a "mezzanine" level. Connection to the bottom plate, whether shared or discrete, may be made through a plated through hole (PTH) or microvia (μvia) to the lower plate level. Connection to the upper capacitor plate is achieved through a μvia connection to the mezzanine level. A depiction of the finished structure is shown in Figure 2(e). A microscope photo of a finished CapTV-1 section, showing a mezzanine capacitor with a μvia connection, appears in Figure 3.

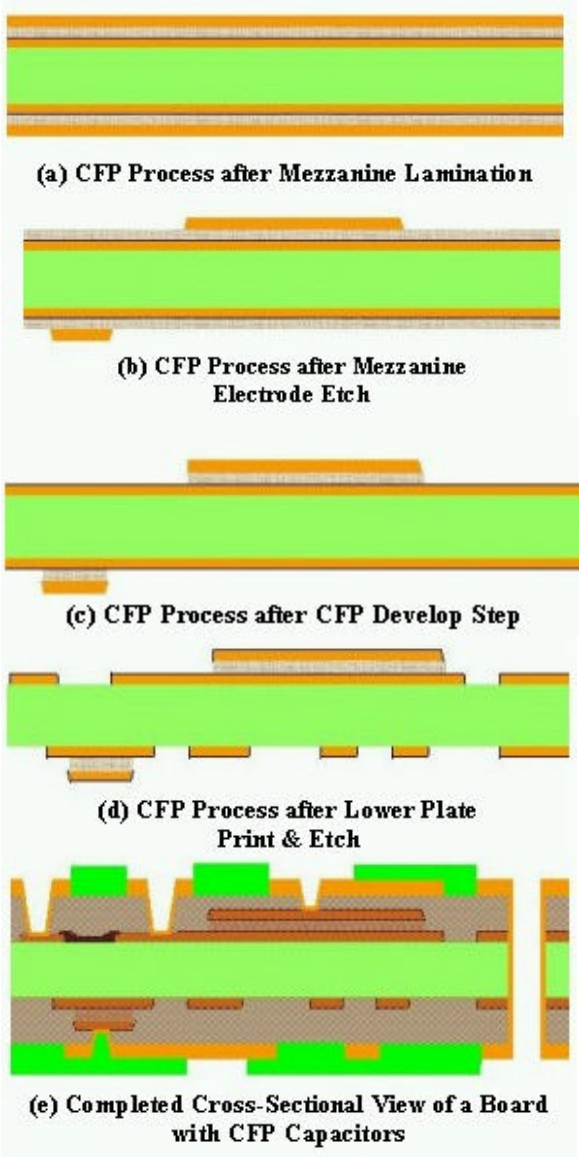



**Figure 2 – CFP Dielectric Fabrication Process**

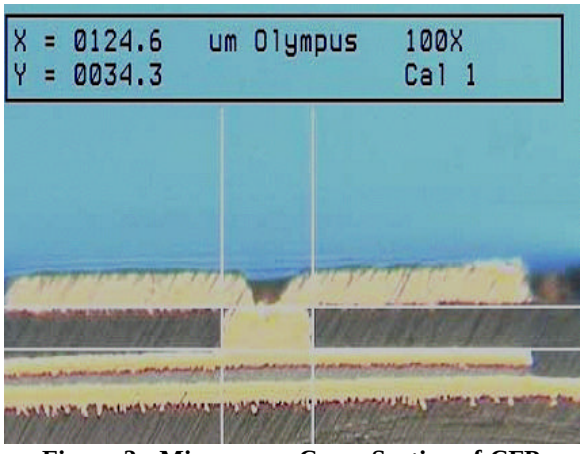



**Figure 3 - Microscope Cross Section of CFP Capacitor with Mezzanine µvia Contact**

**Test Vehicles**

Two test vehicles were constructed to test the fabrication process capability, qualify the board shop partners, measure the electrical properties of fabricated capacitors, and gauge the reliability of the embedded devices under typical environmental tests. The first test vehicle, CapTV-1, is shown in Figure 4, with inner layer design files and a picture of the finished test coupon.

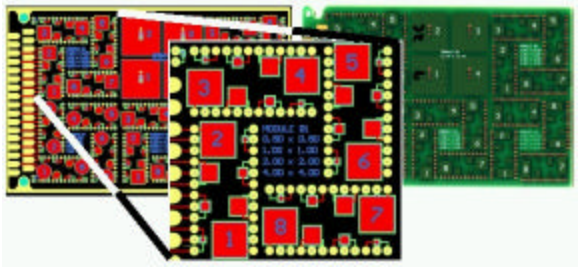


**Figure 4 – Layout Drawings and Photo of Cap TV-1 Design**

The first test vehicle included permutations on both size and shape of the capacitors, as summarized in Table 3. The areas of the circles were generated to be the same as that of the squares, but the rectangles were formed to have the same perimeter as the squares, although with less area. These modifications were made in an attempt to quantify the degree of variation related to fringe effects. In addition, CapTV-1 also incorporated an HDI capacitor directly above each CFP capacitor.

**Table 3 – CapTV-1 Geometries and Sizes**
**(all dimensions in mm)**

| Size\Shape | Square | Circle (diameter) | Rectangle |
|---|---|---|---|
| **S** | 0.5X0.5 | 0.56 | 0.33X0.67 |
| **M** | 1X1 | 1.13 | 0.67X1.33 |
| **L** | 2X2 | 2.26 | 1.33X2.67 |
| **XL** | 4X4 | 4.51 | 2.67X5.33 |

A drawback associated with CapTV-1 was the connection scheme to the three-capacitor plates. As can be seen in Figure 5, each capacitor location has three test points associated with it, providing one connection each to the inner layer plate, the mezzanine plate, and the HDI plate. The mezzanine connection trace from the plate out to the test point also had CFP and bottom layer conductor beneath it due to the fabrication process. In effect, the capacitor was extended out along the trace. For the larger capacitor structures, the built-in error from the connection was small. However, the smallest capacitors were dominated by the capacitance associated with the connection trace. Additional test structures were placed on the coupons that approximated the extra capacitance of the trace in order to subtract the trace capacitance from the

measurements for correction. The connection scheme in CapTV-1 was definitely a problem for measurement accuracy and de-embedding the properties of the capacitor alone.

To resolve the connection issue and reconfigure the sizes of the various geometry capacitors, a second test vehicle was created, CapTV-2, as depicted in Figure 5. The range of areas was expanded on both the low and high ends, as shown in Table 4. Moreover, connections to the capacitor plates were made by direct µvias. Any traces required to preserve the test point separation for the fixed probe pitch were run above the mezzanine plates. No HDI capacitors were included on this test vehicle.

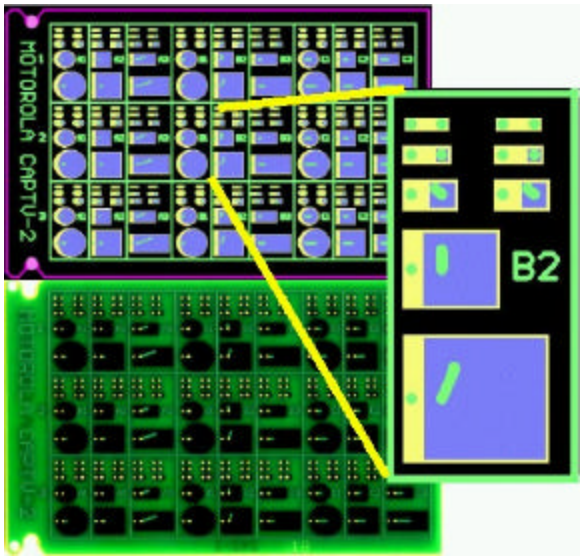



**Figure 5 – Layout Drawings and Photo of CapTV-2 Design**

**Table 4 – CapTV-2 Geometries and Sizes**
**(all dimensions in mm)**

| Size\Shape | Square | Circle (diameter) | Rectangle |
|---|---|---|---|
| **XS** | 0.3X0.3 | 0.34 | 0.21X0.42 |
| **S** | 0.5X0.5 | 0.56 | 0.35X0.71 |
| **M** | 1X1 | 1.12 | 0.71X1.41 |
| **L** | 3X3 | 3.38 | 2.12X4.24 |
| **XL** | 5X5 | 5.64 | 3.54X7.08 |

**Electrical Tests**

High frequency measurements to 1.8GHz were conducted using an HP4192A Impedance Analyzer, a Signatone probe station, and Cascade Microtech fixed-pitch compliant GS-1250 probe. In the cases where higher frequency measurements were needed, an HP8753C Vector Network Analyzer was used to measure $S_{11}$ out to 3GHz, and the reflection coefficient was then converted to impedance (or capacitance) for direct comparison with the HP4192A results.

Perhaps the most important parameter for a high-K capacitor dielectric is capacitance density, or capacitance per unit area, C/A. This parameter combines the two major effects of dielectric thickness and relative dielectric constant into one measure. A plot containing capacitance vs. area data from a 16µm dielectric CapTV-1 samples and 11µm CapTV-2 samples is shown in Figure 6. Data in this figure is shown at 10MHz. Note that in this figure, the responses fit well to a linear model with minimal spread in the data. In fact, standard deviations are 7% in the worst cases. The slope of the lines indicates the capacitance density, which is 16.8pF/mm$^2$ ($D_k$=21.0) for the 11µm dielectric.

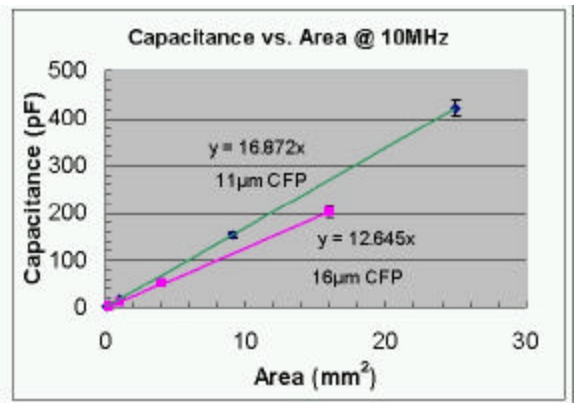



**Figure 6 – Capacitance vs. Area**

In Figure 7, the capacitance vs. frequency response is shown for a variety of sizes of capacitors from CapTV-2. Note that the roll-off at higher frequencies is a characteristic response with larger sizes, as inductance of the plates becomes appreciable more quickly. Note that the lower values of capacitance are relatively stable, even out to the 3GHz range. No evidence of self-resonance behavior is observed out to this frequency. (Note: the CapTV-2 design minimizes parasitic inductances and capacitances for the design.)

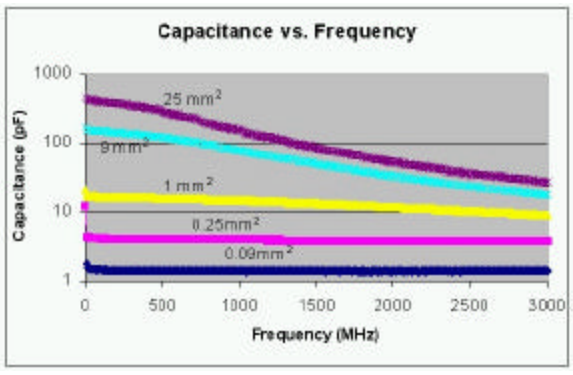



**Figure 7 – Capacitance vs. Frequency**

The relative dielectric constant, $D_k$, is plotted versus frequency in Figure 8. Rolloff at higher frequencies is expected, as polarization of the dielectric material

becomes less effective at higher oscillation rate. It should be noted that only the linear portion of the capacitance vs. area curve was used at each frequency to discriminate against rolloff errors associated with larger area capacitors.

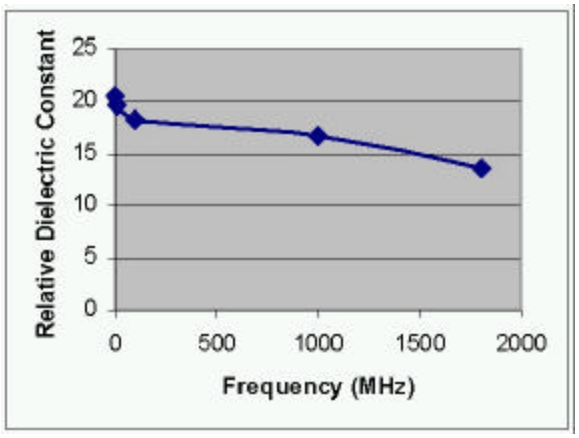



**Figure 8 – $D_k$ vs. Frequency**

A representative plot of loss tangent, tan δ or $D_f$, is shown in Figure 9. This chart is a line graph of 640 samples, ranked in increasing size, over several frequencies. On average, the loss tangent is 3-4%, which is relatively high for capacitors, but is unavoidable due to the epoxy resin base of the material. The increase in loss for the larger devices at higher frequencies is related to the onset of self-resonance, a problem that was generated by the CapTV-1 design, from which this data is taken. Other sources have also confirmed loss tangents for CFP on the order of 2% to 4% based on a variety of measurements.

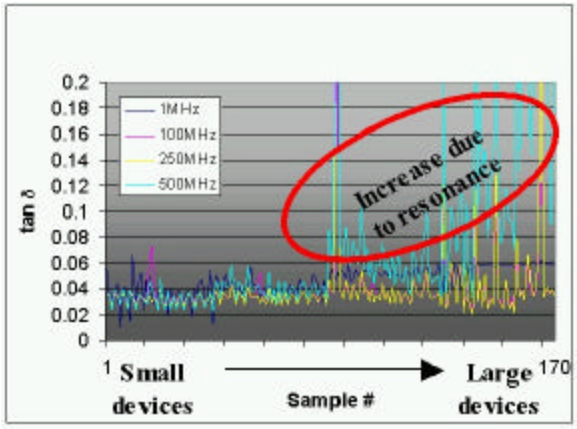



**Figure 9 – CFP Loss Tangent at Various Frequencies**

Another critical parameter for capacitor dielectrics is breakdown voltage and leakage current. Breakdown voltage measurements were conducted with an Agilent 4155B Semiconductor parameter analyzer, stepping voltage at 0.5V increments and holding for 1 sec at each step. The results for leakage current measurements on the 11µm CFP capacitors are shown with a logarithmic y-scale in Figure 10. Although the fit curve appears to be power-law, it is actually a linear equation plotted on the logarithmic axis. No sign of breakdown was observed.

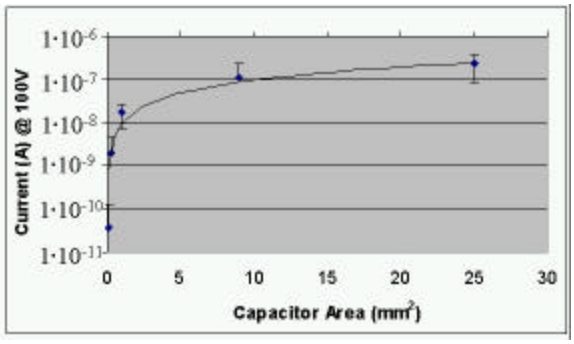



**Figure 10 – Capacitor Leakage Current vs. Area**

Although properties of CFP do not rival that of most SMT parts, a wide variety of applications can be served by this material. The relatively high dielectric constant of the material allows for embedding of capacitors as large as 450pF in areas below 30mm$^2$. The high loss tangent prevents the material from being used in some filtering applications, but still is available for use in many slow roll-off filter applications. Its high breakdown voltage (>100V @ 11µm) also indicates a robust material electrically. The next section will deal with the mechanical robustness of the CFP dielectric.

**Reliability Tests**

Embedded components are of little value unless they can survive the same rigors of testing that modules or boards would receive. To demonstrate reliability, the following tests were conducted:

1) 5X reflow at standard profiles
2) 5X reflow + 1000 cycles of liquid-to-liquid thermal shock (LLTS), -55ºC to 125ºC
3) 5X reflow + 1000 cycles of air-to-air thermal cycling (AATC), -55ºC to 125ºC
4) 5X reflow + 250 hours 85ºC/85% relative humidity storage
5) Limited bend testing (165,000 cycles)

The first stage of testing dealt with the material's response to 5X reflow. Six CapTV-1 coupons were processed for this test, and all mezzanine devices on the coupons were measured both before and after the reflow cycles. The results from two of the coupons appear in Figure 11, with capacitance measured at 10MHz. The other four coupons exhibit quite similar results. Net shifts post-reflow tends to be negative, but limited to about –1 to –4%. This shift can be attributed to water evacuation in the dielectric film, since materials of this nature tend to absorb water with a resulting increase in effective dielectric constant.[4]

The next phase of testing involved 1000 cycles of LLTS after the 5 reflow cycles. Here, two full coupons were utilized for this test, and all 640 devices were measured initially, post-reflow, and after the 1000 cycles, as well as a several points during the test. The reflow results are similar to those in Figure 11. The shifts after 1000 cycles LLTS appear in Figure 12. Devices tended to shift slightly positive from the state after reflow, resulting in a slight positive shift after the test completion, typically within 3% of the original value. None of the 640 devices were found to short or fail in another manner.

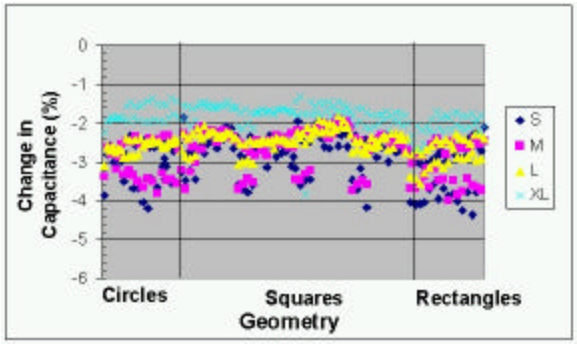



**Figure 11 – Change in CFP Capacitors Following 5X Reflow**

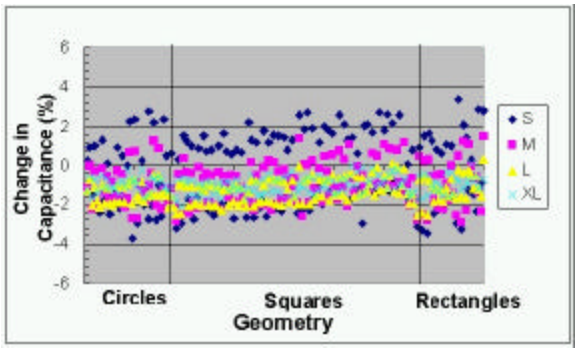



**Figure 12 – Change in CFP Capacitors Following 5X Reflow and 1000 Cycles LLTS**

The third phase of testing was to subject the 5X reflowed parts to 1000 cycles AATC. Test methodology was similar to that of the LLTS testing. Results post-reflow are again similar to the data in Figure 11. The results after the 1000 AATC cycles appear in Figure 13. Although the pattern is slightly more diffuse than for the LLTS samples, the overall variation is not quite as large a positive shift—still very encouraging results. Three devices out of the 640 tested samples did fail, but the problem was related to HDI processing rather than the CFP material.

The fourth test performed on the devices was 250 hours of humidity storage in 85ºC and 85% relative humidity. Values after 5X reflow are again similar to those in Figure 11. Results after 250 hours of storage appear in Figure 14. Again, the measurement frequency was 10MHz. A larger distribution is observed relative to the LLTS and AATC data, and a clear pattern based on size is also observed. The data suggests a relatively small change in capacitance for smaller devices as compared to other tests, while the larger devices shift in the positive direction to +5-7%. Water absorption obviously has a strong effect on the capacitance. The relatively small change of the smaller samples may be due to an artifact of measurement, with the water being released from the small capacitor structures prior to measurement, whereas water was trapped under the larger capacitor plate structures. Subsequent drying experiments indicate that samples baked at 110ºC after exposure will return to their initial dry values of capacitance, demonstrating that the excursions due to humidity storage are not a true failure mode.

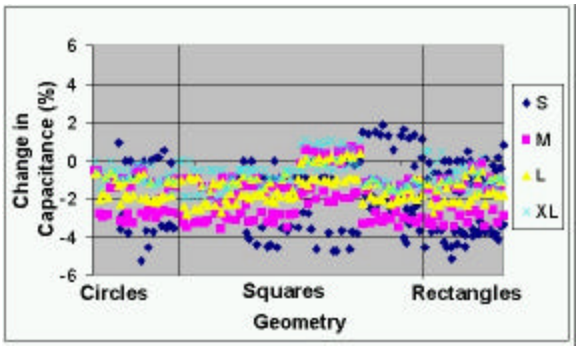



**Figure 13 – Change in CFP Capacitors Following 5X Reflow and 1000 Cycles AATC**

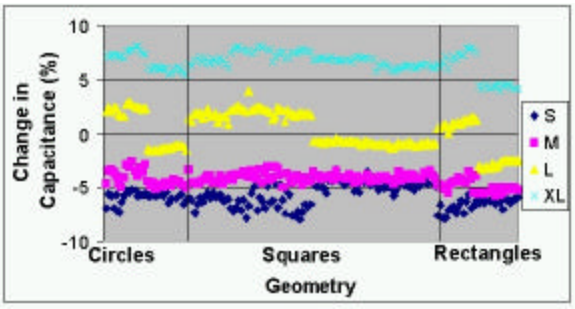



**Figure 14 - Change in CFP Capacitors Following 5X Reflow and 250 Hours 85ºC/85%RH Storage**

Additionally, some limited bend fatigue testing was conducted on a sample coupon from CapTV-1. A 1 $in^2$ sample was drilled with support points in an equilateral triangle arrangement (see inset, Figure 15). A force of 15N was applied and released at the center of the equilateral support triangle. After 165,000 cycles, no statistical change in capacitance was observed, as is shown in Figure 15. Although this test is not sufficient to solidly indicate mechanical strength of the material, it does suggest the fundamental mechanical capability of the material.

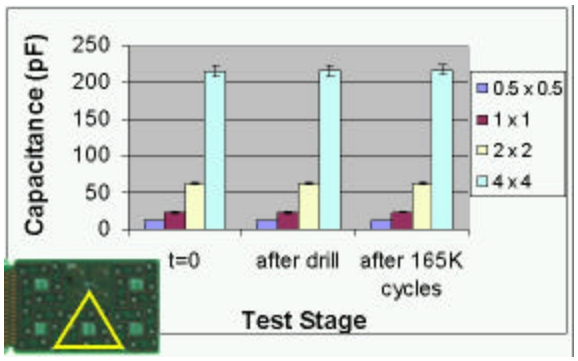



**Figure 15 – Capacitance Change Following Bend Testing; Inset Shows Support Points**

Overall, CFP has proven to perform acceptably through reliability testing, with the greatest concern being humidity storage. Even though shifts are relatively high after this test, approaching 10% for some geometries and areas, the effects are reversible with simple drying, indicating that the effect is a water absorption phenomena, as is typically reported of this type of material in literature,[4] rather than a defect-driven mechanism.

**CFP in RF Modules**

CFP dielectric has been shown above to perform adequately from both electrical and mechanical standpoints for many capacitor applications. Although much of the conventional wisdom in the industry is that embedded capacitance is only beneficial for power-ground decoupling applications, Motorola has taken a lead in discrete embedded passives by utilizing CFP in RF modules.

One such RF module is depicted in Figure 16. In this case, the module is a re-designed part from an all-SMT design. The new design incorporated 18 CFP capacitors along with 11 embedded resistors and 4 embedded inductors, leaving 56 placed passives and 11 other placed parts. The revised design occupied 43% less space than its SMT version. Initial modules performed their intended function with only slight surface part value tweaks on the first pass, with some performance metrics better than the original SMT design.

The goal for the module in Figure 16 was to decrease surface area occupied by the module as much as possible, increasing functionality within a given area. Other EP design scenarios are possible, such as the cost-conscious design evaluation presented in Figure 17. Here, another RF module is evaluated, with layout, comparing an all-SMT design, a design using only embedded resistors and HDI-based capacitors, then a design also utilizing CFP capacitors. The SMT design occupies 93mm$^2$ and has 32 surface mount parts. Converting to an embedded design limited to embedded resistors, parallel plate capacitors using the HDI dielectric, and embedded spiral inductors results in a module with only 21 SMT parts, occupying only 63 mm$^2$ (a 32% reduction in size). Substrate cost is increased substantially, since the design is converted to HDI and additional EP process are used, but the overall module cost including BOM and assembly cost is marginally reduced. In this example, the size effectively reduced, but cost is left basically unchanged.

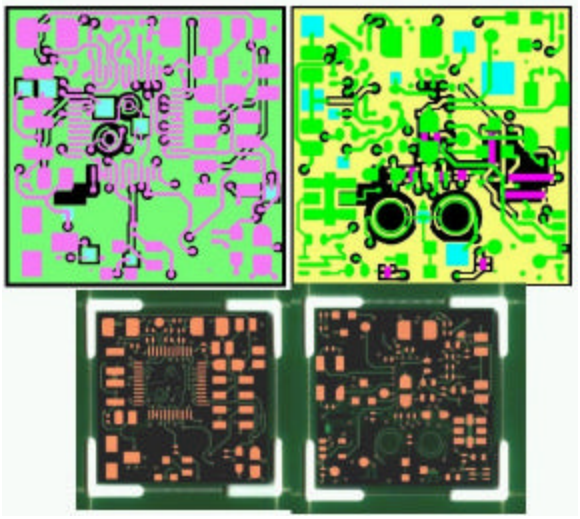


**Figure 16: Layout & Photos of a RF Module Incorporating CFP Capacitors**

The rightmost column of Figure 17 evaluates the same module when allowing embedded resistors, inductors, and CFP capacitors. Area usage is further reduced to 52.3 mm$^2$, a further 17% reduction from the HDI design, and a 44% area reduction compared to the SMT design. The embedded part count increases to 20, leaving only 12 parts on the surface. Board cost is further increased due to the additional processes related to CFP capacitor fabrication. However, since so many parts are now embedded, a substantial conversion cost is saved, resulting in a 12% reduction in cost from the HDI design and a 13.7% reduction in cost compared to the SMT design.

Utilizing CFP capacitors for the RF module in Figure 17 allowed for a tremendous area reduction while concomitantly reducing the cost of the system, despite increasing the net cost of the board itself. Such evaluation is essential for determining products that will benefit from embedding capacitors with CFP.

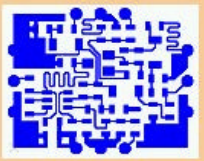
| Technology | | | All-SMT | R & HDI C | R & CFP |
|---|---|---|---|---|---|
| Number of component | SMD | R | 9 | 0 | 0 |
| | | L | 4 | 3 | 4 |
| | | C | 14 | 13 | 3 |
| | | Tr, D | 5 | 5 | 5 |
| | Embedded | R | 0 | 9 | 9 |
| | | L | 0 | 1 | 0 |
| | | C | 0 | 1 | 11 |
| | Total | | 32 | 32 | 32 |
| Ratio of Embedded component | | | 0% | 34.4% | 62.5% |
| Unit Size | | Dimensions | 8.7x10.7mm | 7.0x9.0mm | 6.3x8.3mm |
| | | Layout |  |  |  |
| | | Area | 148 | 100 | 83 |
| Unit Cost | | Substrate | 33 | 100 | 110 |
| | | BOM | 106 | 100 | 92 |
| | | Assy | 124 | 100 | 67 |
| | | Total | 102 | 100 | 88 |

**Figure 17 – Comparison of All-SMT, HDI Capacitor, and CFP Capacitor Solutions for a Specific RF Module (Embedded Resistors Also Included)**

**Conclusions**

Motorola Labs and its supply chain partners have introduced a new type of embedded capacitor dielectric based upon a high-K, positive-acting photo dielectric. This material allows for the formation of self-aligned, embedded, "mezzanine" capacitor structures that do not occupy area on the top surface of a board, allowing non-sensitive traces to be run above the embedded parts.

Electrical properties, although not sufficient to replace all SMT chip capacitors, are adequate for many applications, including bypassing, some filtering, and DC-blocking applications, among others. Reliability studies have shown the material to be robust even under harsh temperature swing tests. The largest capacitance changes occur with humidity, but these shifts are reversible.

RF modules have been developed utilizing the new CFP material, with performance exceeding that of SMT designs in some cases. Total system or module cost can also be reduced using the material, although the board cost will increase due to the added materials and processing of the board. The fabrication process is compatible with standard PWB processes, and boards containing CFP capacitors are easily fabricated at world-class board shops.

**References**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