Presented at IPC Printed Circuits Expo® 2002
www.ipcprintedcircuitexpo.org

Embedded Passives Technology Implementation in RF Applications

John Savic, Robert T. Croswell, Aroon Tungare, Greg Dunn,
Tom Tang, Robert Lempkowski, Max Zhang and Tien Lee
Motorola
Schaumburg, IL

Abstract
Motorola has developed a suite of technologies for embedding resistors, inductors, and capacitors in HDI printed wiring boards. This paper describes the technology and presents a case study demonstrating the performance trade-offs and design considerations that must be taken into account when embedding passive components into HDI PWB substrates. Furthermore, the benefit of embedded passives technology in adding "value" to the PWB, and in driving down size, cost, and part count for the OEM is illustrated.

Introduction
The development of the Embedded Passives (EP) technology was driven by the OEM need to decrease part count and board size, increase board functionality and lower overall product costs. Passive parts represent a significant portion of the total number of components used in electronic devices with resistors and capacitors making up the bulk. Historically, a typical GSM phone contained in excess of 500 passive parts that occupied half the board surface area and represented 25% of the solder joints. The EP technology described in this paper focuses on identifying non-critical resistors, capacitors, and inductors and embedding as many as possible into the HDI-PWB.

This paper briefly describes the EP technology capabilities and the manufacturing process. The primary focus of the paper is to highlight the performance trade-offs and design considerations that must be taken into account when integrating EP structures into HDI-PWB's. Furthermore, a case study for the design and manufacture of an RF module for use in a handheld phone is presented in order to demonstrate the "value" EP technology provides to the OEM by driving down the size, part count and cost.

EP Technology
There were three major objectives for the development of the EP technology. The first objective was to develop a technology capable of embedding at least 30-50% of the passive components currently used in wireless and portable products. The EP technology developed at Motorola initially focused on improving methods for embedding polymer thick film (PTF) resistors and understanding the limitations of using the HDI dielectric (RCC or photo-via) for creating simple parallel plate capacitors and 2.5-turn multi-layer inductors. Subsequently, it focused on developing new high permittivity materials for embedding higher value discrete capacitors.

The second objective was to make the technology compatible (drop-in) with conventional and HDI-PWB manufacturing processes and equipment in order to minimize capital investment and to expedite the development of a supply base. PTF resistors, HDI dielectric parallel plate capacitors, and inductors all rely on equipment available at most HDI PWB fabricators. High permittivity ceramic filled photo-dielectric (CFP) "mezzanine" capacitors require the use of curtain coating or vertical roller coating and solvent developing.[1]

The third objective was to make the new EP technology less expensive than existing options. Creating embedded resistors using thin metal films [2] has become commonplace but the materials have a limited range of sheet resistance and a scarce material and manufacturing supply base. Similarly, available capacitor technologies[2,3,4] are limited in range of applicability, don't allow for discrete capacitors and can be difficult to process.

The EP technology described in this paper is compatible with any 1-x-1or 2-x-2 HDI build-up. Screen-printing of PTF resistors has been in the industry for decades, is accessible to most PWB fabricators, and has been shown to be low-cost from both the material and processing aspects. The HDI dielectric-based embedded capacitors and inductors are limited in range of applicability, but they are inherent to the HDI build-up process and therefore are available for embedding at no additional cost.

The process flow for the EP technology is shown for reference in Figures 1 and 2. A brief description of the reliability and performance of each of the embeddable elements follows.

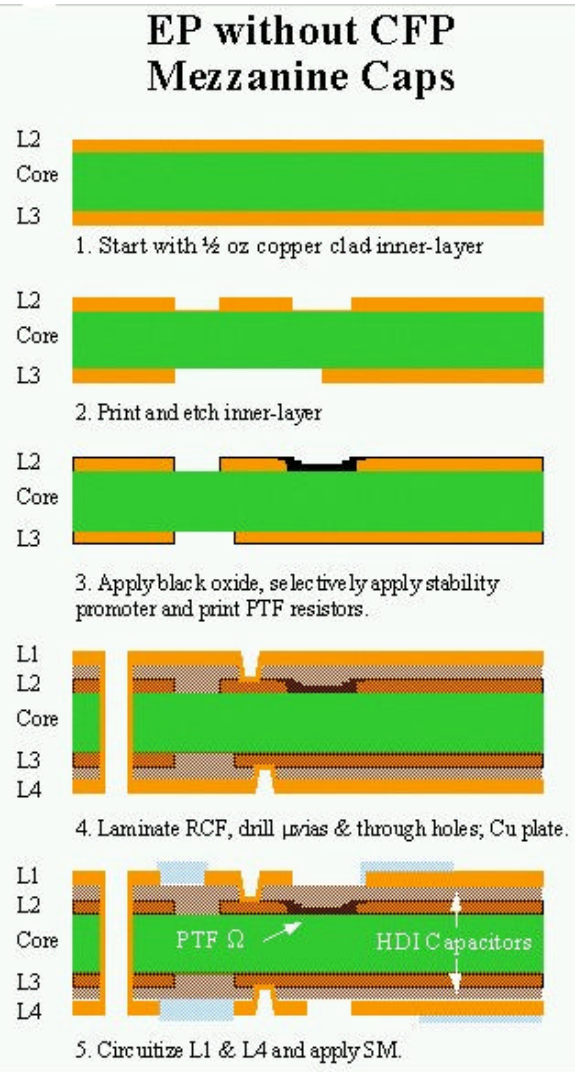

Figure 1 - General EP Technology Process Flow. Features Include: PTF Resistors, HDI-Dielectric Capacitors And Inductors

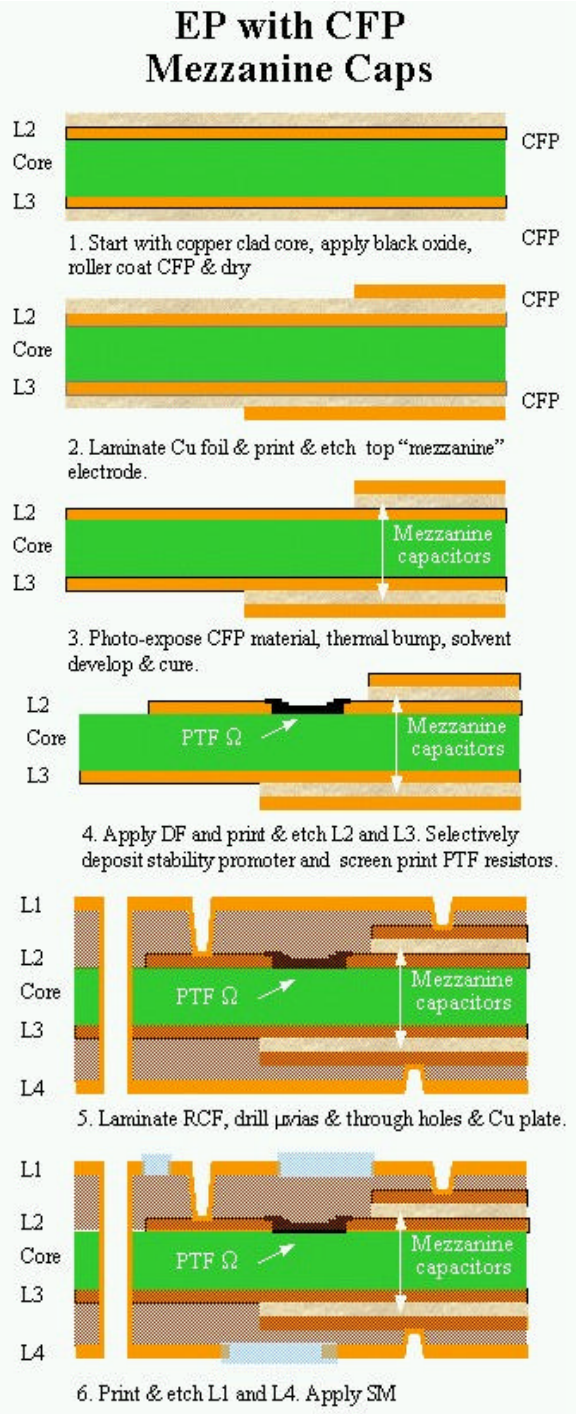

Figure 2 – EP Technology Process Flow with CFP Features Include: CFP Mezzanine Layer Capacitors, PTF Resistors, HDI Dielectric Capacitors and Inductors

PTF resistors

Improvements in commercially available PTF inks[5] combined with internally developed processing enhancements have resulted in the deployment of a broadly applicable and highly reliable PTF embedded resistor technology. The ASAHI TU-00-8 carbon phenolic resin ink is used to create the embedded PTF resistor. This ink is available in sheet resistivities from 35 Ω/□ – 1 MΩ/□ and can be blended in order to achieve any value in between. PTF resistor technology allows for multiple inks to be printed on the same layer, thereby covering resistors with values as low as 18 Ω to as much as 10 MΩ.

Conventionally, PTF embedded resistors are printed either directly on etched copper terminations or on screened silver paste terminations. Neither of these two existing PTF resistor processes can meet the industry's requirements of high reliability and increased space savings. Terminating directly on copper results in relatively poor resistor stability under environment stress (exposure to 85% relative humidity/85 °C)[2] due to corrosion at the copper/carbon ink interface. This can be ameliorated by printing at fairly large resistor dimensions (widths of several mm), but advanced products require sub-mm resistor widths and high resistor densities to provide significant space (and cost) savings vs. discrete surface mount chip resistors.

Motorola's EP technology interposes a proprietary material between the copper termination and the screen-printed PTF resistor. Replacing the traditional silver paste with an interfacial stability promoter deposited directly on the copper terminations substantially mitigates resistor drift under environmental stress while preserving the precise edge definition and density advantages of photolithographically patterned copper. Figure 3 shows that the overall change in resistance after 500 hours exposure to 85% humidity/ 85°C is within ±10% of the initial value when the stability promoter is used. Moreover, this resistance increase is entirely reversible (Figure 4) when exposed to a bake-out (3 hour at 125°C) and therefore not indicative of device performance in real operating conditions. In separate tests, resistors were exposed to 5X- high temperature reflow (peak temperature 220°C) followed by 500 cycles of liquid-to-liquid thermal shock resulting in a ±4% change in resistance.

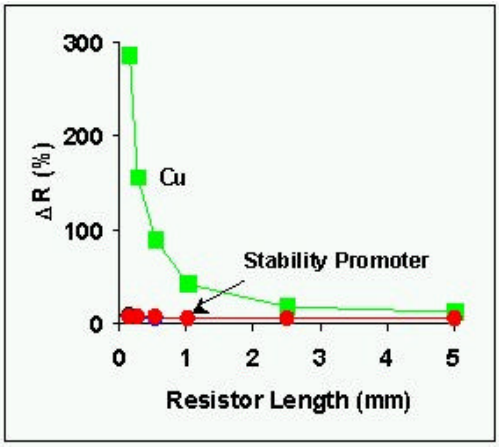

Figure 3 – Reliability of PTF Resistors Printed on Bare Cu Terminations and Cu Terminations Treated with a Stability Promoter after 500 Hours of 85% Humidity/85 °C

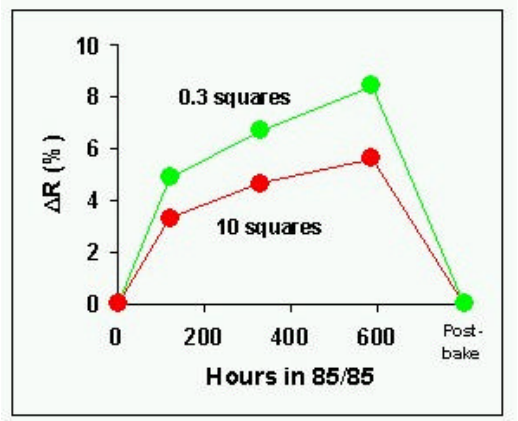

Figure 4 – Resistors Exposed to 600 Hours of 85% Relative Humidity/85 °C Show Near Complete Recovery after 3 Hour Bake at 125 °C

Capacitors

The capacitor technology was developed in two phases. In the first phase of the technology deployment the HDI-dielectric was used to form the parallel plate capacitors. The capacitance density of a typical HDI dielectric is 0.8 pF/ mm^2 at a dielectric thickness of 50 µm. This limited the reasonable embeddable capacitor range to less than 12 pF although larger capacitors could be done if space allowed.

In the second phase of the technology deployment, a high permittivity CFP material was co-developed in partnership with Vantico AG and allows for embedding discrete capacitors that lie between the core and outer HDI layer (hence the name "mezzanine" capacitor). The manufacturing process requires vertical roller coating, lamination and solvent developing but the added equipment is readily available and has not been a detriment to deployment.

The material properties of the CFP can be seen in Table 1. The capacitance density of 16.8 pF/mm^2 (@ 12 µm dielectric thickness) allows, for example, 30 pF capacitors to be embedded in an area less than 2 mm^2. The reliability under stress (temp/humidity and LLTC) of the mezzanine capacitors is satisfactory with minimal drift during testing and nearly full recovery after post-bake.[1]

Inductors

Inductor technology focused mainly on creating 2-turn and 2.5-turn multi-layer spiral inductors with the embeddable range up to 22 nH. Development work focused on creating mathematical models for predicting the behavior of embedded inductors at a variety of RF conditions and determining the main causes for variability. The tolerance of the embedded spiral inductor is between 15-20% and is affected by the registration, print-and-etch and HDI dielectric thickness control capability of the individual PWB fabricator.

Design Considerations

Designing EP components into RF circuits requires intimate knowledge of the circuit operating requirements, the capabilities of the EP technology and properties of the materials used in creating the embedded elements. Table 1 shows the capability of the EP structures and a list of the relevant EP material properties.

Figure 5 is an illustration of the methodology applied for sorting out which passive components may be embeddable in any given design. The selection process always begins with an analysis of the bill of materials (BOM) and electrical schematic. As an initial screening to determine which passives are embeddable, the values and tolerances of each of the components are always analyzed first. The RF engineer is then required to make an assessment of components which are too critical to circuit functionality for embedding. Critical may entail passive components that require high Q, high power dissipation or are noise sensitive and components that are used for fine-tuning the circuit functionality. Furthermore, the electrical engineer must determine how to layout the EP elements such that their individual functions do not interfere with each other and degrade the overall circuit performance (mutual/parasitic capacitance or inductance). Finally, a calculation must be done to determine if there is adequate space on the respective layers to embed all the selected parts. Whereas the PTF resistors typically use space only on the inner-layer, inductors and capacitors require space on both inner and outer layers. Although this may seem unfavorable, EP circuit elements can be combined with each other as well as with SMT components to produce a module with an overall smaller footprint and equivalent functionality. Examples of novel techniques used to lay out an RF component are presented in the case study.

Table 1 - EP Performance Characteristics and Material Properties

EP Performance Characteristics								
	Embeddable range	Tolerance @ 1.3 CpK (untrimmed)	Usable Frequency	Peak Q	Power	Trimmable	In-process testable	Copper Thickness
Resistors	18 Ω - 10 MΩ	20%	Tested up to 3 GHz	N/A	≤ 100 mW/mm^2	Yes	Yes	15 µm max @ termination
HDI Capacitors	1 pF-12 pF	15%	Tested up to 3 GHz	30	> 100 V (break down)	Not tested	Not currently	Top: 25-32 µm Bottom: 17 µm
Mezzanine CFP Capacitors	2 pF - 450 pF	15%	Tested up to 3 GHz	35 to 50	> 100 V (break down)	Not tested	Not currently	Top: 9-12 µm Bottom: 17 µm
Inductors	Tested up to 22 nH	15%	Tested up to 3 GHz	70		Not tested	Not currently	17-32 µm

Material Properties					
	Dk	Tan δ	Capacitance density	Resistivity	TCC/TCR
HDI Dielectric	3.8 - 4.3	2%	0.8 pF/ mm^2 @ 50 µm thickness	n/a	
CFP Dielectric	20-22	2-4%	16.8 pF/mm^2 @ 11 µm thickness (@ 10 MHz)	n/a	Near X7R
PTF ink	n/a	n/a	n/a	30 Ω/□ - 1 MΩ/□	300 ppm/C

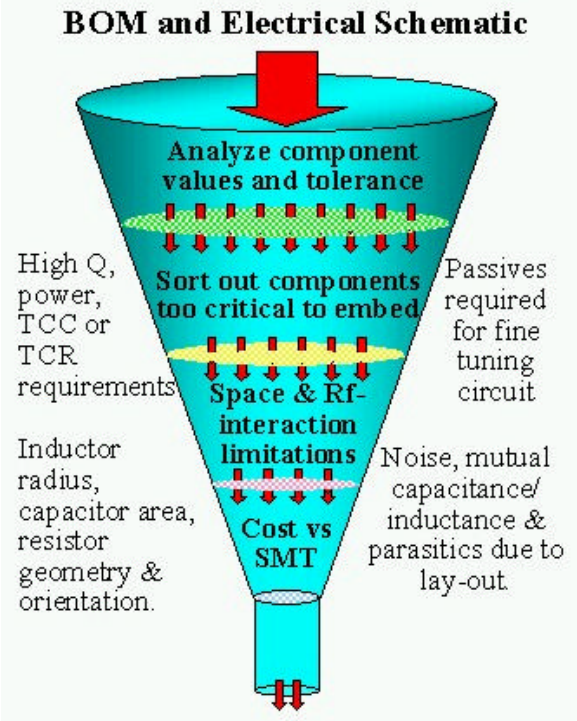

Figure 5 – Methodology for Deciding on Embeddable Components within a Given Design

After the selection process has been completed, the cost of the EP assembled module must be compared to an equivalent SMT module. Many of the early EP module designs were direct replacements for existing SMT ceramic RF modules. This enabled a direct cost comparison and has become the major selling point for promoting EP-RF modules into new products. New EP designs do not lend themselves to such easy comparisons because many times there is no non-EP alternative. Nevertheless, EP technology has shown to be a viable cost reduction opportunity for most RF and other module applications.

RF Module Case Study

An EP-RF module was designed as a cost reduction opportunity to replace an existing co-fired ceramic module in a GSM phone (Figure 6). The design utilized PTF resistors, HDI capacitors and inductors. The EP-module is a 7 x 9 mm component designed with the same pin-out and footprint of the existing ceramic version in order to facilitate drop–in surface mounting onto the motherboard substrate. More than half of the module's passive components were embedded into the four-layer HDI/FR4 build-up structure. Eight resistors were embedded using two different inks. Capacitors were embedded as parallel plate structures with 50 µm HDI epoxy as the capacitor dielectric. Inductors were embedded as single or two-layer copper traces. At the time of this design (1999), CFP capacitors had not been scaled-up for production and therefore could not be used. Comparison of the EP module with both the co-fired ceramic version (and alternative SMT versions) demonstrated that the electrical performance of the EP-HDI module, including phase noise, is equivalent or superior.

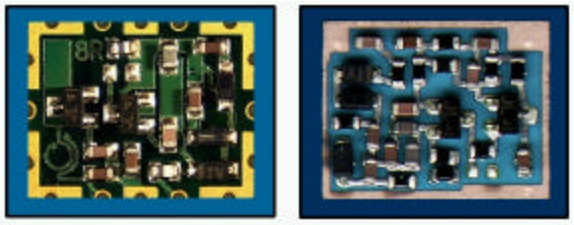

Figure 6 EP RF Module on HIGH Tg FR-4 Substrate (left) Designed to Replace an Existing Co-fired Ceramic Component (right)

A schematic cross-section illustrating the board construction is shown in Figure 7. A single HDI layer is applied to both sides of a 20 mil thick, high Tg FR4 core. The bottom of the module is primarily groundplane and pinout pads; most of the circuitry is on layers 1 and 2. PTF buried resistors on layer 2 are connected to layer 1 circuitry by µvias allowing for a very efficient board design, with few long traces that would introduce parasitics or interference. The finest line and space are 4 mils. Microvias and pads are 5 and 10 mils, respectively.

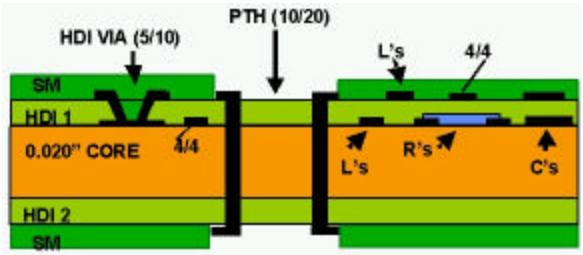

Figure 7 - Schematic Cross Section of RF Module Substrate Construction, with Feature Dimensions Shown in Mils

Embedded Resistors

In most designs the possibility of embedding resistors is usually examined first because they are the most abundant passive component and offer the greatest potential for freeing up surface real estate. The vacated surface area can then be utilized to either embed larger caps or inductors that otherwise could not fit or to shrink the module footprint.

An analysis of the RF module's electrical schematic led to the conclusion that all eight resistors could tolerate 20% variation and therefore should be embedded. Figure 8 shows the lay out of the PTF resistors on layer 2 of the module design. A 50 Ω/□ ink was used to print 22, 51, and 220 Ω resistors. A 1000 Ω/□ ink is used to print 1.5, 1.8, and 2.2 kΩ resistors. The resistors are 400-750 µm wide and 280-850 µm long. The use of two different inks allows the

design to be compacted into the desired footprint. Additionally, resistors were terminated directly onto the bottom electrode (layer 2) of the HDI-parallel plate capacitors thereby minimizing both electrical losses and occupied space (Figure 8).

As a rule of thumb the added cost of printing two or more inks is not an issue as long as the panel resistor density exceeds 8k-10k for each print. There are many factors that impact the substrate cost, but the single most important factor is panel utilization. The higher the resistor density per panel the lower the substrate cost and ultimately, the overall module cost. In the case of this RF module, using two inks to embed all the resistors was necessary to achieve the desired footprint, eliminated the need for more expensive dual package transistors or 0201 components, and created space to embed a costly inductor. These extra benefits significantly offset the cost adder of not having a minimum panel resistor density.

Capacitors

Only 3 out of a possible 11 capacitors were embedded. Five capacitors had values out of range for capacitors fabricated with HDI-dielectric. Out of the remaining six low-value capacitors (<12 pF), the electrical design engineer identified three as either too critical to circuit functionality or necessary for circuit fine-tuning to embed. The remaining three were embedded as parallel plate capacitors with electrodes located in layers 1 and 2. The selection of non-critical capacitors for embedding was validated by an experiment in which the size of the embedded capacitor (and hence value) was varied by ± 24%, without any impact on assembled module yield.

The size of the capacitors had to be calculated based on the capacitance density of 0.8 pF/mm^2 (@ 50 µm dielectric thickness). Capacitors over 1 pF occupy a space larger than what is normally required for a 0402 surface mount capacitor. In multilayer HDI constructions and in constructs utilizing CFP, it is possible to bury the capacitors so that they do not compete with SMT components for topside real estate. In a single-layer HDI construction, such as this one, the top electrode resides on the outer layer. Nonetheless, embedded capacitors up to 2.2 pF were used in the design because (1) they are essentially "cost-free" while concurrently saving the component and assembly cost of the displaced SMT equivalent; (2) the requirement that the footprint of the EP module must match that of the existing LTCC module resulted in otherwise unused space; and (3) the space efficiency of the embedded capacitors was enhanced by having top electrodes double as solder pads for one or more SMT components (Figure 8).

Inductors

Embedded inductors less than 4 nH were designed as single-layer copper traces (transmission lines), typically 6-8 mils wide. Higher inductance values (up to 10 nH) were designed as two-layer windings (spiral). EP inductor performance can be predicted well but still requires expert engineering judgment to assess the circuit's robustness to manufacturing process variations. The inductor geometries were modeled and then imported into the Mentor Graphic component library for use with current and future designs.

Even low value spiral inductors occupy more space than most 0402 components. However, it is recommended to embed as many inductors as possible because they also come at no additional cost. Furthermore, as shown in this case study, they occupy no top-side surface area because SMT components were placed directly over them (Figure 8).

Cost

The EP-RF module in the case study used 13 fewer parts than the equivalent co-fired ceramic component. This translated to a part cost savings of over 10%. A 30% substrate cost savings was realized when replacing the co-fired ceramic with HDI-EP. The savings in assembly cost were even more significant exceeding 40%. This was mainly due to the difficulty in handling the ceramic substrates during the assembly process. The HDI-EP parts are produced on standard size PWB panels and are shipped in large format arrays that facilitate efficient and high speed assembly practices.

It has been observed with numerous other examples that EP technology is ideal for a multitude of module applications and can generate significant cost savings. The savings realized from 1999-2001 on this single RF module has paid well beyond the cost of developing the technology.

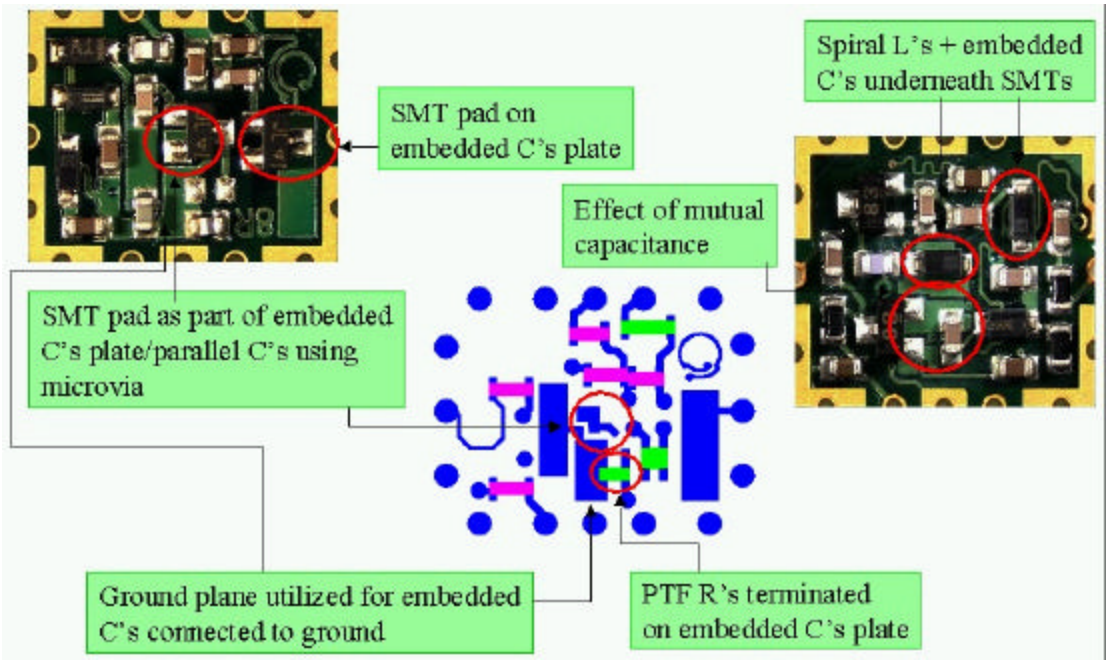

Figure 8 – Depiction of Layer 2 (center) for a RF Module Using 50 W/☐ (green) & 1 kW/☐ (pink) Ink to Print PTF Resistors Novel Design Elements Used in this EP-RF Module Include: PTF Resistors Sharing Termination Pads and PTF Resistors Terminating onto Bottom Electrode of Parallel Plate Capacitor (center); Top Electrodes of Capacitors Doubling as SMT Solder Pads and Ground Plane Areas Used for Creating Large Caps-to-Ground (top-left); Spiral Inductors "Hidden" Underneath SMT Components (top-right)

Conclusion

The EP technology described in this paper enables a significant number of passive components to be easily and reliably embedded into organic HDI substrates. It is compatible with all HDI build-up processes and is commercially available from three global PWB suppliers. The case study demonstrated that HDI-EP RF modules are an excellent application for the technology and that significant cost savings can be realized.

Each OEM is likely to place a different value on part count reduction, increased functionality and smaller board size depending on the specific situation. This technology allows the OEM to seriously consider using HDI-EP to help them achieve all of their objectives today and into the future.

Acknowledgments

We are indebted to Dave Peckham, Jie Xue and Sande Petty-Weeks for their significant contributions to the deployment of this technology and to the design and manufacture of the RF module presented in our case study. We are especially grateful to all of our industry partners: Barrie Jones of Polymore Circuit Technologies for his expert collaboration and direction during the development of the PTF resistor technology; Juergen Herbert and Richard Stoessel of Vantico AG for their efforts in developing the CFP material; to each of our PWB fabricators for their patience and hard work in helping us establish a world class supply base: Wolfgang Bauer and Heinz Gach of AT&S; Kota Noda of Ibiden Circuits of America and Peter Tan and Brandon Huang of WUS Printed Circuit Co.

Part of this work was funded by DARPA through Wright Laboratory under Agreement F33615-96-2-1838.

References

1. Robert T. Croswell, Ph.D. *et al.*,"Embedded Mezzanine Technology for Printed Wiring Boards". IPC Printed Circuits Expo 2002, March 2002
2. William J. Borland and Saul Ferguson, "Embedded Passive Components in Printed Wiring Boards: A Technology Review," *Circuitree*, March 2001.
3. John Davignon and Bob Greenlee, "A PWB Fabricator Perspective of Embedded Decoupling Capacitance Materials", IPC SMEMA Council APEX^{SM} 2001, 2001.
4. T. Hubling, Ph.D, and M. Xu, "Investigation of New Materials for Embedded Capacitance in Printed Circuit Boards," IPC SMEMA Council APEX^{SM} 2001, 2001.
5. Isao Morooka, "Developments in Polymer Thick Films", *Electronic Packaging and Production*, January 1993.