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Experimental and Numerical Assessment of Plated Via Reliability

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Abstract
This paper discusses two typical PTH failures – barrel cracking and post separation – induced by accelerated testing or observed during manufacturing. Finite element models have been developed to help understand the effect of the hole design parameters on the stress/strain state after thermal excursions.

An identical approach is then applied to study buried core vias – buried vias that connect from layer 2 to layer n-1 in a Type II, high density interconnect (HDI) board. The impact of via fill material and its mechanical properties are also presented. Additionally, the use of finite element analysis to perform life is discussed.

Introduction
Plated through hole (PTH) is one of the key interconnects in a multilayer printed wiring board (PWB). It is also arguably the weakest link in an unassembled PWB. The underlying source of this reduced reliability is the high coefficient of thermal expansion (CTE) of the laminate material in the thickness (Y) direction. PTH failure due to thermo-mechanical stresses has been studied[1,2,3] in the past with major emphasis focused on cracking in the barrel.

The Weakest Link
What is the weakest link in a fully assembled electronic product? Traditionally, the focus has been placed on the solder joints between the packaged components, especially area array packages such as ball grid array (BGA), and the PWB – the 2nd level interconnects. Figure 1 is a qualitative illustration on how the board thickness affects the reliability of the PTH and the solder joints of a specific package. It is expected that the influence of board thickness on solder joint reliability will taper off as the board reaches a certain stiffness level.

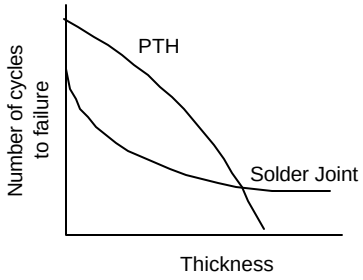

Figure 1 – Effect of Board Thickness on PTH and Solder Joint Reliability

Conversely, a fixed hole size PTH will be less reliable as the thickness and aspect ratio continue to increase. Theoretically, there is a crossover point where PTH becomes the weakest link. This suggests that more systematic studies on the PTH failure modes are critical to ensure the reliability of the future printed circuit assemblies (PCAs).

Figure 2 is a Weibull plot showing the 2nd level reliability of two area array packages (shaded area) in comparison to PTH from two board suppliers. The area array packages are 1 mm pitch, CCGA (1247 I/O) and PBGA (1156 I/O). The test board is 12 layers, 2.36 mm (0.093") thick. PTH is 0.25 mm (0.010") drilled hole size (DHS). The accelerated thermal cycle (ATC) was performed between 0 to 100°C. Boards from vendor A showed PTH reliability similar to the solder joint reliability. However, boards from vendor B showed PTH reliability much worse than that of the solder joint. Even though the early failures in the vendor B boards were probably caused by poor copper quality, it clearly demonstrated the importance of quality control in high aspect ratio PTH PCAs.

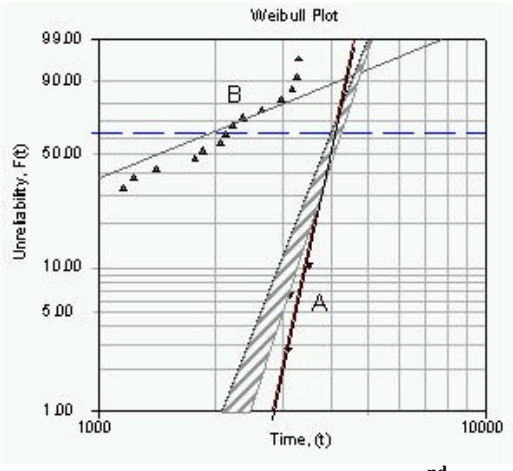

Figure 2 – Weibull Plot Showing the 2nd Level Reliability of Different Reliability Packages and PTH
Shaded Area Denotes the of Solder Joint Reliability
A, B are Reliability of PTH from Two Suppliers

Finite Element Analysis (FEA)

FEA has been used extensively in the electronics packaging industry to assess thermo-mechanical stresses within a package due to package assembly and to evaluate solder joint reliability for BGA-type packaging.[4,5,6] In this study, FEA was used to assess the experimental results obtained from the PTH reliability tests. The ANSYS FEA software application is employed for this investigation.

In order to simplify the modeling efforts and minimize computation time, a 2-D axisymmetric finite element model was utilized as an initial effort to model the PTH structure.[7] Only the top half of the PTH structure was modeled with symmetric boundary conditions along the bottom and outer surfaces of the model to constrain the out-of-plane displacements in those areas as a worst-case approximation. The outer surface is located at half the PTH pitch, i.e. at the midpoint between two adjacent PTH's. The model was created parametrically and employs a user-defined ANSYS command macro to generate each layer of the PTH. This facilitated the model generation of various PTH geometries. Figure 3 illustrates the model geometry with the various materials denoted.

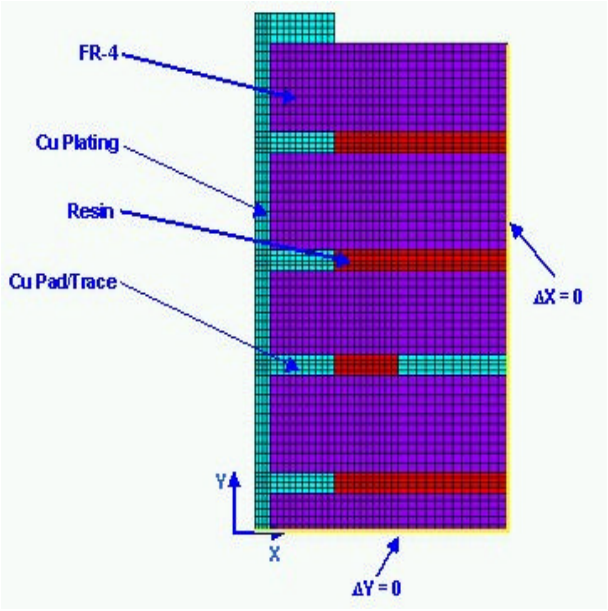

Figure 3 – Finite Element Model of PTH

The FE model incorporated nonlinear elasto-plastic behavior of the copper using a bilinear kinematic hardening model and linear elastic behavior of the FR-4 and resin materials. The FR-4 material also included orthotropic behavior for the elastic modulus and coefficient of thermal expansion. The material properties utilized in the finite element models are shown in Table 1.

Table 1 – Material Properties Used in the PTH FE Model

Material	T [°C]	Elastic Modulus [GPa]		CTE [ppm/°C]		Poisson's Ratio		
		x	y	x	y	xy	xz	yz
FR-4						0.39	0.14	0.39
	-55	19.5	8.48					
	125	15.4	6.76					
	<140			17.6	70			
	>140			17.6	300			
Resin						0.39	0.14	0.39
	<140	6.2	6.2	70	70			
	>140	6.2	6.2	300	300			
Copper		124	124	17	17	0.34	0.34	0.34
	Yield Stress = 0.25 GPa Tangent Modulus = 1.17 GPa							

PTH Barrel Cracking

Barrel cracking is the most common failure mode of plated through holes. It is typically a fatigue crack that occurs after the board has gone through several thermal excursions (from the assembly processes and/or field operation). Several copper fatigue models have been proposed that relate the cyclic strain range (Δe) to the cycles-to-failure (N_f). The most noticeable work is from Engelmaier.[8]
Where:

$$\Delta e = D_f^{0.75} N_f^{-0.6} + 0.9 \frac{S_u}{E_{Cu}} \left[\frac{e^{D_f}}{0.36} \right]^{0.1785 \log\left(\frac{10^5}{N_f}\right)}$$

Δe = cyclic strain range
D_f = copper ductility
N_f = cycles-to-failure
S_u = ultimate strength of copper
E_{Cu} = Young's modulus of copper

There are other formulae using similar expressions between Δe and N_f. In general, they are all empirical equations derived from experimental data. Figure 4 summarizes the "range" of some of the fatigue models. It is more difficult to predict high cycle fatigue failures since a slight change in strain range can result in an order of magnitude change in cycles-to-failure. Previous work[1] suggested that life prediction between 50 to 200% is reasonable.

FE models are commonly used to predict the cyclic strain range in a fatigue failure. The advantage of detailed numerical modeling is that the material anisotropy and complex geometries can all be accounted for. Critical stresses and strains at any point in the structure can be obtained and incorporated with a fatigue prediction model (such as Figure 4) to estimate the fatigue life.

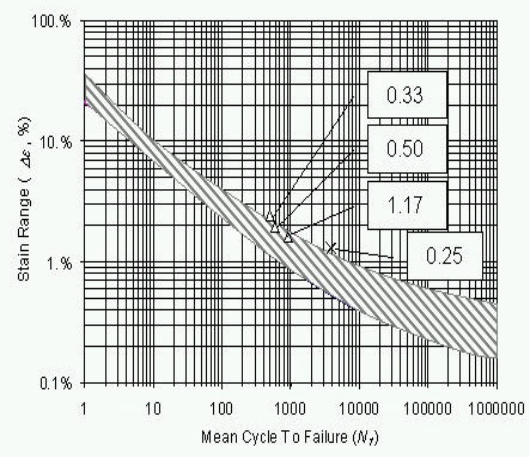

Figure 4 – Comparison of PTH Fatigue Models (shaded area) with Experimental IST Data of 3 PTH Sizes (D) and ATC data (X)

As an example, the FE model in Figure 3 was used to simulate various PTH sizes within a PWB under Interconnect Stress Test (IST) conditions. Three different drilled hole sizes, 0.33 mm (0.013"), 0.50 mm (0.020") and 1.17 mm (0.046"), were evaluated. The simulated copper cyclic strain ranges, based on an isothermal temperature cycle between 25°C and 150°C, are plotted in Figure 4 with the experimental cycles-to-failure from Interconnect Stress Test[9] (IST). Also, plotted in Figure 4 is the ATC data from figure 2, vendor A and its modeled strain range. Both FEA and experimental data indicate that the PTH reliability improves with increasing PTH diameter, or decreasing PTH aspect ratio. These trends agree with the studies previously cited and the general experiences.

A more detailed examination on the accuracy of the fatigue life prediction with the current FEA approach is beyond the scope of this article. It is critical to note that both the material properties and boundary conditions input into the model can impact the accuracy of the result. As detailed in reference three, sources of accurate material properties are very limited. In addition, FEA does not take into account process and quality variations. Therefore, experimental data should always be used to further validate and refine the FE model.

PTH Post Separation

Post separation creates intermittent opens in a printed circuit assembly (PCA) typically during in-circuit test (ICT) or early in its service life. It is generally attributed to processing issues, such as improper hole drilling, poor desmear and/or electroless plating or excessive thermal shocks.[10] Post separation is often observed in larger hole sizes, such as connector holes (Figure 5). The stress/strain components at the pad/barrel interface using the same FE model in Figure 3 was employed to assess the driving force for this failure mode.

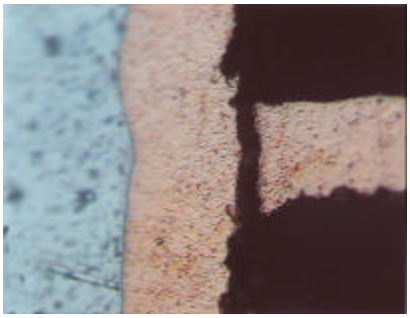

Figure 5 – Post Separation at a Backplane Connector Hole After Assembly

The early failure characteristic of post separation suggests that it is not a fatigue related failure. Indeed, the cyclic strain range at the intersection of a copper barrel and inner layer pad shows a higher strain range for smaller vias (Figure 6) – not favoring the large hole sizes.

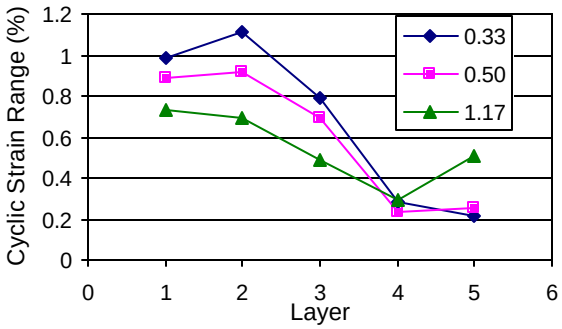

Figure 6 – Variation of the Cyclic Strain Range at the Pad/Barrel Interface (PTH Diameter in mm)

Other stress/strain components at this interface are illustrated in Figures 7-10 with respect to the locations of the pad/barrel interface. It was found that only the stress in the X direction (perpendicular to the plated copper barrel) is consistently higher for the larger hole sizes (Figure 7). This stress also increases away from the center of the board, or closer toward the surfaces of the board. A bending moment acting on the innerlayer pads as the laminate expands/contracts during the thermal cycling is likely the cause for this stress (Figure 11). Further analysis is necessary to determine if the X direction stress component is the only contributing factor to this failure mode.

Based on this analysis, post separation is a failure that occurs when the stress exceeds the "strength of the material" – the bond strength between the barrel metallization and the innerlayer pad. The strength of the interface is weakened when there is a processing issue. On the other hand, improper rework processes

can subject the board to excessive temperatures that increase the stress level and cause an initially good board to fail.

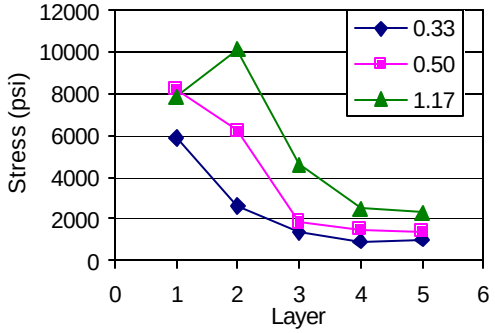

Figure 7 - Variation of Stress in the X-direction at the Pad/Barrel Interface (PTH Diameter in mm)

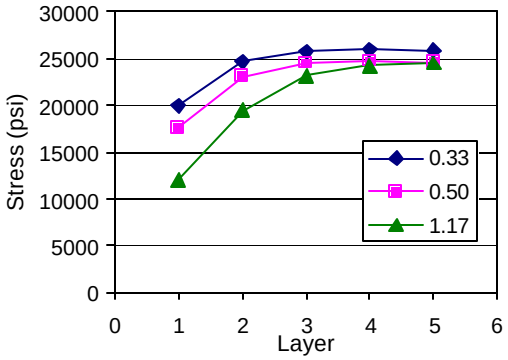

Figure 8 – Variation of Stress in the Y-direction at the Pad/Barrel Interface (PTH Diameter in mm)

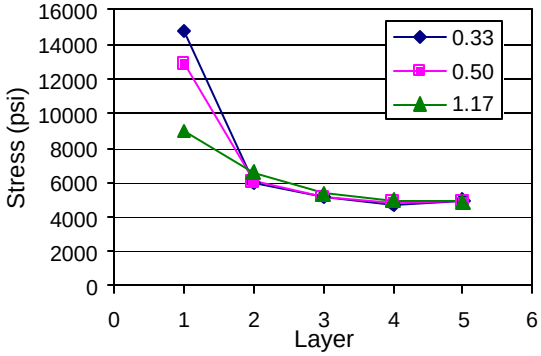

Figure 9 – Variation of Shear Stress in the XY-Direction at the Pad/Barrel Interface (PTH Diameter in mm)

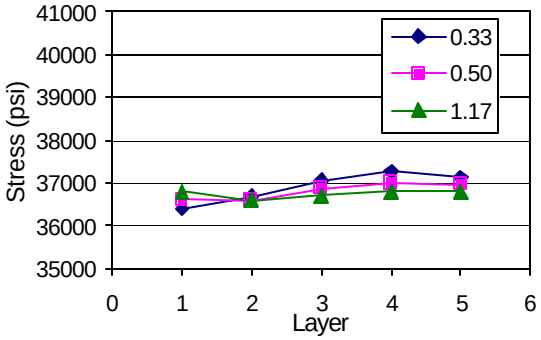

Figure 10 – Variation of Von Mises Stress at the Pad/Barrel Interface (PTH Diameter in mm)

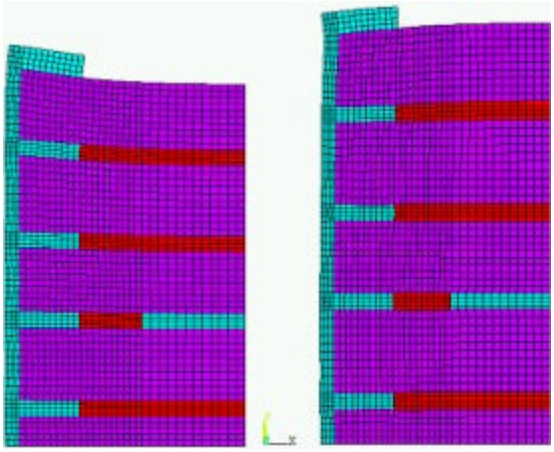

Figure 11 – Bending of the PTH Pads (Pad Rotation) During Thermal Loading (Left: Cold Cycle; Right: Hot Cycle) Note: Deformation is Exaggerated by About 7X

Buried Core Via

It has been demonstrated how FEA can be used to provide mechanics-based insight into the PTH failure modes. The same technique can be applied to model the buried core via found in a Type II, HDI board.

Buried core via is a key feature that differentiates a Type II HDI board from a Type I HDI board. It connects from layer 2 to layer n-1 and typically has a high aspect ratio. Two issues associated with the buried core via have been constantly raised:

1. Should the via be filled? If so, with what material and to what percentage?
2. How much plating is required?

One will obtain different answers from different board suppliers on the first question. Pre-filling the buried core via provides better surface flatness and prevents insufficient resin fill during lamination. It requires another process step and increases the cost. Conversely, the resin in the prepreg can fill these core vias in-situ during the final lamination step. However, there is less control in the fill percentage and the resulting dielectric thickness. Therefore, the question about the necessity of a 100% fill arises. In

fact, 100% filling may be difficult to achieve by both methods as the aspect ratio of the buried core via gets higher. IPC 6012A suggests that 60% filling of the buried via is sufficient, but how would one perform an experiment, with varying void volumes, to verify that? FEA becomes a very convenient tool to provide good comparative guidelines on this subject.

A PTH and a buried core via model was created based on a 14-layer Interconnect Stress Test (IST) coupon. This IST coupon was 2.36 mm (0.093") thick, with a 1 mm (0.040") via pitch, 0.25 mm (0.010") DHS for both PTH and buried core via. The FE models are shown in Figure 12.

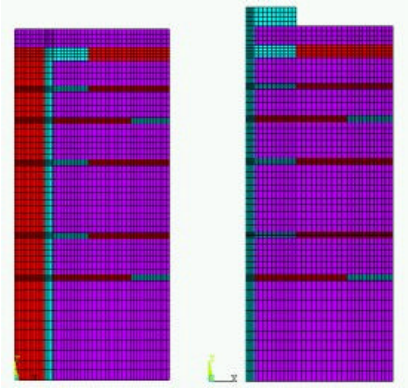

Figure 12 – FE Model of A 14 layer PWB with Buried Core Via (Left) and PTH (Right)

Four sets of via fill materials were used for the model. Their mechanical properties are listed in Table 2.

Table 2 – Material Properties Used in the Buried Via Core FE Model

Material	T [°C]	Elastic Modulus [GPa]	CTE [ppm/°C]	Poisson's Ratio
Filler A	25	4.5		0.4
	<155		31	
	>155		88	
Filler B	25	1.6		0.4
	<120		98	
	>120		150	
Epoxy Resin	25	6.2		0.4
	<170		70	
	>170		300	
Solder	25	30.6	24.5	0.35

Effect of Fill Materials

In a study by Goyal et al,[11] it was concluded that the fatigue life of a PTH could be impacted positively when the PTH is filled with solder. A similar trend was observed in this study of the buried core via (Figure 13).

However, it is interesting that two of the fill materials (i.e. epoxy resin and filler B) can cause the buried core via to be less reliable than the unfilled PTH. This result is not surprising considering that a filler with a very high CTE can help in stretching the copper barrel during thermal loading. Also, a low modulus filler is not capable of "sharing" any significant amount of stress in the copper barrel.

In contrast, materials with controlled CTE's (e.g. filler A) can alleviate this problem. Higher modulus and lower CTE are clearly the right combination for the via fill material formulation.

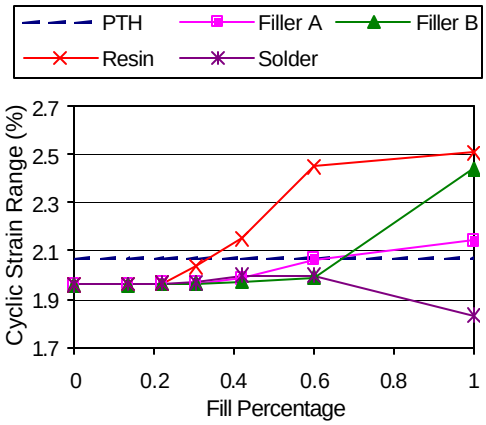

Figure 13 – Maximum Cyclic Strain Range in a Buried Core Via with Different Via Fill Materials and Fill Percentage

Effect of Fill Percentage

A cylindrical void was generated at the center of the buried core via by removing a portion of the elements. The effect of fill percentage was studied by varying the void volume. The maximum cyclic strain range in the copper barrel calculated at different fill percentages are shown in Figure 13.

Again, the effect of fill percentage is strongly dependent upon the fill material properties. If the fill material can lower the cyclic strain range when the buried core via is 100% filled, then the buried core via is always more reliable than the PTH at any void volume. For this type of "reliability enhancing" fill material, the higher the fill percentage the better the reliability. Conversely, if the fill material is "reliability degrading" then it is better to have the buried vias completely unfilled.

It can be seen from Figure 14 that the cyclic strain range of an unfilled buried via is less than that of a PTH. This could be attributed to any of two possible reasons:

1. The stiffness of dielectric over the buried via adds a constraint to the buried via and thus reduces the plastic strain in the copper.
2. The lower aspect ratio of the buried via makes it more reliable than the PTH.

To test these hypotheses, the dielectric thickness over the buried via was reduced to see if the reduction of the dielectric stiffness would increase the cyclic strain range. As the dielectric thickness approaches zero, the model becomes a PTH with the same aspect ratio as the buried core via. The results obtained are illustrated in Figure 15.

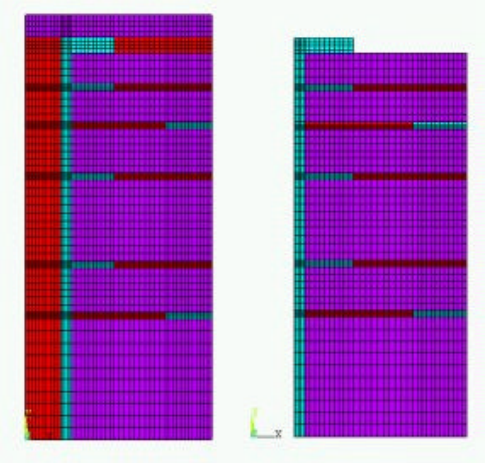

Figure 14 – A Buried Core Via (left) vs. A PTH (right) of the Same Aspect Ratio

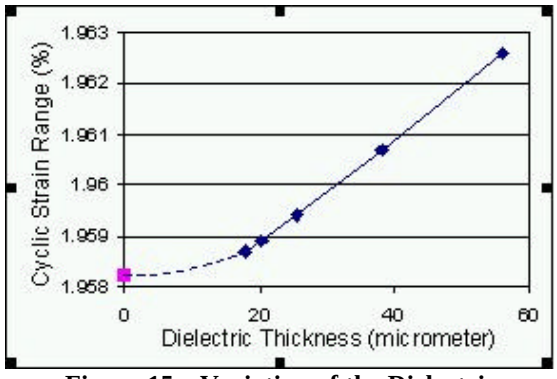

Figure 15 – Variation of the Dielectric Thickness over the Buried Core Via

Note that the cyclic strain range actually increases as the dielectric thickness increases. Therefore, the lower plastic strain in an unfilled buried core via is simply due to the lower aspect ratio. This analysis also suggests another important reliability guideline: the dielectric between the buried core via and the surfaces should be thin when possible.

The construction of a Type II HDI board requires that layer 2 and layer n-1 be plated at the same time the core vias are plated. It is therefore desirable to reduce the amount of copper plating to achieve fine line capability and good line width control on these layers. Lower plating thickness also prevents innerlayer image transfer (smoother outerlayer surfaces) and insufficient resin fill during the final lamination.

It has been concluded in the previous studies[1,2] that thinner copper plating will result in lower fatigue life of the copper barrel. This study has also demonstrated that some via fill materials, including the epoxy resin from prepreg, can further reduce the fatigue life of the buried vias. Consequently, it is not recommended that the plating be thinner in the buried core vias than in the PTH.

Observations on Buried Core Via Failures

IST coupons were manufactured based on the models featured in Figure 12. Copper plating in the barrel was determined from cross section measurements. As previously described, thinner plating in the buried core vias was observed in all coupons manufactured by the two different suppliers. (See Table 3.)

Table 3 – Copper Plating Thickness (in Micrometer) in Buried Core Via and PTH Measured From Cross Sections

	Fill Materials	Buried Core Via	PTH
Vendor C	Epoxy Resin	38	41.5
Vendor D	Filler B	24.3	32.5

Preliminary IST results on these coupons confirmed that the buried core via tends to fail earlier than the PTH when "reliability degrading" fill material were used.) Detailed results will be published later.

Figure 16 shows two buried core vias, filled with resin from prepreg, and failed after assembly. The dark field images indicate that the fracture is in both the copper barrel and the filled resin. We do not consider the copper barrel crack to be fatigue related. It is more likely to be the result of poor ductility in the plated copper. However, it is also possible that the resin may have fractured first and then the crack propagated into the copper. That would be another undesirable failure mechanism associated with pure resin filling in the buried core vias.

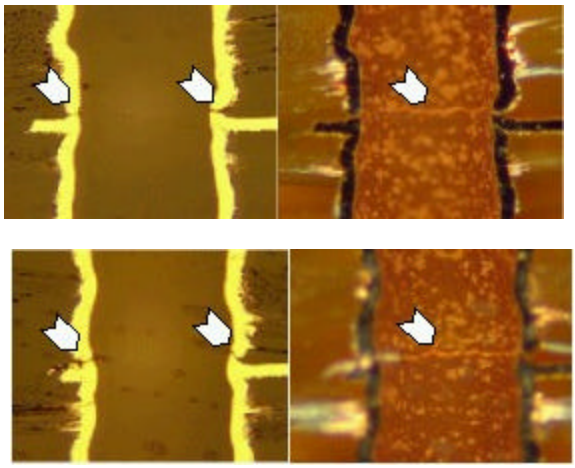

Figure 16 - Barrel Cracking in Buried Core Vias Filled with Resin from Prepreg during Final Lamination (Left: Bright Field, Right: Dark Field)

Figure 17 shows yet another failure mode associated with buried core via – laminate crack between the buried core via and outerlayers.

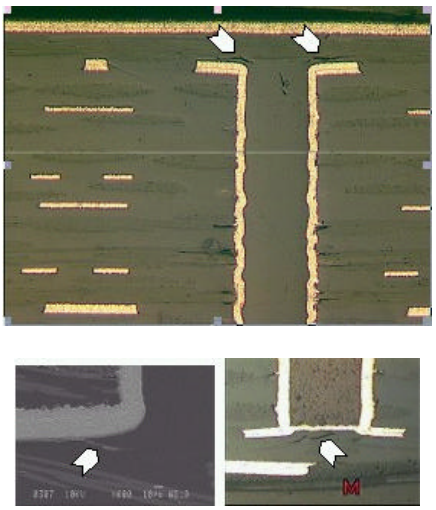

Figure 17 – Laminate Cracks Between the Via Fill Material and Prepreg Outside the Buried Core Via

This type of laminate crack was found both in as-received samples and thermal stressed samples, with latter being worse. Figure 18 shows that there is high stress (Y direction) concentration at the interface of the buried via pad and the top dielectric. This stress is developed when the via fill material expands more than the surrounding copper barrel and laminate during the heating cycle. Conceivably, a "reliability enhancing" material should also help alleviate this type of failure.

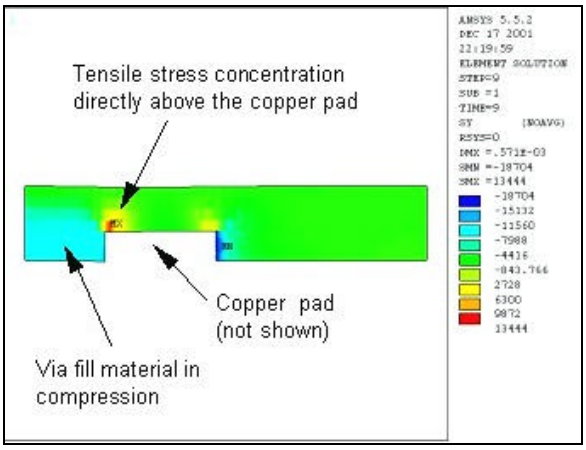

Figure 18 – Stresses (Y-Direction) Distribution in the Dielectric Layer over the Buried Via During the Heating Cycle

Conclusions

FEA has been successfully used to study some of the failure modes observed in PTH and buried core vias. The method alone can provide useful information regarding reliability trends and parameter sensitivity. Life prediction is also possible in combination with experimental data and failure models.

Specifically, this study has identified that the fill material in a buried core via can greatly impact its reliability. Glass transition temperature, CTE and elastic modulus are the key properties in determining whether the fill material can enhance or degrade the reliability.

Acknowledgements

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