Presented at IPC Printed Circuits Expo® 2002
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HDI'S Technology Influence on Signal Integrity

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Abstract
Highs Density Interconnects (HDI) printed circuits are now being designed in ever increasing quantities. HDI brings some interesting new solutions to age-old signal integrity (SI) concerns, and concerns that will grow as rise-times continue to drop.

This article focuses on five major areas of SI concerns:
1. Noise
   a. Noise-reflections
   b. Noise-crosstalk
   c. Noise-simultaneous switching
2. Electro-Magnetic Interference (EMI)
3. Interconnect Delays

In each case, HDI offers improvements and alternatives - but it is not a panacea. A couple of 'cautions' are listed that can be a major stumbling block to HDI implementation, fortunately, they are not SI based. Important to SI is the materials used in HDI. Although not the focus of this article, the materials selected as well as the dimensional stack-up and PCB design rules will influence SI and electrical performance (impedance, crosstalk and signal conditioning). Miniaturization provided by HDI will be a major contributor to SI performance. Finally, fine-pitch BGAs are addressed in term of design rules and layer stackups, all using the improved SI performance recommendations included in this article

Introducing the Benefits of HDI
The widespread use of new electronic components employing Ball-Grid Array (BGA), Chip Scale Packaging (CSP) and other evolving technology form-factors means new fabrication techniques must be used to create printed circuit boards (PCBs) that will accommodate parts with extremely tight lead pitches and small geometry's. In addition, extremely fast clock speeds and signal bandwidths challenge systems designers to find better ways to overcome the negative effects that radio frequency interference (RFI) and electro-magnetic interference (EMI) have on their product's performance. Finally, increasingly restrictive cost targets are compounding problems associated with today's smaller, denser, lighter and faster systems.

Staying competitive and delivering the products people want means seeking out and embracing the best available technologies and design methodologies. The use of PCBs incorporating microvia circuit interconnects is currently one of the most viable solutions on the market. Adopting microvia technology means products can utilize the newest, smallest and fastest devices, meet stringent RFI/EMI requirements, and keep pace with downward-spiraling cost targets.

What is Microvia Technologies?
Microvias, as the name implies, are vias of less than or equal to 6 mils (150 micron) in diameter. Their most typical use today is in blind and buried vias used to create interconnections through one dielectric layer within a PCB. Microvias are commonly used in blind via constructions where the outer layers of a multi-layer PCB are connected to the next adjacent signal layer. Used in all forms of electronic products, they effectively allow for the cost effective fabrication of high-density assemblies. The IPC has selected High Density Interconnection Structures (HDIS) as a term to refer to all of these various microvia technologies.

Why use Microvias in PCBs?
Better Electrical Performance / Signal Integrity
Due to the physical structure of microvias, there is a reduction in switching noise. This is attributable to the decreased inductance and capacitance of the via as its physical size becomes smaller and shorter. A microvia will have nearly one-tenth the electrical parasitics of a through-hole. Another advantage of using microvia technology for creating interconnects is a reduction in signal reflections and crosstalk between traces. The corresponding increase in routability area also allows designers to place traces further apart when necessary to reduce crosstalk.

Improved RFI/EMI/ESD

In the realm of RFI/EMI, increased routability area combined with the microvias physical via-in-pad implementation allows designers to place more ground plane around components. By doing this, the size of ground return loops decreases and improved RFI/EMI performance is realized. These benefits are highlighted in Figure 1.

Figure 1 – Benefits of HDI Come from Five Major Areas

Signal Integrity and Electrical Performance

I am certainly not a signal integrity expert! The information I will present here has been presented before by experts.[2,3] These experts have done a very good job in training me and I hope that my explanations here do them justice. Just in case I happen to be slightly off, you can download several excellent papers from www.GigaTest.com.

Signal integrity improvements are certainly available to all who take the time to respect 'Mother Nature'. HDI's contribution comes mainly from the adage," Smaller and Closer is Better!", that is. HDI's main contribution is ***miniaturization***! The signal integrity improvements for HDI comes from three phenomena:

1. Reduction of noise
2. EMI radiation reduction
3. Improved signal propagation and lower attenuation

Noise

There are really only four different categories of noise that all the various effects can be described by[2]:

- Signal quality of one net and its return path (ringing due to reflections)
- Cross talk between two or more nets (noise pulses due to switching on neighboring lines)
- Switching noise (noise on power and ground lines/planes)
- ElectroMagnetic Interference (EMI)

A simple illustration of this is provided in Figure 2 and Table 1.[2]

Noise can come form many sources, many created by the layout of the board:

- Change in trace width
- Plane splits
- Cutouts in Power/Ground planes
- Via antipads
- Insufficient plane capabilities
- Excessive stubs, branched or bifurcated traces
- Component lead frames
- Improper impedance matching and termination networks
- Coupling between signals
- Varying loads and logic families

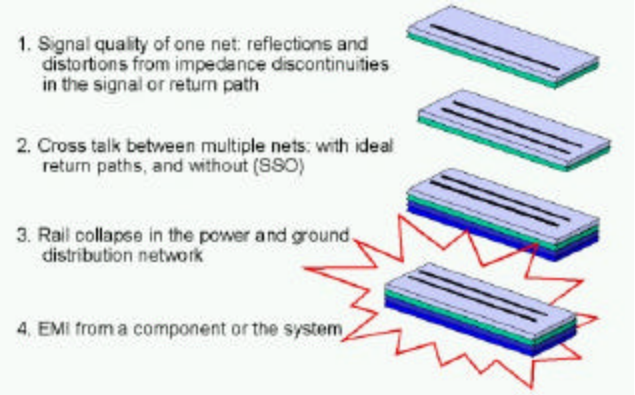

Figure 2 - All Signal Integrity Problems Can Be Grouped in Four Families

Each one has specific causes. By identifying the cause of each family of problems, design and technology based solutions can be identified and implemented.[2]

Signal Quality of One Net

HDI is a fabrication technology of miniaturization. Where we kill two birds with one stone, is that shorter interconnect length, smaller vias and thinner dielectrics of lower dielectric constant materials not only make the substrate smaller- - they also improve signal integrity!

With HDI, devices can be brought so close together that the signal may not need to be terminated. This is not just close from a surface point-of-view but also that the secondary or backside of the interconnect can be utilized effectively. "Interconnects with a time delay shorter than about 20% of the rise time of the signal may not need to be terminated."[2] The interconnect length is given by:

$LENGTH_{short}$ must be less than 20% τ_{12} in/nsec/$\sqrt{\varepsilon r}$.[2]

Where: τ_{12} = signal rise time in nsec

εr = dielectric constant of the material

For a rise-time of 1 nsec, for FR-4, this is only 1.14 inches.

Table1 - HDI Features and the Signal Integrity Problem they Help Solve [2]

HDI Features	Signal Quality	Cross Talk	Switching Noise	EMI
Short interconnect lengths	X	X		
Low dielectric constant	X	X		
Small vias and small features	X		X	
Vias in pads			X	
Fine lines and thin dielectric		X	X	X
Support for fine-pitch components			X	X

The signal return path is just as important as the signal path. It exists whether you provided for it or not! It contributes to the inductance, capacitance and resistance experienced by the signal. The signal return current will seek the path of minimum energy, which is the least impedance. For low frequency, this path will be the least resistance, but for high frequencies, it will be the path that minimizes the current loop. At higher frequencies, inductance dominates over resistance, so the return path follows the signal path even though this is higher resistance.

The low dielectric constant results from the use of many new HDI materials. Many of these are not glass-reinforced and thus have lower dielectric constants than glass-reinforced laminates. Many of these dielectrics are liquid such as the high-Tg epoxy or polyimide, or the photodielectric resins (PDR). Some are thin-vacuum laminated dielectrics with high thermo-plastics contents. However, all are uniformally – THIN- and this contributes to reductions in wiring delays and reduction in noise.

Crosstalk Noise

HDI miniaturization provides shorter interconnect lengths and if the lower dielectric constant material is used, then cross talk in HDI substrates is reduced:

$$\frac{Vnoise}{Vsignal} = \frac{len\ coupled}{len\ sat} = \frac{len\ coupled\sqrt{\varepsilon r}}{\tau_{12}\ in/nsec} K_b$$

Cross talk in HDI substrates is reduced by the shorter coupled lengths and by the lower dielectric constant. This reduction can be as much as 50%. Shorter trace lengths will radiate less, and traces with thinner dielectric will radiate less. The thinner the traces, the less the mutual capacitance *(Cm)*. Moreover, the thinner the distance to the reference plane, the lower the near –end crosstalk will be or the same crosstalk for a longer coupled length. With length reductions of 2x and dielectric thickness reductions of 2x over conventional boards, the radiated field from HDI signal loops might be reduced by as much as 4x, which is 12 dB.

Simultaneous Switching Noise (SSN) and Voltage Rails

The actual circuit performance varies with the rise-time of signals. Because most of these larger-higher performances HDI boards deal with high-speed computer busses and telecom signals, they are very sensitive to noise and signal reflections. Switching noise is the most difficult type of noise to control. It has its origin in the instantaneous demand for current as devices turn on and off. Any drop in the power supply voltage will adversely affect components. This then involves the power distribution in the board and how devices are connected to ground. Keeping the inductance of the power and ground distribution low and the inductance to the ground connections low reduces this type of switching noise or 'ground bounce'. Conceptually, this would look like this:

$$\Delta V = N_{switching}\ L_{effective}\ \frac{di}{dt}$$

To manage SSN, the focus needs to be on:

1. Minimizing di/dt
2. Good selection of decoupling capacitance
3. Careful induction management

Reducing $L_{effective}$ can be helped by HDI techniques. The use of area array packages instead of peripheral leaded packages is one way. Watching how ground is assigned on peripheral leaded packages is another. Increasing the number of power/ground leads to packages and using a power/ground plane in the package (even a floating plane) helps. However, the major issue is board layout. Nearly 70% of BGA and QFP inductance is due to breakout routing on the PCB or the ground return path. The choice of microvias now provides and advantage. Looking at the simple lumped models of PCB vias in Figure 3 shows that the smaller microvia has nearly 1/10 the inductance and capacitance of a through-hole via.

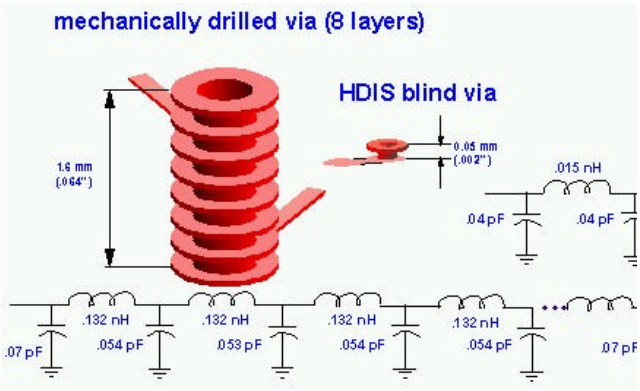

Figure 3 - Lumped Models of a Microvia Compared to a Drilled Through-hole Via

Via-in-Pad and Short Via Lengths

Expert 1 provided the partial self inductance of a microvia 2 mils deep and 1 mil in diameter as less than 10 pH, while a drilled via, 10 mils in diameter and 32 mils deep has a partial self inductance of almost 200 pH. This is significant for higher frequency designs. At 300 MHz, Expert 1 goes on to point out that the impedance of an HDI microvia is only 18 milliohms compared to the through-hole via which is 400 milliohms.

The via-in-pad reduction of inductance is even more dramatic. One of the largest sources of inductance to devices and decoupling capacitors is the trace-via combination to power and ground. By placing the microvia in the SMT pad, this inductance is decreased to practically nothing. This is compared to a conventional trace to a through-hole that at 20 mils would be as much as 500pH to the loop inductance. This loop difference is shown in Figure 4. Using a via-in-pad microvia and a surface ground plane, there is essentially no inductance to ground and if power is used as the second layer under the microvia, only a minimum inductance to power. The close nature of this power/ground combination will lower loop inductance and provide a significant amount of decoupling capacitance. A final advantage is the reduction of part spacing and shortening of all the signal tracks. Figures 5a and Figure 5b show high-speed controlled impedance multilayer redesigned with only the use of microvias-in-pads [4]. No parts were changed and current assembly minimum spacing was observed. The advantages from a cost and size point-of-view is nearly 40 % lower cost, from 12 layers to 8 layers and 40% smaller in size, allowing more up on a fabrication panel. But that the signal integrity was improved significantly.

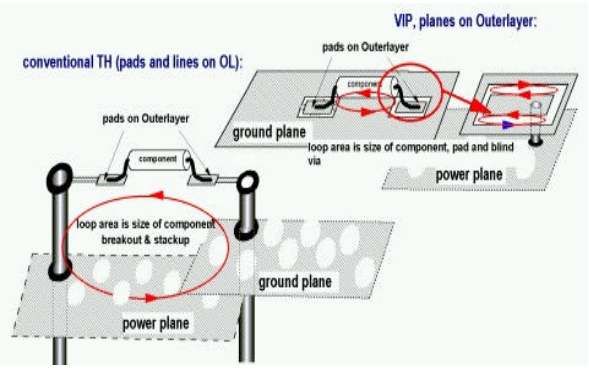

Figure 4 - Comparison of the Power-ground Loop on a Conventional through-hole Multilayer Compared to a Microvia-in-pad Design with a Flooded Surface Ground Plane

Power / Ground Distribution

Keeping the inductance of the power and ground distribution low is a major objective if fast rise-time circuits are going to be used. Two factors that contribute to the inductance of the power and ground interconnect: are the physical length of the path, and the separation between the actual power and ground planes.

Again, advice[2] is: "The use of very thin dielectric layers between the power and ground planes contributes to a very low loop inductance for the power and ground currents. For two rectangular conductor sheets, separated by a dielectric thickness, h, the loop inductance for current to go down one surface and return back on the other is given by:

$$\text{Loop} = \mu 0h \left(\frac{len}{W}\right) = h \times \left(\frac{len}{W}\right) \times 33\text{pH/mil}$$

Where *len* is the length of the current path and *W* is the width. The loop inductance decreases as the spacing between the power and ground planes drop.

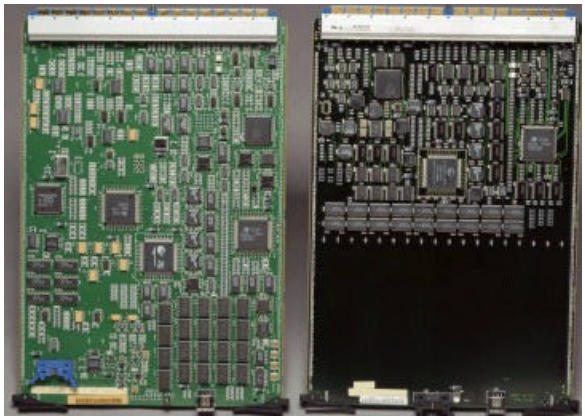

Figure 5a - A 12 Layer, Controlled Impedance Multilayer was Redesigned Employing only Microvia-in-SMT Pads on the Left is the Original Through-hole Version, and on the Right, the Microvia Version but Requiring only 8 Layers

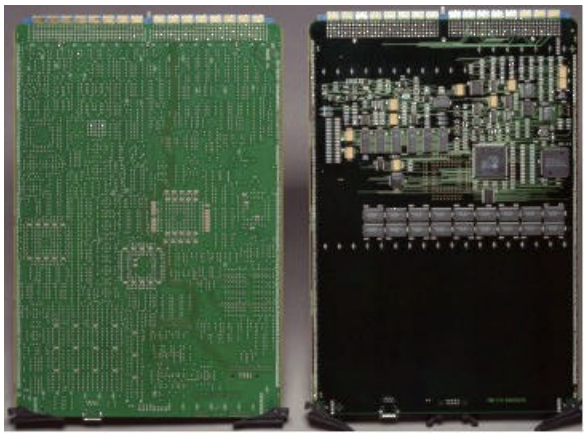

Figure 5b - The Secondary Side of the Redesigned Multilayer Shows the Advantage of Blind Vias and the Via-in-pads Design Concept

When the dielectric thickness is one mil, there can be as low as 33 pH/square of loop inductance. When the current travels in conductors that are shaped like a square and have the same length as width, the loop inductance is independent of the size of the square. This represents a rough approximation to the typical interconnect inductance in the power and ground planes. Between the decoupling capacitor pads and the chip attach pads, the connecting loop inductance can be about 1 square's worth. Thin HDI layers can keep the power and ground inductance very low."

Signal Propagation and Interconnect Delay

Higher via density, microvias (smaller vias) and via-in-pads allow components to be placed closer together reducing wiring delays by a factor up to 50%. Signals propagating through a transmission line have a characteristic velocity that is primarily determined by the square root of the effective dielectric constant of the surrounding medium. The reciprocal of this velocity is the signal propagation delay per unit of conductor length. This is for a classical microstrip topology, but if the conductor is located between two reference planes, then it is proportional to the square root of the materials dielectric constant:

$$\text{Propagation Delay}(ns/in) = 0.847\sqrt{e}$$

Where: e = dielectric constant of substrate

Interconnects with a time delay shorter than about 20% of the rise time of the signal may not need to be terminated.

EMI Radiation

Ground Return Path

Voltage and current waves are supported by propagating electric and magnetic fields. The ideal return path is continuous and uniform. This is usually not the case in high-speed dense circuit boards. The more the return path is non-ideal, with discontinuities, the more it produces ground loops. The ground loop of the conventional through-hole with inner-layer power and ground has been discussed prior and is shown in Figure 4.

The ground planes of a high-speed dense multilayer are discussed here. For this 9.2-inch by 6.3 inch 18 layer board, 8.46 square inches of copper is etched away to make room for the through-holes. When redesigned as a 10 layer HDI multilayer, that replaced the original 18 layer, the surface ground plane had only 6.63 square inches removed and the secondary side had only 6.35 square inches removed. This is 21.6% and 24.9% respectively less discontinuities for the return path. In addition, the fine-pitch BGA devices lets the ground copper go in substantial all the way into the center ground pins.

Effect of Shrinking Pitch on BGAs

Perhaps the most important feature an HDI substrate offers for improved signal integrity is the ability to support the use of flip chip attach and fine-pitch BGAs and CSPs. The improvements in wiring and signal integrity can best be shown by the example of three new BGAs used for high speed networking and computing. These are:

- 676 pin, 1.0 mm pitch, 26.7mm body BGA
- 384 pin, 0.8 mm pitch, 18.5 mm body BGA
- 232 pin, 0.65 mm pitch, 12 mm body

These finer pitch BGAs are shown in Figure 6.

Tight Via Pitch

It has been pointed out: "Even by using heroic efforts to get the inductance of the power and ground distribution of the substrate as low as possible, the inductance of wire bonds can swamp any gain. With a partial self-inductance of a wire bond of roughly 1 nH/mm, and typical wire bonds on the order of 1 mm long, the inductance of one bond can be 1 nH. To reach the 10 pH range, a minimum of 200 wire bonds would be needed just for power and ground. Microvias on an 8-mil (200 micron) pitch can provide the connections for most high pin count flip chips (or BGAs). With a solder ball length of only 5 mils (0.15mm), the chip attach inductance can be reduced over an order of magnitude from wire bonding."

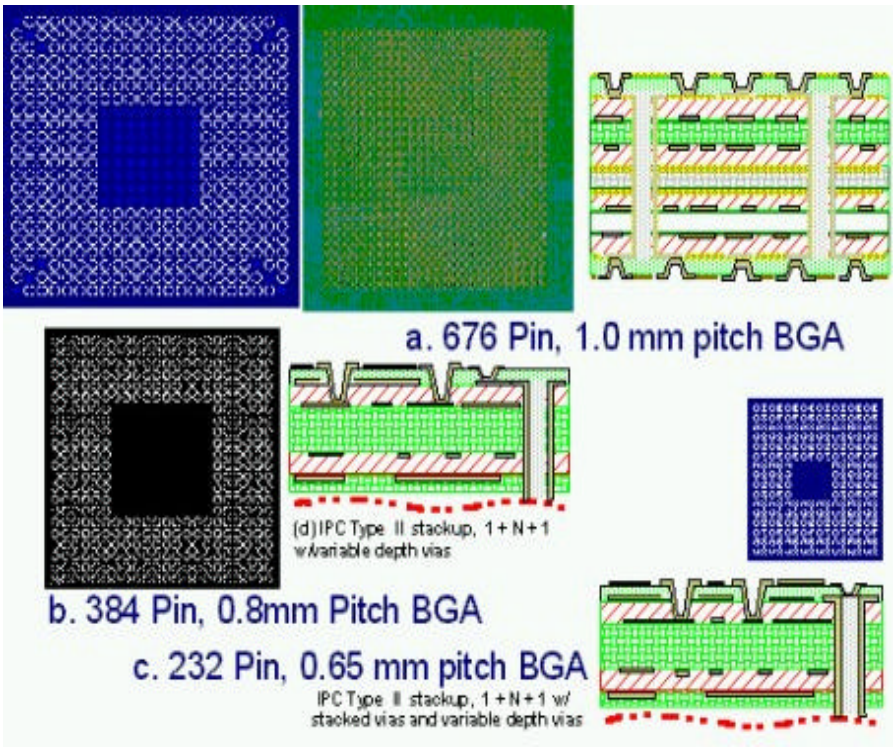

Figure 6 - Three Fine-pitch BGAs that Require Microvias:
a. 676 I/O BGA with 1.0 mm Pitch a
b. Surface Pattern (layer 1 b. 384 I/O BGA with 0.8 mm Pitch a. Surface Pattern (Layer1)
c. 232 I/O BGA with 0.65 mm Pitch a. Surface Pattern (Layer 1)

Conclusion

Blame it on Maxwell's Equations, but SI is getting more important and *more difficult*. HDI provides small geometries and dielectrics. Providing you take advantage of the other benefits of HDI, like lower costs and higher densities, SI will benefit as well. All of the problems listed get worse as signal rise times decreases. With current IC geometries shrinking, decreasing signal rise time is assured. Unfortunately, the amount of time to solve these problems is also shrinking. The successful company will be the one that masters signal integrity problems and HDI.

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