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Processing Thin Core Capacitor Materials[1]

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Processing thin core capacitor materials can be challenging, particularly those with non-reinforced dielectric less than 0.001" thick. Several processing steps require special attention to ensure the material is not damaged during manufacturing. Material storage and loading systems, conveyor systems and lamination systems must be capable of handling thin core material. Equipment modifications or special fixtures may be required in order to reduce the risk of jam-ups or fractured material. Special attention to cleanliness and the documentation of careful handling practices are also important. This paper will review some of the lessons we have learned about processing thin core capacitor materials from our participation in the NIST Advanced Embedded Passives Technology consortium.

Merix currently produces a considerable amount of product with .002" or less power/ground cores. The demand for this product is increasing as the need for distributed capacitance, reduced board impedance and EMI shielding grows. The typical product incorporating thin power/ground cores are boards with from twelve to thirty layers, approximately 0.093" thick, often utilizing 1mm pitch ASIC packages.

As a participant in the NIST Advanced Embedded Passives Technology (AEPT) consortium, embedded capacitor test boards have been built with from one to four cores of materials that are ≤ 0.001" thick. Figure 1 shows the TV1-C four-layer test board that includes one embedded capacitor core. This board was used for thermal cycle, thermal shock, temperature/humidity and ESD testing of several embedded capacitor materials.

The TV2-C (figure 2) is an eight-layer high frequency (>5 GHz) test board that includes two C-Ply embedded capacitor cores. This board incorporates microvias and is designed for high-frequency model testing of the embedded capacitor materials.

As part of the consortium, the NIST AEPT/Nortel product emulator board has also been built. This board simulates an existing high-speed board and is designed to test signal performance improvement. This is the first emulator board for the AEPT project, and includes both an embedded resistor layer and four cores of 3M's C-Ply, an ultra-thin core embedded capacitance (UTCEC) material.

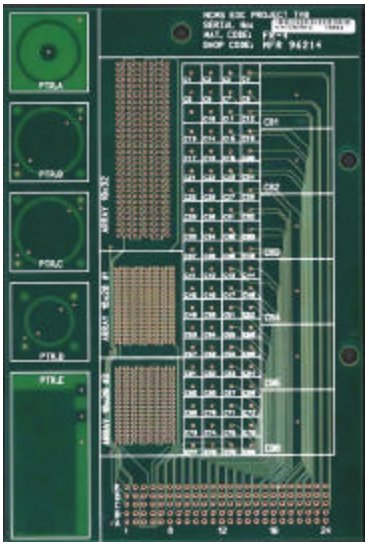

Figure 1 – Pictorial view of the TV-1 Capacitor Design Included 0.170" Square Capacitors - 0.60" Square Capacitors, NIST Capacitor Patterns, and Daisy Array Capacitors

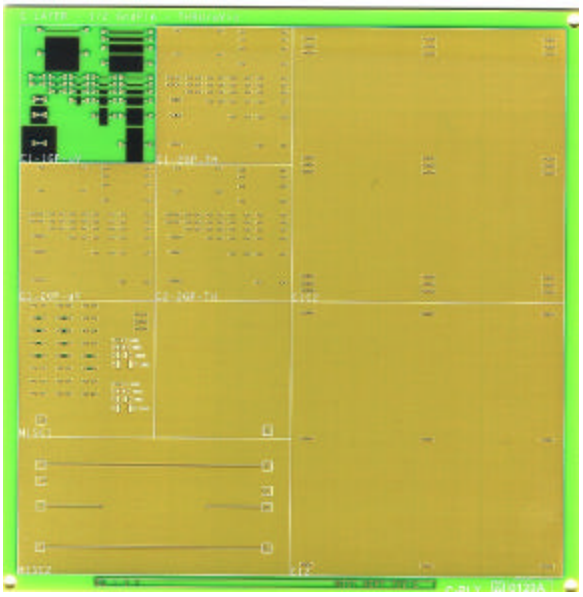

Figure 2 – Pictorial View of the TV-2 Capacitor

Another thin core project was fabricating test boards for a major OEM (see Figures 3 and 4), made with the same UTCEC material and with a .001" core FR4 material. These are twenty layer boards, and incorporate four embedded capacitor cores and microvias. The test boards were used to compare the

board impedance and EMI of several different embedded capacitor materials.

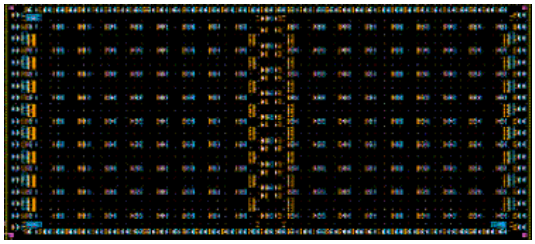

Figure 3 – Pictorial View of the OEM Test Board

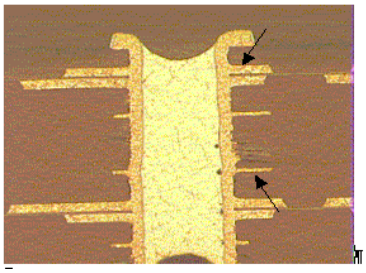

Figure 4 - Cross Section of OEM Test Board Showing Two UTCEC Cores Separated by a Regular Core

Other OEMs have asked us to build prototypes using the same UTCEC material. Figure 5 shows a cross section of a construction using two adjacent UTCEC cores, and Figure 6 shows a construction using a single UTCEC core in the center of the board.

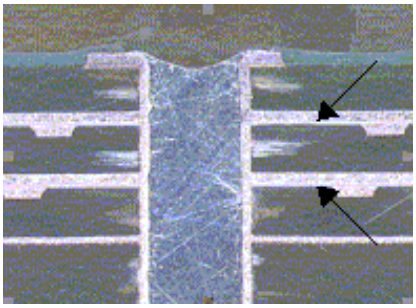

Figure 5 – Adjacent Embedded Capacitance Cores

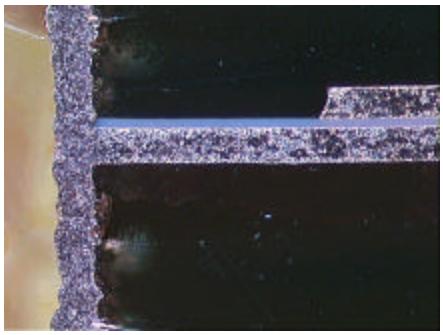

Figure 6 – Single UTCEC Core in Center of the Board

Processing Thin Core Materials

Most materials with core thickness greater than 0.001" can be processed using standard equipment and procedures. However thin, non-reinforced materials that are less than 0.001" thick require special attention to ensure the material is not damaged during manufacturing. Most of our work with very thin cores has been done with the previously described UTCEC material, which has a core thickness of only 0.0003" without fiberglass reinforcement. The following processes may need modification for processing thin cores.

Pre-Clean

Thin core materials can easily jam up in the conveyor system of the pre-clean line. Ensuring that all rollers are in place and properly aligned prior to processing is the first step to eliminating jam-ups. Other modifications, such as repositioning rollers and spray nozzles may be required to make the equipment capable of handling thin core materials.

Resist Lamination

The dry film photo resist auto-laminator may require some process modifications in order to prevent thin core materials from wrapping onto the laminator rolls. However for the most part we found that minor adjustments to the lamination pressure and careful attention to the resist tension were enough to ensure the panels did not jam up in the auto-laminator. A new auto-laminator with thin core equipment options has just been installed, and our preliminary tests indicate that it performs very well with this UTCEC material.

Print

Other than careful handling, the print process is essentially unchanged. Clear traveler instructions and training is the key to successful printing. Cleaning the material can be a challenge and it may be necessary to use a tacky roller to clean the material by hand. However, we have found that at least some of the automatic panel cleaners are capable of tacky cleaning the UTCEC material without damaging it. We are also evaluating the use of the automatic printers to improve handling and help speed up processing of thin cores.

Develop-Etch-and-Strip (DES)

It is fortunate that DES equipment is available and capable of handling the ultra-thin core materials without jam-ups. Whenever panels do wrap around rollers, it is generally the case that the rollers were not correctly replaced after cleaning and line maintenance. Rollers must be placed opposite the spray nozzles to prevent the spray from pushing the thin material out of line.

Care must also be taken that the panels are not bent when removing the mylar from the dry film photo resist. The corners may need to be gently flattened before feeding them into the conveyor. Depending on the equipment, it may also be necessary to offload the panels by hand to avoid damaging the panels.

Hi-Pot Test

All very thin core materials are tested after etching to ensure there are no voids or embedded particulates that might cause high resistance shorts. Because the dielectric thickness of these materials is so small, they won't pass the same standard hi-pot test parameters set for other materials. Final continuity testing of the board is also done at a reduced voltage. Careful handling of the material is the main concern at this step, since it is more fragile after the image has been etched.

Post-Etch Punch (PEP)

Depending on the type of copper foil used, enhancement of the PEP fiducials may be required to improve the contrast between the copper foil and the dielectric. This may be as simple as brushing the fiducials with an eraser, or it may require adjusting the PEP parameters. Again, good material handling practices are important at this process step.

Automatic Optical Inspection (AOI)

All of the thin-core embedded capacitor materials that we tested were able to be inspected using AOI equipment. Different lighting settings were required depending on the copper type, but otherwise, good material handling practices are the main concern for AOI technicians.

Oxide

Both our vertical black oxide and our horizontal alternative oxide lines were effective in treating the thin core capacitor materials. Careful handling is particularly important for the vertical black oxide line. The alternative oxide line has proven capable of handling thin etched cores without jam-ups.

Scaling

During multi-layer lamination, thin-core embedded capacitance materials tend to move differently depending on what materials are adjacent to them. Therefore a scaling run is typically required prior to building any new board stack-up. After the scaling values have been determined, however, they appear to remain consistent from build to build.

Volumes & Yields

Since the beginning of the NIST AEPT project, we have processed about 1600 square feet of this UTCEC material. Pilot test boards have begun to have been built in order to learn more about thin core processing issues and to improve yields.

The pilot test board is a large and complex, twenty-two-layer board with two adjacent UTCEC cores plus two other manufacturer's embedded capacitance cores, also adjacent to themselves. Although we have built only a few orders with small lot sizes so far, Figure 7 shows that the yield of this board is currently running about 75%. A failure mode effects analysis has helped identify problem areas.

Specific yield issues include Hi-Pot failure (which we expected, since none of the incoming UTCEC material was electrically tested prior to receiving it), handling damage, power-to-ground shorts and mis-registration related to scaling.

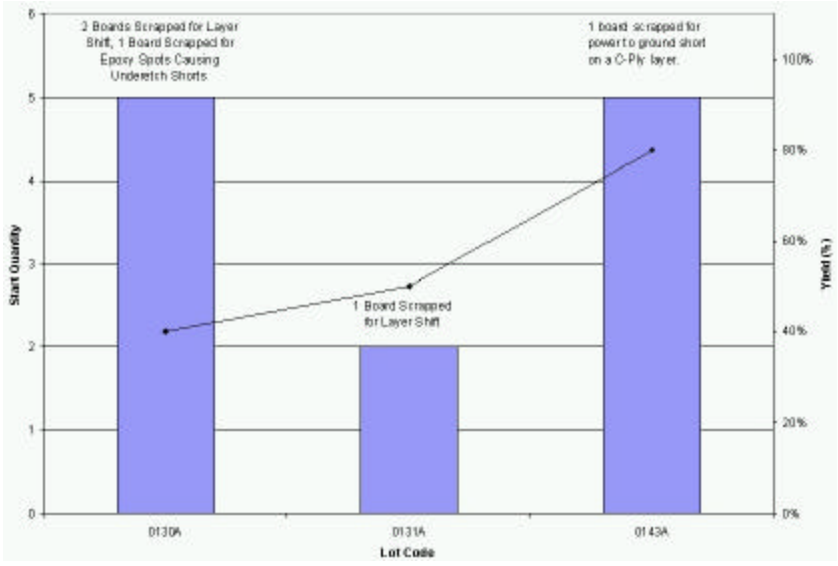

Figure 7 - Yield Trend Test for Pilot Boards Based on UTCEC Material-Related Defects. Line Indicates Yield Trend; Bar Height Indicates Quantity of Boards Started

Lessons Learned

To put it simply, we have learned that in order to process thin core capacitor materials it is critical to have equipment with thin core capability and to provide technicians with good training in thin core handling. That said, there are at least two approaches to etching non-reinforced (i.e. the dielectric does not contain fiberglass) thin core materials such as the UTCEC material.

- **Standard etching** (etch both sides of the thin core material at the same time).
- **Sequential etching** (etch one side of the thin core material, laminate into a subpart, then etch the second side).

Each approach has its own strengths and weaknesses.

Approach 1: Standard Etching

Border Modifications

Because several of the thin core embedded capacitance materials are not self-supporting, they may fracture or disintegrate if the copper is etched away from both sides of the dielectric. Therefore it is important that there are no overlapping etched features. This requires modification of the border files, dams and vents, and placement of full copper out to the edge of the panel. It also requires that the border around the image cannot be etched on both sides, which means that there will be copper out to the edge of the board. This copper does not have to be electrically connected to the plane, but customer acceptance may be an issue for some OEMs.

Other potential problems include tearing of the laminate along the panel edge, particle generation in the etcher, and loss of tooling hole integrity. Figure 8 shows a UTCEC panel etched on both sides using a modified border file. Note the overlapping etched clearance areas where the dielectric material has disappeared. These particles can be problematic in the etch chambers, and require a good filtration system.

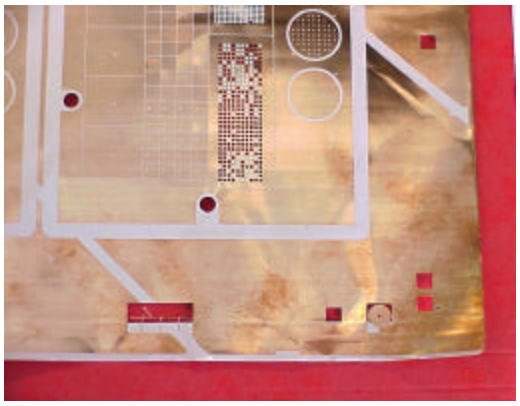

Figure 8 - UTCEC Panel Etched on Both Sides Using a Modified Border File

Approach 2: Sequential Etching

Process Modifications

A second approach to processing innerlayers with non-reinforced thin embedded capacitance materials is to first image and etch one side, laminate that side into a subpart, and finally image and etch the second side of material. Etching one side at a time eliminates the need for artwork modifications and the problem of copper at the board edge, but requires an additional lamination step before the second side is imaged and etched.

Potential problems with this approach include registration of the second side image to first side image and registration of the subpart to the parent part. Subpart constructions are also more prone to epoxy spots, which can create shorts.

UL Qualification and IPC Standards

Multilayer UL qualification of the UTCEC material is being pursued, and test samples for qualification at the laminate level are being pursued with the material provider. Involvement with the efforts initiated by members of the NIST consortium to develop IPC standards for embedded passive materials is also underway. These standards will include a material specification, a board performance specification and a design specification.

Challenges to Implementation

In summary, the primary challenges to implementation of very thin core embedded capacitance materials are the need for equipment capable of handling very thin panels, and technician training on thin core handling. Depending on whether a standard etching or sequential lamination process is used, border file modifications may be required. Other challenges include the tendency of some of the non-reinforced materials to move during lamination, and ensuring that the defect density of the material is low. While challenging, these materials offer a promising next step for increasing the functionality of printed circuit boards.

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