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Solid Solder Deposits (SSDs) For Advanced Packaging Applications

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Introduction

Solid Solder Deposit (SSD) technology was developed in the early and mid-1990's to improve first pass yields in the manufacture of electronic devices. As the trend towards finer pitch surface mount devices accelerated an alternative to conventional solder paste printing at assembly was desirable. Over 60% of defects in the assembly process have been attributed to the paste printing operation. These defects include solder shorts, insufficient solder/opens, and component skew.

With the implementation of higher density devices, i.e. components with pad pitch spacing of .020" (Figure 1) and below, assembly yields declined dramatically. Yields were further exacerbated by the lack of planarity of the hot air solder leveling surface finish. Smaller pad geometries, as well as limitations in the solder leveling process and equipment, made it difficult to maintain a planar finish on double sided surface mount devices, particularly with the most prevalent vertical systems. A higher incidence of solder tails and shorts was more pronounced on fine pitch products. Further hot air leveling could cause thermal degradation, which may result in warp, delamination or solder mask related failures.

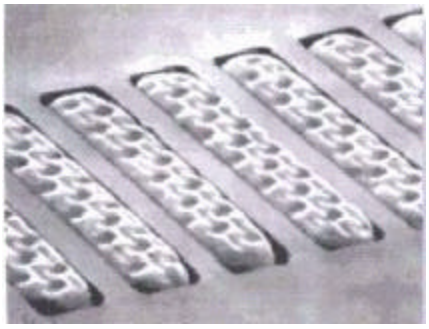

Figure 1 - SSD "Flat Pad" on.020" Pitch SMD

A number of surface finishes gained popularity in an effort to overcome the limitations of solder leveling. Included among these were organic coatings, nickel/gold and immersion tin. End users evaluated each products impact on performance, cost and long-term reliability. While these provided better uniformity than the HASL coating they also presented problems associated with shelf life, a limited number of thermal excursions that could be sustained and poor wetting at assembly.

SSDs were developed specifically to overcome the defects associated with:

- Circuit board surface finish, and;
- Solder paste printing.

While several methods exist to form SSDs, they were developed with a common goal: to perform macro-planar metal deposits on all surface mount lands on the bare printed circuit board and eliminate solder paste at assembly.

Deposits had a sufficient volume thickness so that no additional metallization was required at assembly. The SSDs flat surface topography was designed to prevent component skew at assembly, where a sticky flux was applied prior to component placement and reflow. As the manufacture of complex devices became more challenging, SSDs gained popularity.

SSD "flat pad" applications on the board level were qualified as an alternative surface finish by end users and have been used in a myriad of applications in the automotive, computer, medical and telecommunications industries. In addition to fine pitch devices, BGA and Chip Scale Packages were particularly well suited to the SSD process in that a uniform volume of solder is applied that can be quantified prior to assembly, virtually eliminating the requirement for rework on area array packages.

While a flat surface topography was desirable for conventional surface mount applications, SSDs have evolved and are now formed with both flat and spherical geometries for applications in the PCB, SMD and microelectronics industries. These include pre-formed solder deposits for:

- Flat pads;
- Mechanical connections;
- Pin insertion thru-holes;
- Multi-tiered deposits;
- Solder bumps for semiconductor wafers, and;
- Solder spheres for Chip Scale and BGA packages.

Information is presented on employing SSDs for advanced packaging applications.

Key words: Solid Solder Deposits (SSDs), Ball Grid Arrays (BGAs), Chip Scale Packages (CSPs), Interconnects, and Surface Finishes.

Background

The SSD process is comprised of three steps:

1) Solder paste print using conventional methods;
2) Reflow/formation of the metal deposits using equipment licensed specifically for this purpose;
3) Cleaning in the event that a water-soluble solder paste is employed.

In the SSD process a very rudimentary paste printer is employed for products as dense as .008" pitch. Much of the skill and accuracy required in conventional processing is not required in SSD processing, for a number of reasons:

a) The stencil used in the SSD process is normally .004" thick with increased apertures, or an overprint. Most assembly sites use a .006-.008" foil. This makes the SSD paste printing process much more repeatable due to the aspect ratio of the apertures on the stencil vs. the foil thickness.
b) While the viscosity of solder paste for conventional processing is thick and difficult to print (i.e. 850 KCPS), solder pastes used in the SSD process are typically 600 KCPS and this, in combination with the flux carrier employed, makes the paste quite runny.
c) Registration in the SSD process is not critical. Visual alignment by the operator is normally done even on high-density designs, obviating the need for optical registration systems. Misregistration or shorts evident after paste printing are eliminated during solder reflow and formation, as described further below. This provides more process latitude than conventional paste printing.

Subsequent to paste print, panels or arrays are loaded into the Reflow/Formation System. A tensioned stainless steel mesh is lowered directly onto the panels or arrays, with the mesh sitting in intimate contact with the wet paste. A hot air knife then travels over the boards in the SSD System. The traveling heat source is designed to insure a very brief thermal excursion. While solder paste manufacturers normally recommend a reflow stage of 30-90 seconds for eutectic solder at a temperature of 180-235°C, in the SSD process time at temperature is normally less than 20 seconds. The flux carrier used in the paste, and the absence of components during solder formation, both facilitate rapid reflow.

The mesh used in the SSD process acts as a die or mold to flatten (planarize), shape and remove excess solder. During reflow the solder wicks towards the land and up through the mesh. Alternatively, solder spheres (or bumps in wafer bumping) can be formed with the mesh screen acting as a conduit for excess solder to rise and be removed.

The mesh controls solder in the Z axis and enables volatiles present in the solder paste to escape during reflow and SSD formation, which occur simultaneously. Excess solder wicks above the mesh during reflow in the form of solder balls. Even if excess solder re-deposits on the boards after many cycles, i.e. on the surface of the solder mask, it is easily removed in the absence of components. (Note that the mesh is normally cleaned one time per shift to remove residual solder balls.)

In the SSD method described the solid solder deposits have a macro-planar surface finish with an embossed surface topography created by the mesh screen. This "textured" finish creates a larger surface area to retain a high volume of tack flux at subsequent assembly. Further the conduit created by the mesh enables the solder to be formed without voids. After reflow panels or arrays are quenched with a lower temperature-cooling pass and boards exit the Reflow/Planarization system.

In the event that a water-soluble solder paste is used flux residues are removed with conventional equipment. Cleaning at 130°F using a mild saponifier will remove flux residues or residual solder balls formed during planarization. Residue removal is much less difficult without components obstructing spray patterns. Cleaning lines employed include batch processing, industrial dishwashers and conveyorized systems. Ionic tests can be performed to insure cleanliness levels meet end user specifications. While panels or PCBs coated with dry films retain more residue than their liquid photoimageable counterparts, both typically measure ≤ 01.0 µg.NaCl/Sq. In. of contamination when tested with an ionographic unit at ambient temperature.

PCB Capabilities/Design Considerations

The wire-mesh screen process provides a very defined volume of solder, which cannot be accomplished with normal stencil printing. Shorts and solder balls at assembly are eliminated and the copper lands are encapsulated in a thick solder deposit which increases bare board shelf life.

The most common products processed with SSDs are double sided surface mount within the parameters reflected in Table 1. Other design considerations on the board level include:

1) Vias immediately adjacent to sites that require a solder deposit should be plugged or tented with solder mask to prevent solder from wicking into the vias;
2) Two lands connected to one another that require solder deposits of varying heights, or different alloys, should be isolated by a solder mask web

Depending on the board fabricators capabilities there may or may not be solder mask dams or webs between surface mount lands. BGA sites are normally non-solder mask defined due to thermal cycling performance.

Table 1 - Solid Solder Deposit Capabilities/Design Considerations

Maximum Substrate Size	18" x 14"
Minimum Substrate Size	1" x 1"
Substrate Construction	FR-4, polyimid, ceramic, flexible circuits, wafers
Solder Mask	Liquid Photoimageable, Dry or Liquid/Dry Film
Cu Finish	HASL, Organic Coating, Gold, Nickel/Gold, Immersion Tin, Immersion Silver, Selective Solder
Board Thickness	.010" to .250"
Tooling Holes	.125" x 2 Recommended
Solderability	Mil P55110

Alloy Composition/Lead Free Alloys

SSDs are processed with a number of different alloy compositions to meet end users diverse requirements. While eutectic 63/37 solder is most commonly used for conventional surface mount applications, lead free solders have gained momentum and high lead content alloys are used for some advanced applications (i.e. wafer bumping and the formation of solder spheres on ceramic components).

Contingent on PCB design multiple alloys may also be recommended where it is desirable to have two-tiered deposits reflowing at different temperatures. Multi-tiered deposits can be particularly advantageous in loading edge connectors through multiple soldering operations. Table 2 reflects some of those alloys most commonly used in SSD formation. It should be noted that nitrogen is recommended for reflow of high lead content alloys.

Table 2 - SSD Alloys

Alloy	Melting Range °C	Element Key
Sn63Pb37	183	Sn – Tin
Sn62Pb36Ag2	179-189	Pb-Lead
Sn96.5Ag3.5	221	Ag-Silver
Sn43Pb43 Bi14	144-163	Bi-Bismuth
Sn95Ag5	221-245	
SnAg3.8Cu.7	217-221	

Note: Numbers represent the weight percent of the element that is included in the alloy.

Solder Volume/Deposit Height

A number of studies have been done to determine desirable solder volume and height for various component configurations. While some data is presented here, it is important to note that the end users existing solder paste print criteria may be the best method of determining acceptable volume for a specific application. If normal paste print is accomplished using an .008" stencil foil with a 1:1 image with the copper land, and approximately 50% of the paste volume printed is flux that is volatilized during reflow, this converts to the equivalent of a .004" macro-planar solid solder deposit height.

Table 3 - SSD Volume - Conventional SMD

	Volume/Cubic Mils Per Lead
BGA	1900-1950
PLCC	4000-6100
QFP	1800-1900
SOIC	4000-5700
TSOP	1400-1800

Uniformity of deposits across large surface areas is maintained within fairly tight tolerances. The average solder deposit thickness reflected in Table 4 was measured using Laser Thickness Measurement, which may be more reliable than other measuring devices due to the crosshatched surface of the deposits. For thin deposits, i.e. .0008" SSDs required on .009" pitch medical devices, it is important to insure that the measurement device/method does not skew the results due to the peaks and valleys of the solder deposits.

Table 4 - SSD Thickness/Uniformity Conventional SMD

	Range	Uniformity
BGA	.0019-.0025	± .0003"
PLCC	.0019-.0029	± .0002"
QFP	.0019-.0024	± .0002"
SOIC	.0019-.0029	± .0002"
TSOP	.0019-.0022	± .0002"

An ancillary benefit of employing SSD "flat pads" on the bare board may be the increase in deposit height as the solder reaches a meniscus during subsequent reflow at assembly. This height increase, reflected in Table 5, has been attributed to compensating for up to +/- .007" of lead coplanarity defects.

Table 5 – SSD Meniscus Height Increase (with Conventional SMD)

Pitch	SSD Height	After Reflow	% Increase
.050”	.0035”	.0050”	42%
.031”	.0035”	.0045”	28%
.025”	.0035”	.0045”	28%
.019”	.0033”	.0041”	24%

Solder Deposit Planarity/Sphericity

While SSD flat pads are common on the board level, semiconductor wafers are normally bumped, and solder spheres are formed on components (i.e. BGAs) using modifications of the SSD process.

Planarity specifications vary due to a number of criteria including board design, land configurations, pitch, buried vias in the pads or vias connected to the pads which can effect solder volume, as well as alloy. Further it is common for deposits to have a "shoulder" as depicted in Figure 2.

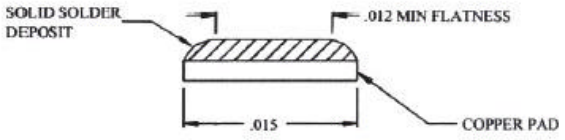

Figure 2 – SSD Planarity Specification

For one end user manufacturing a coaxial cable assembly (Figure 3) a .005" deposit height was specified for a particular pad size (approximately .050" x .015"). Pad planarity was critical for efficient placement of a connector without component skew. A planarity specification of .012" minimum flatness, or 80% of the surface area, allowed for up to +/- .006" of leg misalignment in the lateral direction. The principal advantage of SSD over conventional paste printing for this application was the elimination of solder smear, which occurred during connector placement using conventional assembly methods. With SSD the component sits on the center of the solid solder pad with an equal amount of solder in front of and behind the pin, achieving a symmetrical solder fillet.

As with the comparison of paste print parameters for flat pads vs. conventional processing, SSD formed spheres should meet the end-users current criteria for solder ball placement. Conventional metallization in the manufacture of Ball Grid Arrays (BGAs) and Chip Scale Packages (CSPs) is the placement of solder balls on the package to form the interconnection between the component and the printed circuit board. Assembly yields are sensitive to ball height variations across an array, and solder spheres should be uniform and exhibit minimal oxides. The majority of solder balls being placed are between .028" to .035" in diameter with uniformity required of +/- .001". SSD formed spheres are most common between .012" and .030" in diameter.

Figure 3 – Micro Coaxial Cable Interconnect

While implementation of SSD technology on the board level was driven primarily to improve first pass yields, on the package level the primary advantage is to reduce raw materials costs. Rather than placing solder balls on an array, the SSD process uses solder paste as the medium to form spheres. This represents a significant capital equipment and materials savings. SSD technology also eliminates the requirement to use nitrogen when forming Sn63/Pb37 solder spheres, providing further cost benefits.

Ionic Cleanliness

Ionic contamination can represent a significant factor causing degradation or failure of electronic assemblies. Residual contamination can result in surface electrical leakage and chemical, galvanic and electrolytic corrosion. It is important to quantify contamination levels to insure that all products perform to there intended level.

Many of the problems associated with ionic contamination at assembly have been reduced due to changes in solder mask materials. Dry film resists used many years ago were porous and prone to retaining high levels of contaminants which could contribute to white hazing, blistering and a high incidence of solder balls at assembly. Liquid photoimageable (LPI) solder masks exhibit fewer contaminants and are now used in the manufacture of most PCBs (i.e. over 90% of circuit boards processed in the U.S. are produced with LPIs).

A common method of testing ionic contaminants is measuring the electrical resistivity of a known volume of rinse solution used to extract and remove the ionizable contaminant off a known surface area. An ionographic unit can be used to test for contamination of boards after SSD processing and cleaning. With a Pass/Fail limit of 6.4 µgrams/square

inch results insure that all boards fall well within acceptable levels.

Table 6 - Ionic Contamination Results

Dry Film A	01.0 µgNaCl/Sq. Inch
Liquid Photoimageable A	00.0 µgNaCl/Sq. Inch
Liquid Photoimageable B	00.0 µgNaCl/Sq. Inch

Assembly Process

The assembly process is simplified with the implementation of SSDs. An adhesive flux is applied to boards prior to assembly via stencil, spray, immersion, dispensing or by pin transfer.

Flux chemistries available include no clean, water-soluble and rosin based formulations. If a water soluble flux is selected it can be dispensed in beads across a row of pads to improve line efficiency and reduce cycle times.

Subsequent to application of the flux components are placed followed by conventional reflow soldering. The flux activates the solder and has sufficient tack properties to prevent component movement during assembly. The reflow profile used is normally determined by the profile of the correspondent solder paste that contains the same paste flux. Following reflow products are inspected and tested.

When qualifying the SSD process the assembly sites inspection and test should include verifying the wetting angles of the solder joint, insuring a very thin intermetallic layer between the solder and the copper pad and analyzing alloy composition. (See Figure 4.)

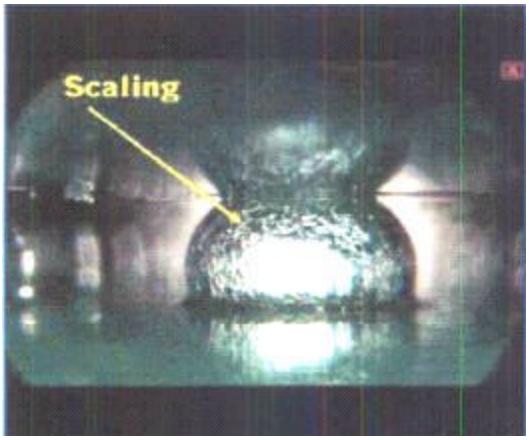

Figure 4 - mBGA Sphere Photograph at 100x Magnification

Summary

The trend towards finer pitch surface mount devices has accelerated over the past decade. At the same time prices for consumer electronics in particular have experienced continuing downward pressure. This has resulted in the electronics industries assessing different methods to increase manufacturing yields and to effectively reduce costs. While margins have eroded in some sectors, the cost of environmental compliance has risen. In response to this market pressure electronics manufacturers have increasingly looked at ways to remain competitive.

SSD technology has evolved to meet a number of different application requirements. Several iterations were developed and include deposits for applications including flip chip designs (.001" SSD on .009" pitch) as well as forming .040" deposits for mechanical connections. The technology can benefit low-density computer applications, mid-density medical, test and measurement and telecommunications (mobile phones and satellites), and the highest density products currently manufactured for data processing, components and consumer electronics. They are employed in the manufacture of PCMCIA cards, flight data recorders, connectors and military electronics.

Since their introduction in the early and "mid-1990's," SSDs have been subjected to rigorous proprietary testing by a variety of end users. These have included reliability testing with respect to thermal and power cycling, solderability and vibration. A number of major advantages have been identified using SSDs over conventional processing. In addition to providing excellent planarity/uniformity of the metal deposits prior to assembly, SSDs

- Lower costs compared with processes currently used;
- Reduce the defect rate of the solder connections;
- Is well suited to high density devices;
- Less complex than traditional methods;
- Reduces cycle time at assembly and improves line efficiency;
- Significantly enhances long term reliability of electronic assemblies;
- Is environmentally friendly.

SSD technology provides significant advantages over conventional processing and accelerates the introduction of new products into the marketplace using the electronic industries existing infrastructure.

References

- Palumbo, K., "gBGA's Solder & Oven Profiles - Critical Process Variables", SMTA, June, 2001.
- Burr, D., "Solder Paste Printing Guidelines for BGA and CSP Assemblies", SMT Magazine, January 1999, pp. 70-74.
- AMP Application Specification 114-110004, "MICTOR Connectors for Surface Mount Technology (SMT) Printed Circuits (PC) Board Applications", 1999.

- Mawer, A., "Array Package Attachment Reliability", Binghamton University - 7`" Annual Electronics Packaging Symposium.
- Prinz von Hessen, W., "CSP and DCA in Manufacturing" in Chip Scale Packaging and Large, Fine Pitch Direct Chip Attach Focus Group Meetings, March 31 and April 1, 1998.
- Holzmann, A., "Solid Solder Deposits (SSD): A Bare Board Solution for high Density Packaging", SMI Advanced Electronic Manufacturing Proceedings, September 10-12, 1996, pp. 559-564.