C4NP Lead Free vs. Electroplated High Lead Solder Bumps

Jayshree Shah
IBM Microelectronics,
Hai P. Longworth & David Hawken
IBM Microelectronics,
Eric Laine & Klaus Ruhmer
SUSS MicroTec, Inc.

ABSTRACT
There are various C4 (Controlled Collapse Chip Connection) solder bumping technologies used in volume production. These include electroplating, solder paste printing, evaporation and the direct attach of preformed solder spheres. FlipChip in Package (FCiP) demands many small bumps on tight pitch whereas Wafer Level Chip Scale Package (WLCSP) typically requires much larger solder bumps. All these technologies have limitations for fine pitch bumping. The most commonly used method of generating fine-pitch solder bumps is by electroplating the solder. This process can be costly, especially when it comes to lead-free solder alloys. These challenges in the transition to lead-free solder bumping has led the European Union to grant exemptions from the ban of lead in certain solder bumping applications. However, the second level assembly cost of Lead-Free and Leaded line in parallel is driving for a commonality to move to lead-free for the entire industry.

The terminal metals process forms C4 (Controlled Collapse Chip Connection) solder bumps and the associated bump limiting metallurgy pads on the surface of silicon integrated circuit wafers. The Bump Limiting Metallurgy (BLM) or Under Bump Mettalurgy (UBM) pads are located between each solder bump and the surface of the wafer. Typically, the wafers contain a replicating pattern of chips / die. The UBM and C4 solder bumps provide an electrical and mechanical connection for the chip to its first level package

C4NP (C4-New Process) is a novel solder bumping technology developed by IBM and commercialized by Suss MicroTec. C4NP addresses the limitations of existing bumping technologies by enabling low-cost, fine pitch bumping using a variety of solder alloys. C4NP is a solder transfer technology where molten solder is injected into pre-fabricated and reusable glass templates (molds). Mold and wafer are brought into close proximity and solder bumps are transferred onto the entire 300mm (or smaller) wafer in a single process step. C4NP technology is capable of fine pitch bumping while offering the same alloy selection flexibility as solder paste printing. The simplicity of the C4NP process makes it a low cost solution for both, fine-pitch FC in package as well as large pitch / large ball WLCSP bumping applications.

This paper provides a summary of manufacturing and reliability results of C4NP Lead-Free bumps and compares it with the Electroplated High Lead solder bumped high-end logic devices. We also discuss the relevant process equipment technology and the requirements to run a HVM (high volume manufacturing) C4NP process. We will also describe the C4NP manufacturing cost model and elaborates on the cost comparison to alternative bumping techniques. The data in this paper is provided by IBM's packaging operation at the Hudson Valley Research Park in East Fishkill, NY

INTRODUCTION

Many new electronic packaging applications are pushing the limits for weight, size, reliability, cost and high speed performance. At the same time, environmental considerations are driving new material requirements. These factors are driving a migration from wire bond to flip chip as the preferred method for connection from the semiconductor chip to the chip carrier or printed circuit board, and from Leaded to Lead-Free packages. Wafer bumping is becoming more pervasive, and several bumping processes have been established, each with different strengths.

Earlier work has shown that Injection Molded Solder techniques have the potential to effectively address the challenges of wafer bumping. Realizing these benefits in production requires an integrated tool set that can support increasingly demanding manufacturing requirements. This paper reports a comparison of new Lead-Free SnCu and SnAg solder C4NP with current electroplated leaded 97Pb3Sn solder C4.

C4NP VS. ELECTROPLATED C4 PROCESS FLOW

The C4NP process starts with a glass mold in which the bump pattern for an entire wafer is replicated as a mirror image of cavities in the glass mold. These cavities are filled with solder as the mold is scanned below a fill head. The fill head contains a reservoir of molten solder and a slot through which the solder is injected into the mold cavities. The cavity depth and diameter determine the volume of the solder bumps that will be subsequently formed on the wafer. The filled mold is inspected automatically and then aligned below a wafer with exposed UBM pads facing the mold. Mold and wafer are heated above the solder melting point and then brought into contact. The solder forms spherical balls which transfer from the mold

to the UBM regions on the wafer, where they preferentially wet and solidify. Wafer and mold are separated, and the mold is cleaned for reuse. Figure 1 describes this process flow.

C4NP molds are formed using borofloat glass plates, which have a coefficient of thermal expansion (CTE) close to silicon wafers. Photolithography is used to pattern and etch cavities whose diameter and depth precisely determine the volume of the solder bump, as well as defining the bump pitch and location. The molds are scanned beneath a solder injection head which fills the cavities with liquid solder precisely to the surface of the mold. Therefore, the solder volume transferred to the wafer is directly a function of the glass cavity volume.

The solders used for wafer bumping do not wet to the glass mold, so upon heating, the solder alloys form spherical balls in the cavities, as described in Figure 2. The reflowed balls protrude above the surface of the mold by 10 – 20 um depending on ball size and cavity. Note from Figure 2 that the balls are not uniformly formed at the center of the mold cavity. The alignment of the mold cavities to the corresponding UBM pads is sufficient to assure that the solder wets to the correct UBM pad.

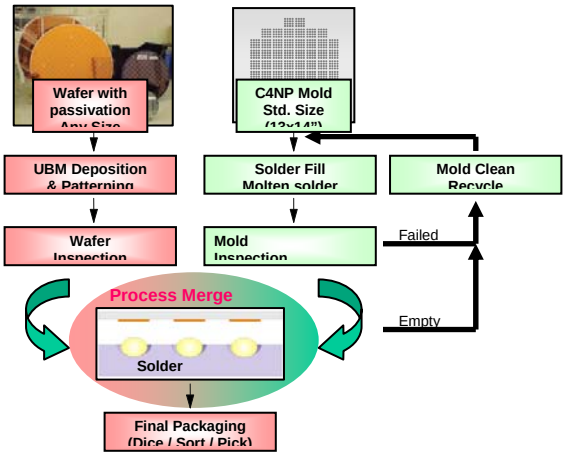

Figure 1 - C4NP Process Flow

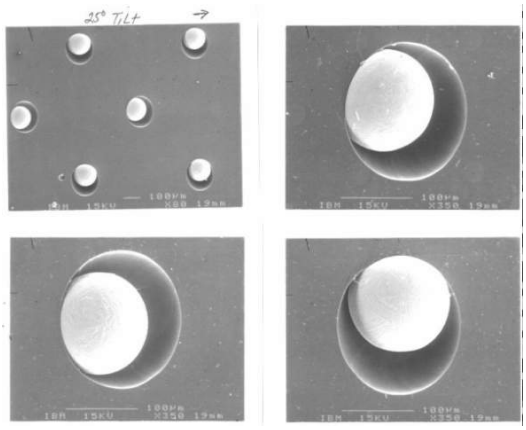

Figure 2 - Reflowed solder spheres in glass mold cavities prior to transfer to wafer.

The filled molds are aligned with the wafer as shown in Figure 3. After alignment, the mold and wafer are heated and are brought into close proximity/contact, allowing the molten solder balls to wet the appropriate UBM pads where they preferentially remain when the wafer and mold are separated.

The solder transfer process takes place in a reducing gas environment which assures clean, oxide free, solder and UBM surfaces and avoids the need for liquid flux and subsequent cleaning. After solder transfer, the wafers are ready for test, dicing and subsequent packaging.

In the electroplated C4 process, C4s are electroplated in the photoresist opening on top of exposed UBM. After stripping the photoresist material, wafers are reflowed at solder melting temperature in an oven. Figure 4 describes this process flow.

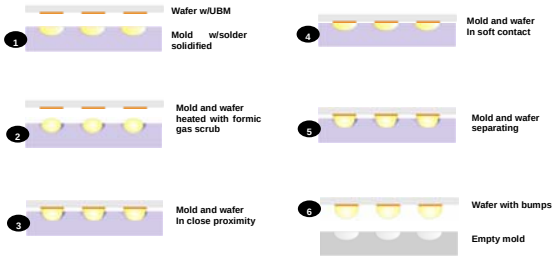

Figure 3 - Solder transfer process sequence.

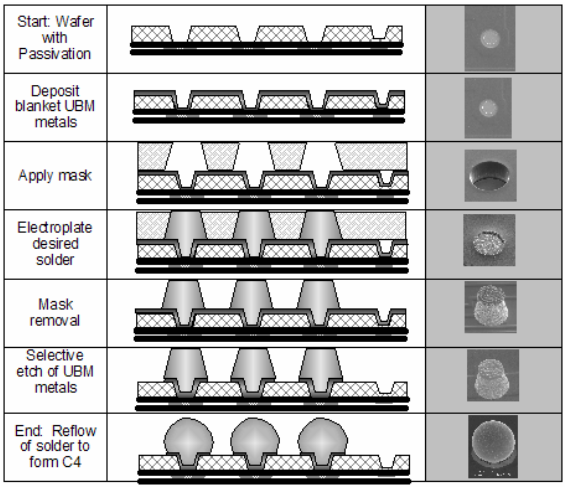

Figure 4 - Electroplated C4 Process Flow

HVM of C4NP

For HVM (High Volume Manufacturing), the C4NP toolset includes a solder transfer cluster tool and mold stocker to support a production rate of 300 wafers per day (WPD) of 300mm or smaller wafers. Production rates for C4NP are independent of wafer size.

C4NP VS. ELECTROPLATED C4 COST

The per wafer cost for production wafer bumping is a function of the following cost determining factors:

A: Personnel cost
B: Consumable and material cost
C: Equipment maintenance and support
D: Equipment depreciation
E: Building overhead (footprint, clean room)
F: Wafer yield
G: NRE cost per part number/bump pattern
H: Chemistry supply and waste treatment
I: IP cost/IP wafer toll

As part of this work, a sophisticated cost model has been developed to compare the cost of C4NP wafer bumping with electroplating of solder. By modeling a variety of cases, C4NP has emerged as the lowest cost fine pitch flip chip bumping technology.

One of the most critical differences between C4NP and alternative bumping technologies is the use of molds. A minimum number of molds are required depending on the number of wafers per day with a particular bump pattern. The cost of molds directly impacts the per wafer bumping cost. It is therefore critical for C4NP equipment technology to minimize the number of molds needed. Also, the number of reuses of a given mold is critical in determining bumping cost.

It is reasonable to assume that molds can be used several hundred times. It is beyond the scope of this paper to provide actual per-wafer costs. The numbers depend on the individual company information which is often considered proprietary. However, the various cases which have been investigated show a per wafer cost reduction by using C4NP instead of electroplating. The "per wafer cost" reduction accomplished by C4NP ranges from approximately 10% to 30%.

The major advantage of C4NP process is in the flexibility of choice of solder. By replacing the mold fill head with choice of solder, Lead-Free vs. Leaded C4, in a variety of alloys can be manufactured with same sets of tools. Alpha particle emission which is directly related to impurities of the solder material is easily controlled in C4NP process. As waste of solder material is very low compared to electroplated process, there is an added benefit of expensive material cost saving for Low Alpha.

LEAD FREE C4NP VS. LEADED ELECTROPLATED C4 RELIABILITY

Lead-Free solder bumping has been one of the most important drivers for new bumping technologies such as C4NP. Lead-Free bumping is also impacting the choice of the UBM stack-up. Since Lead-Free solders typically have a high Sn content, such as Sn2.0Ag and Sn0.7Cu, they are consequently highly reactive with Cu. There are several ways of addressing this issue, one of which is by using electroplated Ni as a barrier layer. C4NP is compatible with any solder wettable surface, including Cu, Ni and Au. The UBM construction and the solder deposition method are two major contributing factors in package reliability.

Manufacturing data for 300mm wafers bumped using C4NP with Lead-Free solders and electroplated Leaded solder and a Ni plated UBM has been collected. Figure 5 depicts the chip test vehicle used to collect 200 um pitch manufacturing and reliability data.

Test Vehicle Description

We use a specially designed test chip to evaluate C4 reliability. There are 3 main test features for C4 evaluation. To monitor C4 fatigue behavior, we use a ring connection of signal C4s to enable the testing of C4 failures at different DNP (distance to neutral point). Migration ring consists of 3 parallel C4-stitch pattern is used to evaluate C4 migration/corrosion by biasing the center ring against the two neighbor rings. There are 4 electromigration (EM) test sites The EM design allows 4-point C4 resistance measurement of the stressed C4 along with a thermal sense and short monitor.

- Chip size: 14.67 x 14.76 mm
- Pitch: 200um
- Wafer size: 300mm
- # of Chips in wafers: 271
- # of C4's in chip: 4,699
- Total C4s in wafer: 1.27 million
- Chip technology: 90 nm
- Package: FC-PBGA
- Solders: 1.) Leaded: 97Pb-3Sn with eutectic cap 2.) Lead-Free: Sn0.7%Cu & Sn2.0% Ag

Product construction

The following product construction was used for the reliability test:

1.)Transfer Technology

- UBM: Sputtered TiW / Cu, Plated Ni / Cu
- C4: Sn0.7Cu and Sn2.0Ag

2.)Electroplated Technology

- UBM: Sputtered TiW / CrCu / Cu, Plated Ni
- C4: 97Pb-3Sn

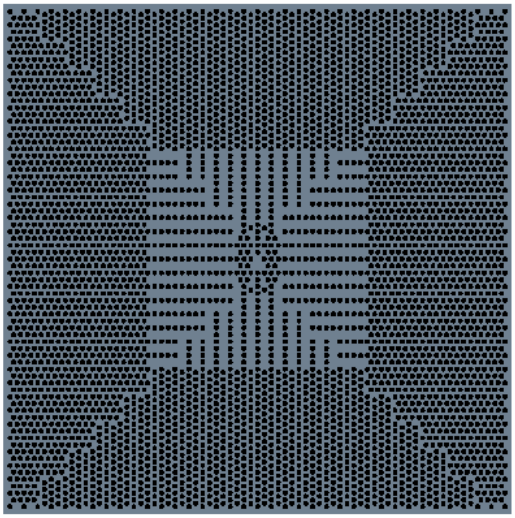

Figure 5 - 200 um pitch test vehicle C4 pattern.

Integrity Evaluation
Extensive evaluation was performed on multiple processing lots to evaluate both C4 and under fill integrity.

1. Tensile Strength and Fracture mode
To evaluate the solder joint strength of Lead-Free C4NP transferred bumps compared to Leaded plated bumps, a series of bump tensile tests have been performed. A stud is glued on back side of the assembled chip on FCPBGA package. Chip is pulled away from the package at constant speed at room temperature until joint is separated.

Lead-Free alloy is stiffer giving higher average tensile chip pull strength, but is no longer the weakest link as in Leaded solder. Fracture mode as a taffy pull in Leaded C4 is not an always case in Lead-Free C4. Tensile chip pull test is useful in Leaded C4 to find problems in UBM.

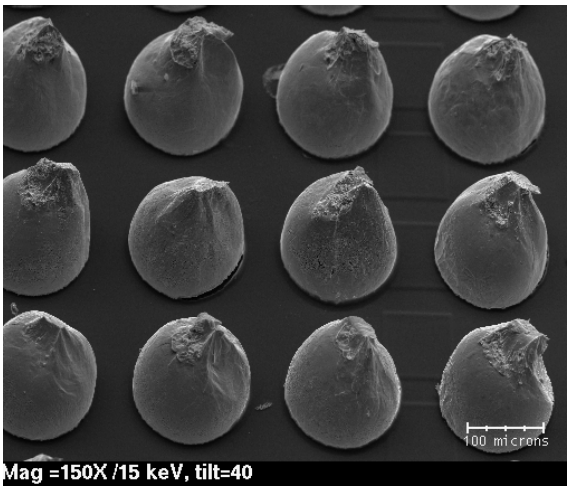

Figure 6 - Taffy pull in Leaded C4

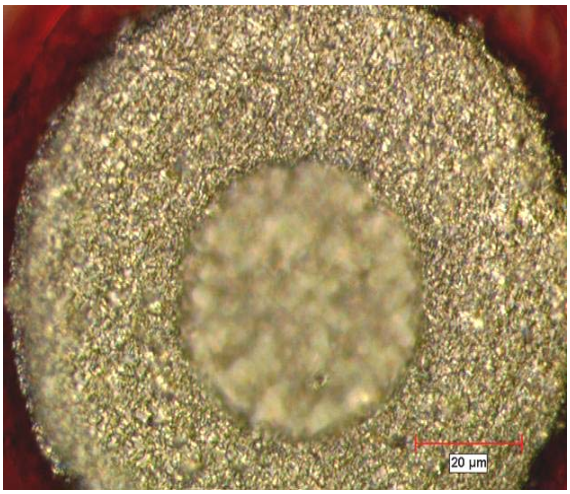

Figure 7 - Rupture in UBM in Lead-Free

2. Solder voids
One of the concerns of any solder deposition technology is the formation of voids at fabrication which may expand and grow during subsequent reflows. During the C4NP fabrication, wafers are routinely inspected for voids by X-Ray in nine locations, approximately 50 C4 bumps per location. To date no voids of any size have been found. This is to be expected, since C4NP uses solid solder alloys that are melted and subsequently transferred to wafers. There is no conversion of the solder to a paste containing flux or to a plating chemistry, so there is no evolution of organics or trapped gasses during reflows. A sample of qualification wafer data is found in Table 1.

Table 1: x ray void inspection data

300mm C4NP Xray Void Data Sheet
FOUP: 25856

QTY: 6 Date: 3/10/06 Inspector: Bobby Henry

Slot	Lot ID	Wafer ID	Zone 1		Zone 2		Zone 3		Zone 4		Zone 5		Zone 6		Zone 7		Zone 8		Zone 9	
		Level	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg
1	05409FTA001.007	90RBX007SJH0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	05409FTA001.010	90RCN165SJB6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	05409FTA001.000	90RCN164SJE7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	05409FTA001.000	90RCN160SJC5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
23	05409FTA001.000	90RCN159SJG7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	05409FTA001.000	90RCN158SJC5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

300mm C4NP Xray Void Data Sheet
FOUP: 9234

QTY: 4 Date: 3/11/06 Inspector: Dave Drotar

Slot	Lot ID	Wafer ID	Zone 1		Zone 2		Zone 3		Zone 4		Zone 5		Zone 6		Zone 7		Zone 8		Zone 9	
		Level	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg	Sm	Lg
14	05409FTA001.009	90RBX006SJC6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	05409FTA001.009	90RBX005SJF7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	05409FTA001.009	90RBX004SJB5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	05409FTA001.009	90RBX003SJE6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

3. Solder composition control

Solder composition for Leaded and Lead-Free C4 alloys plays a major role in package assembly and C4 joint reliability.

For PbSn solder, melting temperature changes drastically with change in % Sn. Plating bath control and actual C4 analysis using DSC (Differential Scanning Calorimetry) technique to find melt temperature is common to determine the solder composition for Leaded electroplated C4.

For SnCu or SnAg Lead-Free C4, the melting temperature range is very wide. DSC techniques do not help controlling C4 solder composition. C4NP process is a big advantage for controlling solder composition. C4 Solder composition is same as incoming solder alloy, filled and transferred.

4. Chip Coplanarity

The contributors to Leaded Electroplated solder bumps coplanarity are solder voids and uneven plating thickness.

The contributors to Lead-Free C4NP solder bumps coplanarity are mold cavity size tolerance and mold fill and clean efficiency.

5. Underfill Adhesion

Underfill integrity is an essential part of module reliability in packaging applications with high chip/substrate CTE mismatch and /or non-hermetic condition. Significant degradation in C4 fatigue life could occur in areas of poor adhesive bonding or underfill voids. For both Leaded and Lead-Free C4s, proper storage, shipping conditions and appropriate fluxes to remove either Pb or Sn oxides are critical to ensure good underfill adhesion. Lead-Free packages with its higher second level processing temperatures (245C or 260C vs. 225C) also require selection of appropriate underfill material

6. Reliability Stressing

Reliability evaluation encompassed standard JEDEC stress conditions (T/C, T/H/B, HAST, HTS, LTS) and several new stresses designed specifically to evaluate no-lead solders such as electromigration, tin whiskers and tin pest.

Prior to stressing, all test modules were subjected to JEDEC preconditioning level 3. The preconditioning consists of thermal shock (-40/60C, 5cyc), 24hrs baked at 150C, a soak at 30C/60%RH for 192 hrs to be followed with three 260 +-5 C IR reflows A subset of modules in each stress cell was subjected to Group B Preconditioning to simulate the worst case mechanical stresses the module must withstand during module/system assembly, shipment and installation. The Group B stresses include 1) Thermal shock (-40C to +60C, 10cyc, 30min dwell), 2) JESD22 B104-B (Shock) and 3) JESD22 B103-B (Vibration).

1. Fatigue

Both JESD22 A104 B thermal cycling conditions (0 to 100C and –55C to 125C) were used. These standard stress conditions require 1000 stress cycles. For comparison purpose, we extended the stressing to 3000 cycles for 0/100C and 1500cyc for -55C/125C. We also added no-underfill modules to the 0/100C cell and stressed them to failures to compare fatigue life of Leaded and Lead-Free C4s.

Our stress data indicated that Lead-Free C4s are more fatigue resistant than Leaded C4s. Both types of solder met JESD22 A104 B with no fails post 1000 stress cycles (Figure 8a and 8b). In the extended -55C/124C stress cell, Leaded C4s started to fail between 1250cyc and 1500cyc but there were no fails in both Sn0.7Cu and Sn2.0Ag post 1500cyc. There were no

fails in any solder system in the 0/100C cell with underfill up to 3000cyc. For the 0/100C cell with no underfill, as expected, many fails occurred within 300cycles with Leaded C4s cell has about 50% more fails than Lead-Free cells.

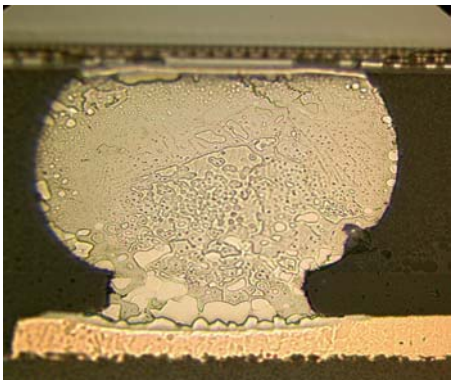

Figure 8a - X-section of PbSn C4 post DTC

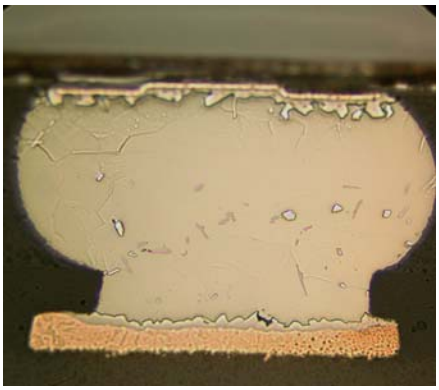

Figure 8b - X-section of SnAg C4 post DTC

2. Corrosion/Migration

T/H/B (temperature/humidity/bias) and HAST (highly accelerated stress test) were used to evaluate both C4 corrosion/migration and underfill adhesion. No fails were observed in all stress cells for all three alloyed systems. The results confirmed that with proper material selection and process control to ensure C4 integrity, corrosion and migration would not be an issue for any C4 types.

3. Electromigration

Establishing current carrying limit of no-lead C4s is a subject of great reliability interest due to application trend divergences for higher performance, higher power usage in high-density devices with tighter ground rule. To compound the problem, the replacement of Leaded C4s with no-lead solder may further reduce the current limit if the chosen material is less electromigration resistant than Leaded alloys.

Electromigration is a current-assisted atomic diffusion due to a momentum transfer from electrons to atoms in the presence of an electric field. It is scaled with a material melting point because the higher the melting point of a material, the higher its activation energy for diffusion. Using Mogro-Campero's estimate of electromigration time-to-failures (MTTFs) as a function of melting temperatures (ref. 4):

MTTF1/MTTF2 = EXP (7.4X10-4(Tm1-Tm2)/kT)

We estimated that Sn-Ag-Cu and SnCu C4s (Tm ~ 220C) would have 3x longer life than eutectic Sn/Pb (Tm ~183C) but 4x shorter life than 97Pb-3Sn (Tm ~ 320C) at the typical stress condition of 150C. These are simply rough estimates since even with identical geometry, factors such as grain size, grain size distribution, impurities, precipitation and intermetallics etc. can greatly influence EM behavior.

Our data to-date indicated that SnCu and SnAg are more electromigration resistant than eutectic solder but not as robust as 97Pb-3Sn. However, Lead-Free EM performance could be further improved with proper BLM material and geometry selection.

4. Metallurgical and underfill stability

High temperature storage (HTS) stressing at 150C for 1000hrs was used to evaluate both C4 metallurgical and underfill stability. Of particular interest is Kirkendall voidings which occur when Cu diffuses from UBM to react with Sn in the no-lead solders. Therefore, we added 170C HTS stress condition to 150C and extended the stressing beyond the standard 1000hrs up to 2000hrs. We also utilize both electrical measurement and physical characterization (x-sectioning) at stress intervals to monitor interfacial stability. There were no electrical fails in all stress cells. X-section image post 1000hrs at 170C showed no Kirkendall voids at UBM in both SnAg and SnCu C4s (Figure 9a and 9b).

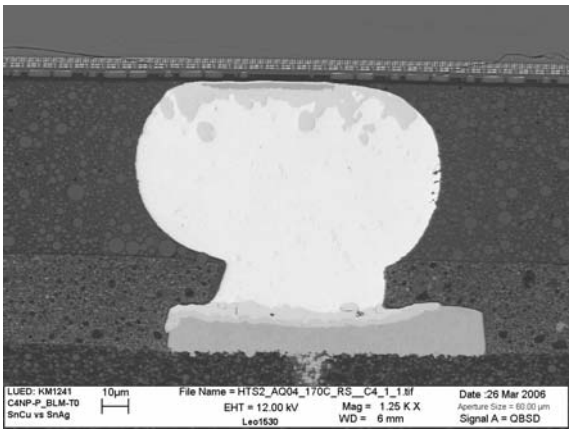

Figure 9a - HTS 170C/1000hrs Sn2.0Ag C4

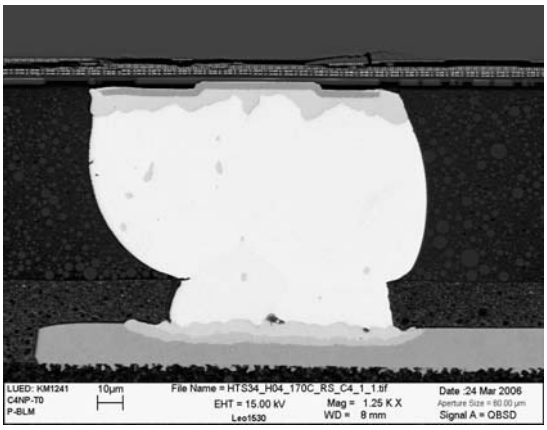

Figure 9b - HTS 170C/1000hrs Sn0.7Cu C4

5.) Tin Whiskers/Tin Pest

Tin whiskers and Tin Pest are reliability issues unique to Tin-based systems. These reliability risks associated with Tin are most likely to be lower in alloyed systems such as Sn-Ag-Cu and Sn-Cu than in pure Tin plating. These failure mechanisms are complex with multiple contributing factors such as thermal, mechanical stresses and impurities. Our approach is to evaluate these risk factors both in bare dies form and in module assembly subjecting thermal and mechanical stresses expected for product use condition such as multiple reflows, JEDEC PC, and group B

For tin whiskers evaluation, we employed two recommended Nemi stress conditions: T/C at 55C/85C, 1000cyc and T/H at 60C/93%RH, 1000cyc. We stressed bare dies and modules both with and without underfill with half under heatsink load and half without heatsink. At stress intervals, the samples were removed for electrical readouts monitoring for shorts, sonoscan of underfill modules and visual inspection of bare dies and no-underfill modules.

The allotropic transformation of white tin (β–Sn, tetragonal structure) to gray tin (α–Sn, cubic structure) at temperatures below 13°C to form tin pest is another reliability concern associated with Sn-rich, Pb-free solders. To address this concern, we extended the standard Low Temperature Storage (LTS) test at -65C over 1000hrs for Lead-Free C4s. Data to date showed no electrical fails post 1000hrs. Tin pest evaluation was also performed for combinations of bare dies, modules with underfill and without underfill. The modules were pre-stressed with JEDEC PC and group B then kept at –40C with periodic electrical measurement and visual inspection every 1000hrs. No fails were observed in either Sn0.7%Cu or Sn2%Ag alloy systems after 6 months.

CONCLUSION

The elimination of Leaded solder alloys for flip chip bumping has clearly become one of the most actively pursued technology solutions in the semiconductor packaging industry. IBM's C4NP bumping technology is enabling a new method of applying Lead-Free or Leaded solders on 300mm and smaller wafers. The use of bump molds allows the separation of the bumping process from the UBM process and enables the use of any solder. With this separation, bumping cycle time is rapid, since molds can be prepared in parallel with the UBM formation instead of sequentially. Since the solder is molten, the form factor is irrelevant. Bumping pitches from very fine flip to coarser WLCSP become possible with one cost effective process. The formation of entirely new solder or non-solder material combinations becomes possible with C4NP.

Lead-Free solder is stiffer and has lower melting point compared to High leaded solder. Lead-Free solder reacts quickly with UBM. Lead-Free C4s are more fatigue resistant than Leaded C4s. With proper material selection and process control to ensure C4 integrity, corrosion and migration would not be an issue for either Leaded or Lead-Free C4. SnCu and SnAg solders are less electromigration resistant than 97Pb3Sn but more robust than eutectic 63Pb37Sn. HTS Kirkendall voiding is not an issue for either solder types with proper UBM selection. No evidence of Tin whiskers or Tin Pest was found in Lead-Free Sn0.7Cu and Sn2Ag C4NP.

Manufacturing C4 using C4NP reduces many challenges for Lead-Free solder and is a less costly process with an equally reliable C4.

Acknowledgments

The authors would like to thank several colleagues at IBM for their contributions – Eric Duchesne, Luc Ouellet, Bill Bernier for Bond, Assembly & Test, Eric Kastberg and Joe Ross for reliability stressing, Eric Perfecto for technical contribution, and Chuck Goldsmith for F/A coordination and analysis.

Ref erences

1. J. Lau, Low Cost Flip Chip Technologies, McGraw-Hill Book, New York, 2000, Ch. 2, pp. 43-94.
2. P.A. Gruber, et al., "Low Cost Wafer Bumping", IBM J. Res. & Dev. Vol. 49 No. 4/5, July/September 2005.
3. B. Hochlowski, D. Naugle, P.A. Gruber, "Low Cost Wafer Bumping using C4NP", Future Fab Article, January 2005
4. A. Mogro-Campero, Simple estimate of electromigration failure in metallic thin films, J. App. Physic 53(2), 1224(1982)
5. K. Ruhmer et al., "C4NP: New Solder Bumping Technology – Low Cost and Lead-Free", IMAPS Flip Chip Advanced Technology Workshop, Austin, TX, June 2005.
6. D. Danovitch, P. A. Gruber et al., "IMS-Injection Molded Soldering", IMAPS 2000.
7. P.A. Gruber, DY Shih et al., "Injection Molded Solder Technology for Pb-Free Wafer Bumping", ECTC 2004.
8. K. Ruhmer et al., "C4NP: Lead-Free and Low Cost Solder Bumping Technology for Flip Chip and WLCSP", Pan Pacific conference 2006