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Bio

Terry Munson, founder and Senior Consultant of Foresite Inc. which has had the pleasure of serving the electronics fabrication, materials, assembly, and failure analysis needs of the industry for 20+ years. With the focus on Process Consulting, and chemical analysis of residues and their impact on product reliability. Terry has participated in many of the IPC committees and research groups for the last 23 years.

Title

QFN Flux Entrapment Case Study

Executive Summary

The presentation will discuss the problems that many QFN users are dealing with by having flux trapped under the component that is still gooey and conductive and the effect on circuit performance of sensitive circuits. The reason why the QFN traps show much flux and why the need for a standoff to lift the component off the board surface using soldermask and via plugging. This comparison will be evaluated using localized C3 steam extractions and Ion Chromatography analysis of the two conditions.

QFN Flux Entrapment Case Study

By Terry Munson

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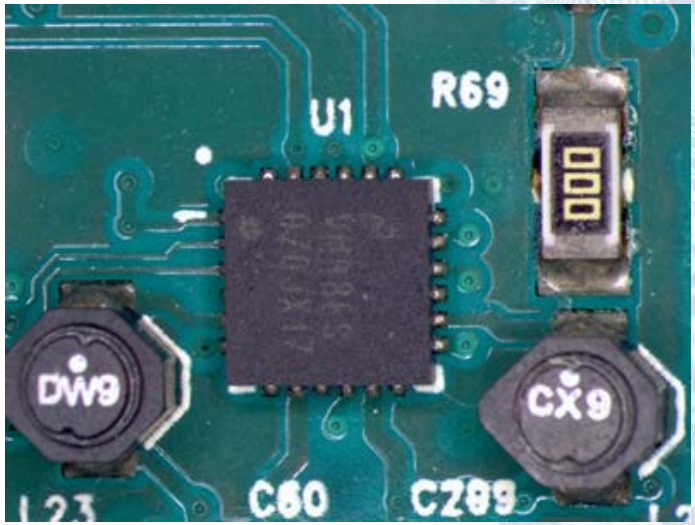
Foresite Inc.

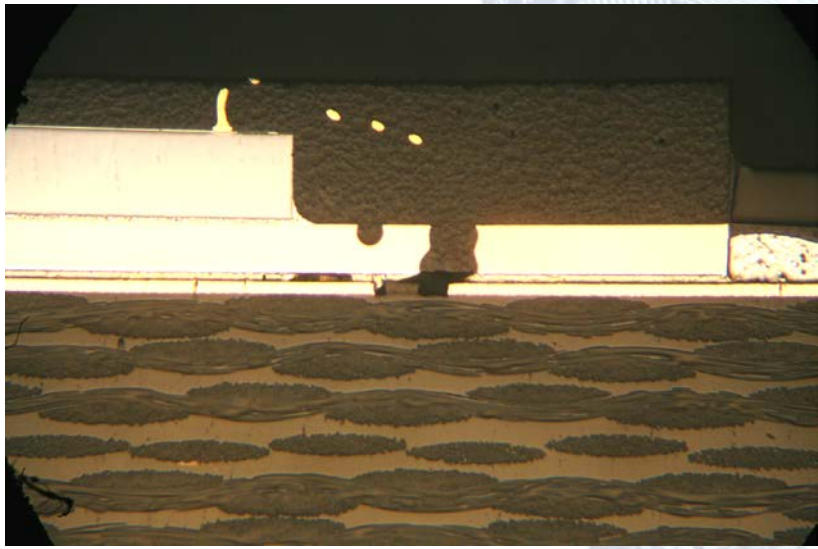
QFN Flux Entrapment

- In this case study on Quad Flat No-lead components we will compare no clean with and without soldermask standoff. The units without soldermask standoff (SS) showed poor leakage and units with SS showed good performance.

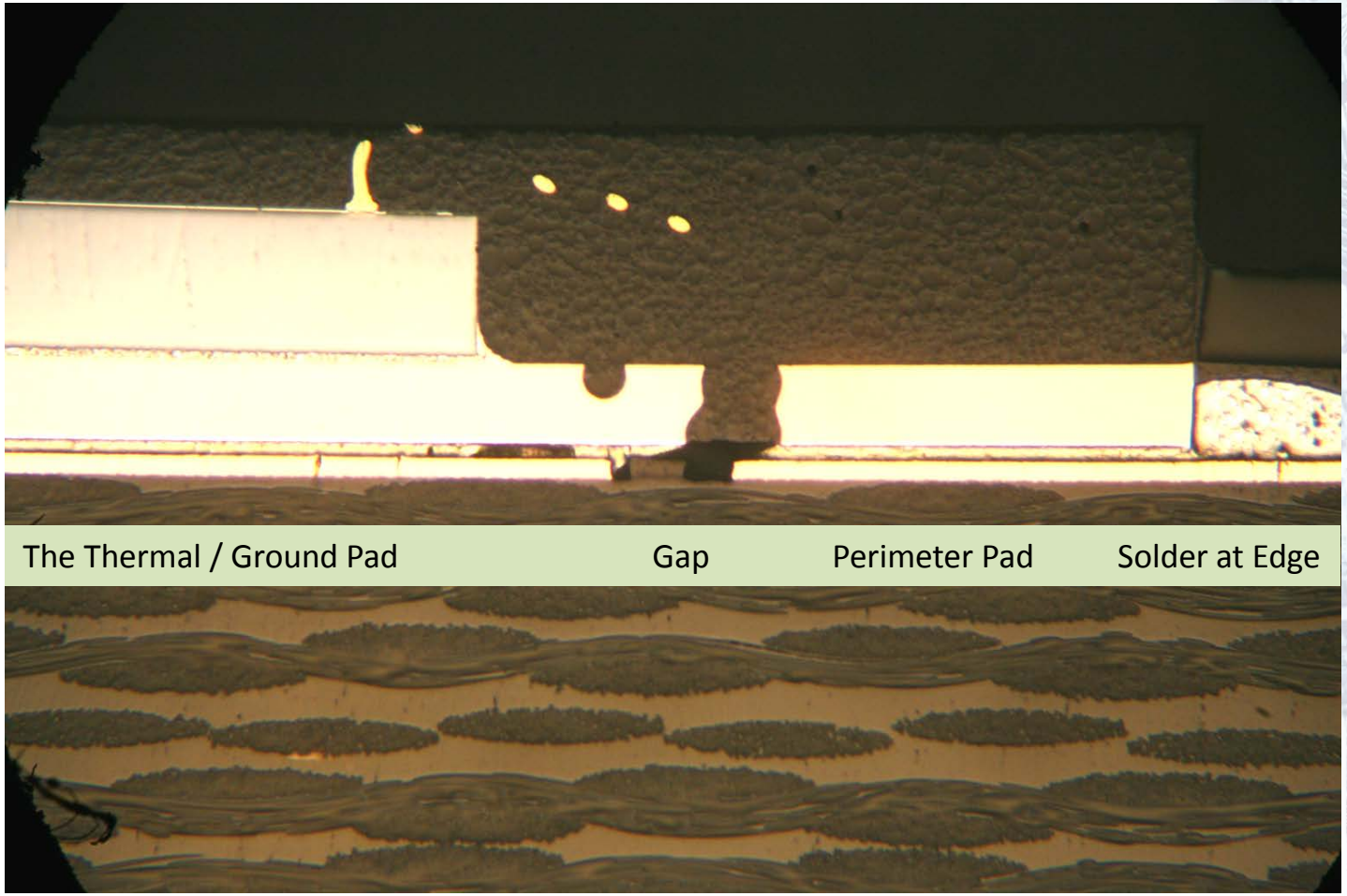


The problem with QFN's

- Many of components have a large heat sink on the base that covers more than ¾ of the component surface. This large thermal mass for conducting heat while the component is in operation.
- The cross section shows that the QFN has four key areas
  - Solder at the edge of the pad
  - Gap
  - Perimeter pad
  - Thermal / Ground pad



QFN Key Areas – So What!



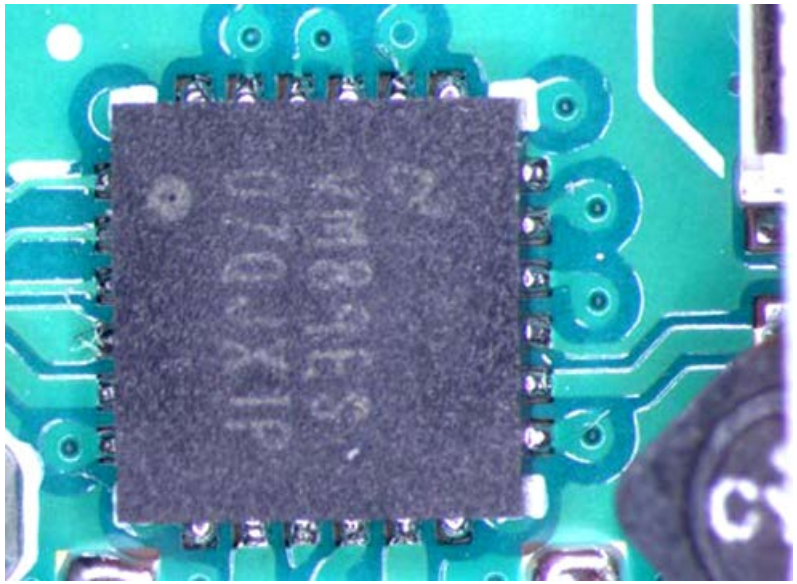
QFN Flux Entrapment Case Study #1

- A Satellite Uplink PCBA failing to communicate due to stray voltage at ambient conditions.
  - Historical component technology (DIP with heat sink) prior to the QFN package change never exhibited communication problems.
  - All QFNs samples with heat sinks and thermal vent are experiencing leakage and shorting problems.

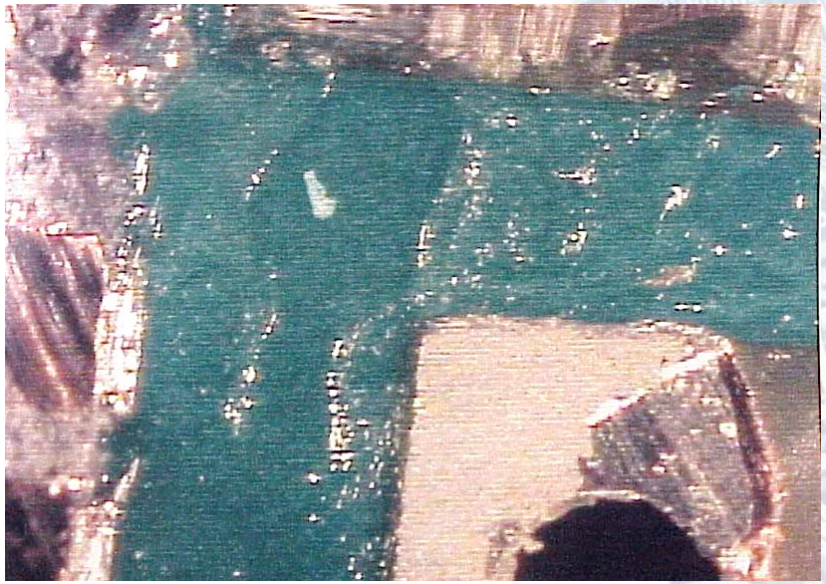
Background Assembly Conditions #1

- PCB is an FR-4 multilayer board with LPI soldermask with an ENIG board finish
- PCBA process is a no clean assembly with lead-free solder and lead free components
- Double pass reflow and selective solder connector attachment
- RF shield attachment by hand solder no clean

Images of QFN Flux Residues Below Component

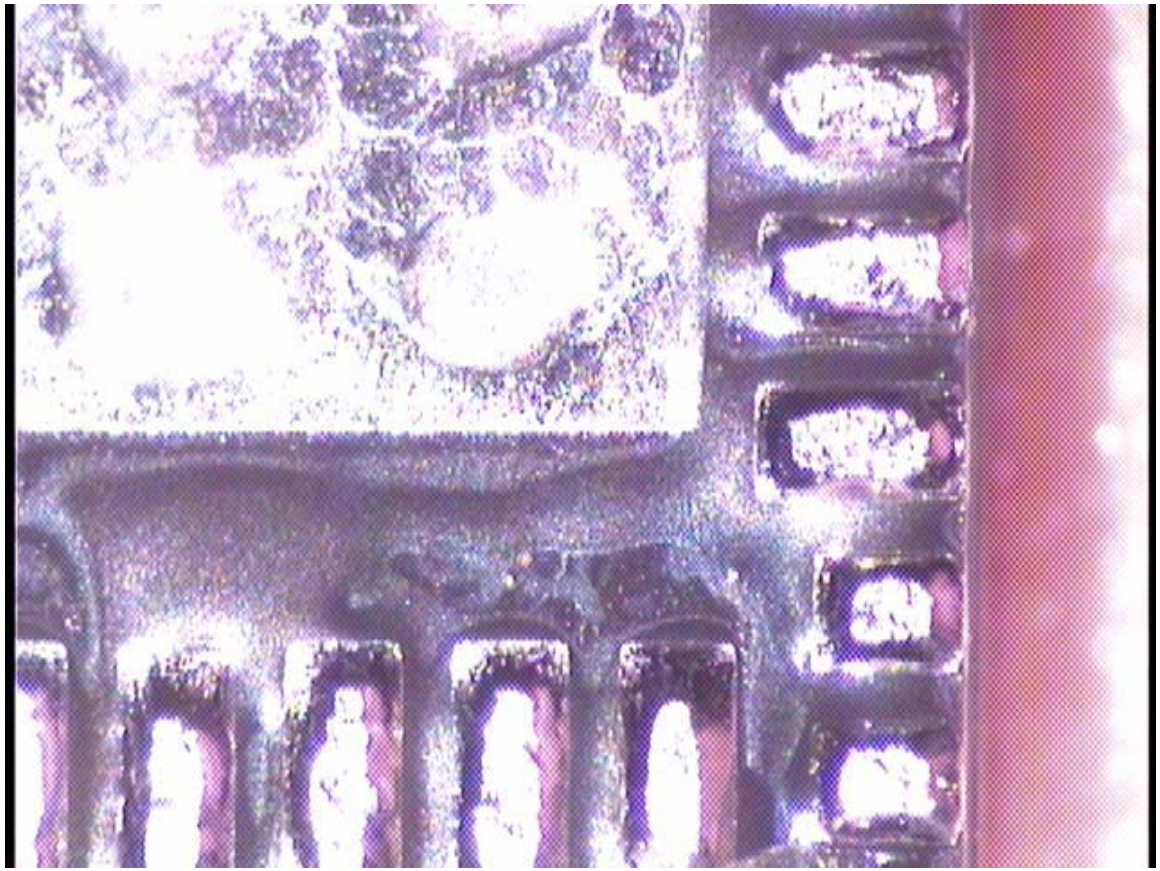


QFN top view

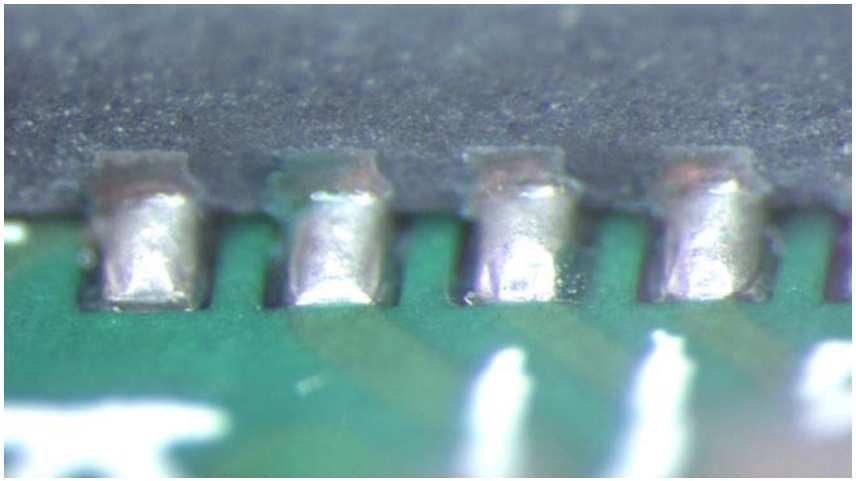


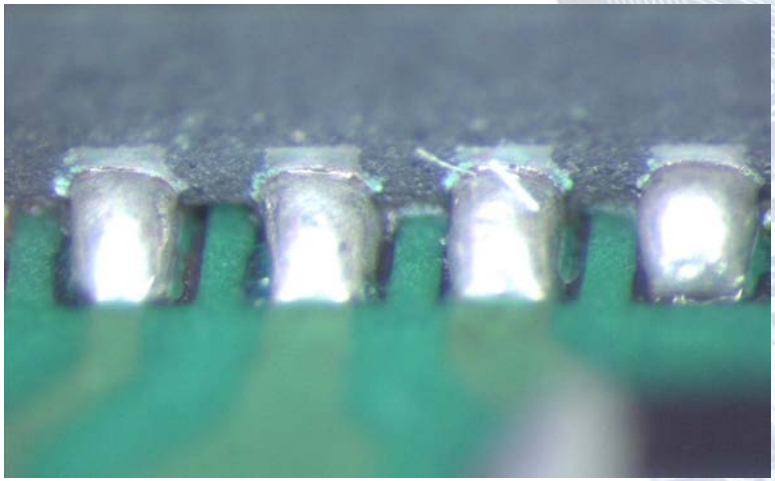
Residue under QFN in the gap still gooey

Image of Flux Entrapment on Components Side



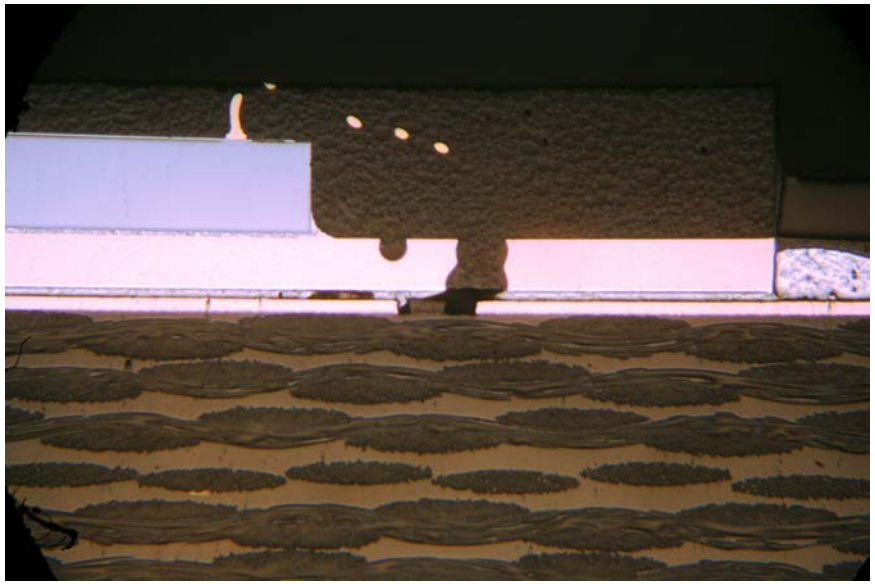
Images of QFN Flux Residues Package Side

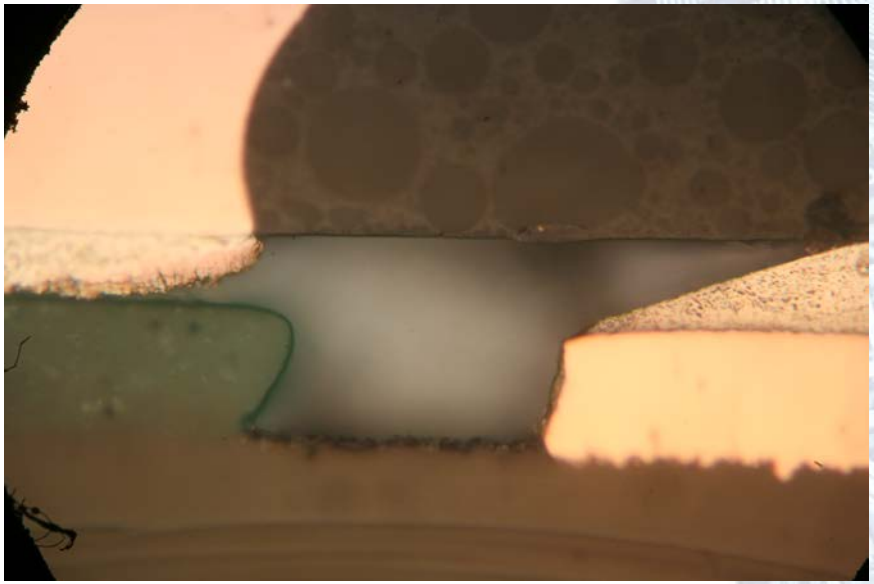




Solder at the edge of the QFN Perimeter pad showing no intermetallic or wetting to the edge lead-frame exposed / oxidized copper

Images of QFN Flux Residues
Gap Between Ground and Perimeter



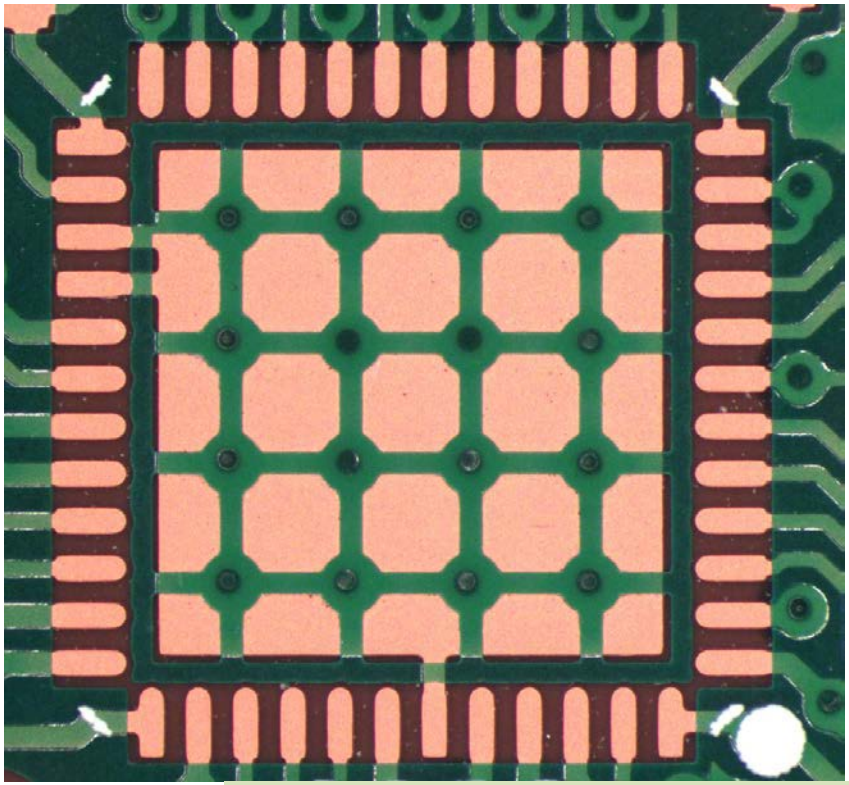


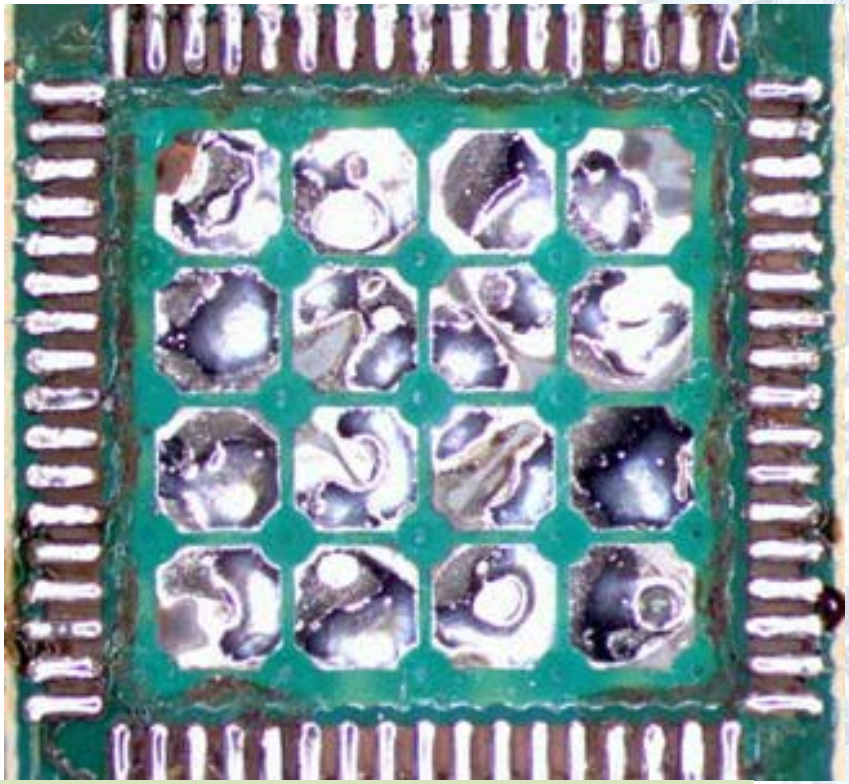
Cross section view of the QFN with a 0.5 mil standoff showing the part shift in the gap is now reduced from 10 mils to 7 mils

Cleanliness Results from Case Study

all values are in ug/in2 unless noted	Ion Chromatography							C3 Tester	
Foresite Cleanliness limits	**Cl^-**	**NO_2^-**	**Br^-**	**NO_3^-**	**PO_4^{2-}**	**SO_4^{2-}**	**WOA**	**Results**	**Time(sec)**
Bare PCB limits	1.0	3.0	6.0	3.0	3.0	3.0	N/A	Clean	>60
No Clean limits for SMT/hand Solder	3.0	3.0	12.0	3.0	3.0	3.0	25.0	Clean	>60
No Clean limits for Wave (direct contact)	3.0	3.0	12.0	3.0	3.0	3.0	150.0	Clean	>60
Failing PCBAs due to leakage									
QFN- U1 Board Surface+QFN Sample #1	0.98	0	0.65	1.69	0	1.05	224.42	Dirty	2
QFN- U1 Board Surface+QFN Sample #2	0.91	0	0.63	1.69	0	1.33	201.26	Dirty	1
QFN- U1 Board Surface+QFN Sample #3	0.92	0	0.50	1.75	0	1.35	198.65	Dirty	2
QFN- U1 Board Surface+QFN Sample #4	1.05	0	0.65	1.36	0	1.11	205.69	Dirty	1
QFN- U1 Board Surface+QFN Sample #5	0.74	0	0.60	1.25	0	1.36	245.11	Dirty	1
QFN- U1 Board Surface+QFN Sample #6	0.82	0	0.54	1.64	0	1.25	209.34	Dirty	2
QFN- U1 Board Surface+QFN Sample #7	0.55	0	0.98	1.55	0	1.33	215.36	Dirty	2
QFN- U1 Board Surface+QFN Sample #8	0.46	0	0.68	1.82	0	1.47	243.27	Dirty	1

Process Improvement for QFN lift





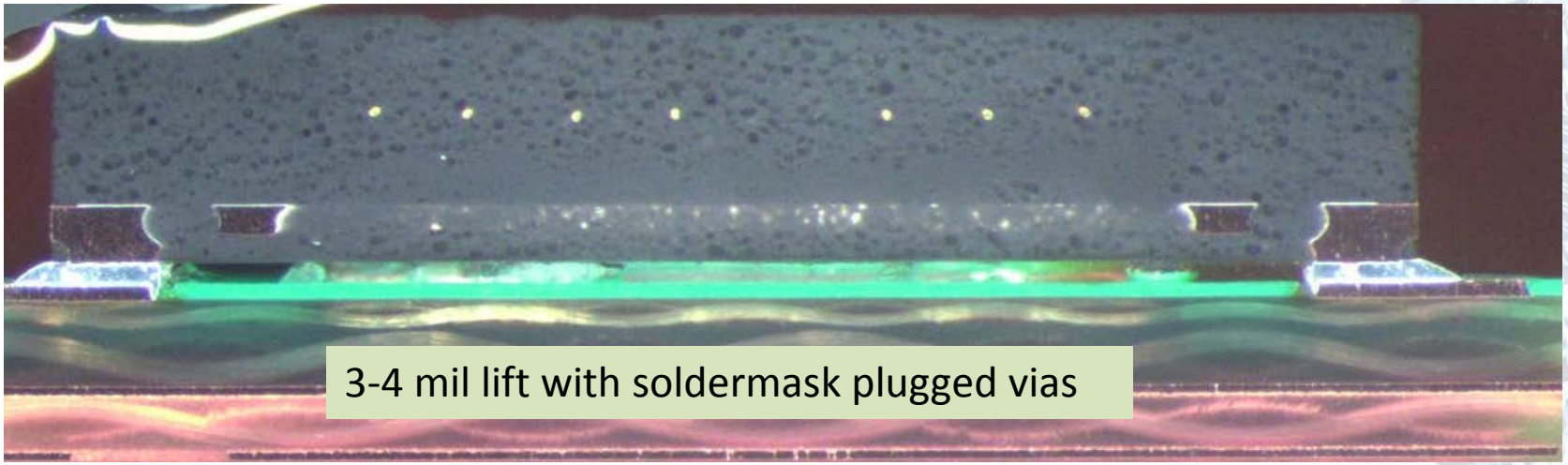
Before Paste and Reflow

After Paste / Reflow

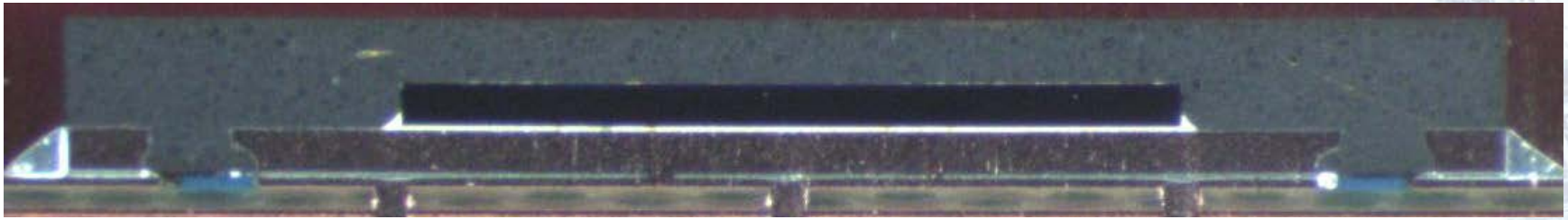
Bare board fix for standoff height improvement , all flux consistently is hard and difficult to probe

IPC MIDWEST CONFERENCE & EXHIBITION

Process Improvement for QFN lift



3-4 mil lift with soldermask plugged vias



0.80 lift mil without soldermask plugged vias

Cleanliness Results from Case Study

all values are in ug/in2 unless noted	Ion Chromatography							C3 Tester	
Foresite Cleanliness limits	**Cl^-**	**NO_2^-**	**Br^-**	**NO_3^-**	**PO_4^{2-}**	**SO_4^{2-}**	**WOA**	**Results**	**Time(sec)**
Bare PCB limits	1.0	3.0	6.0	3.0	3.0	3.0	N/A	Clean	>60
No Clean limits for SMT/hand Solder	3.0	3.0	12.0	3.0	3.0	3.0	25.0	Clean	>60
No Clean limits for Wave (direct contact)	3.0	3.0	12.0	3.0	3.0	3.0	150.0	Clean	>60
PCBA QFN Cleanliness with SM Standoff									
QFN Area + board Area U1 Sample #1	0.58	0	0.49	1.26	0	1.21	15.36	Clean	180
QFN Area + board Area U1 Sample #2	0.69	0	0.65	1.31	0	1.36	12.47	Clean	180
QFN Area + board Area U1 Sample #3	0.82	0	0.61	1.06	0	1.27	13.95	Clean	180
QFN Area + board Area U1 Sample #4	0.35	0	0.39	1.27	0	1.06	14.24	Clean	180
QFN Area + board Area U1 Sample #5	0.94	0	0.74	1.36	0	1.27	15.20	Clean	180
QFN Area + board Area U1 Sample #6	0.76	0	0.81	1.22	0	1.39	11.63	Clean	180

Summary

- QFN components when processed with no clean solderpaste trap flux under the low standoff and leave gooey flux in the gap.
- The reason that the component is so tight to the board is the solder will wick down the surface of the thermal via pulling the component tight to the board surface.
- The soldermask standoff allows the part to sit high enough and with the removal of the mask between the perimeter pads, it is able to vent out properly and complex the flux for good insultative residues.
- The cleanliness results show dramatic differences in the WOA (weak organic acids) between the two groups.