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Biography

Dr. Coleman earned his Ph.D. in Physics from West Virginia University. His early career was spent with NCR developing memory and visual display devices. Bill has spent the past 23 years at Photo Stencil as Vice President of Technology working closely with customers to understand their SMT printing requirements. At Photo Stencil he has developed several innovative solutions for these requirements. Bill has published over 20 papers in this field and is presently Co-Chair of IPC 5-21e committee, which produced IPC 7525 "Stencil Design Guidelines". Bill is on the Editorial Advisory Board for SMT Magazine and the Advisory Board for West Virginia University.

Title

Printing and Assembly Challenges for QFN Devices

Executive Summary

QFN's offer advantages in reducing size and weight and have excellent thermal and electrical Conductivity related to the ground plane. QFN's also present printing and assembly challenges including package floating during reflow and the very small stencil aperture area ratio's resulting from the narrow and short pad design of the packages.

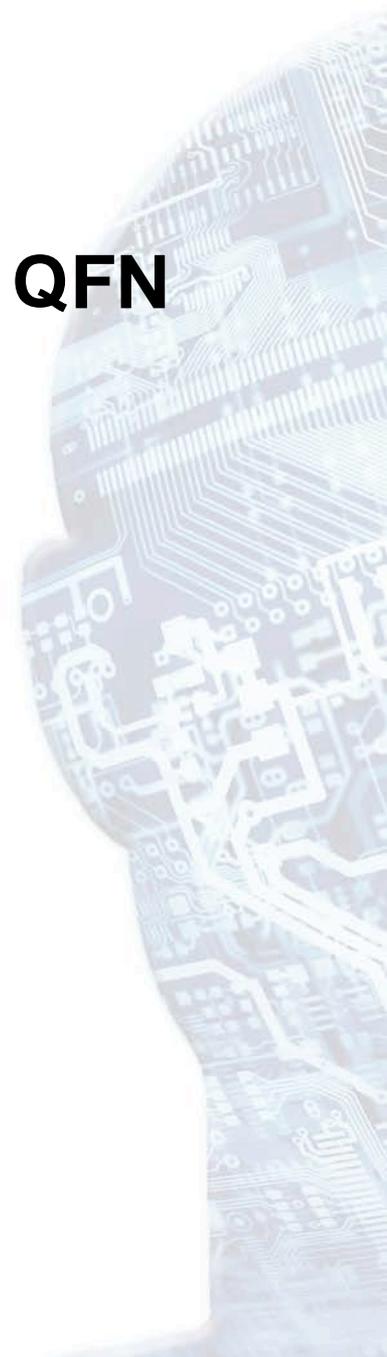
This presentation will review stencil design aimed at improving the QFN printing and assembly process, QFN repair options will also be presented

Printing and Assembly Challenges for QFN Devices

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Colorado Springs



Definition:

QFN (Quad Flat Pack, No Leads)

DFN (Dual Flat Pack, No Leads)

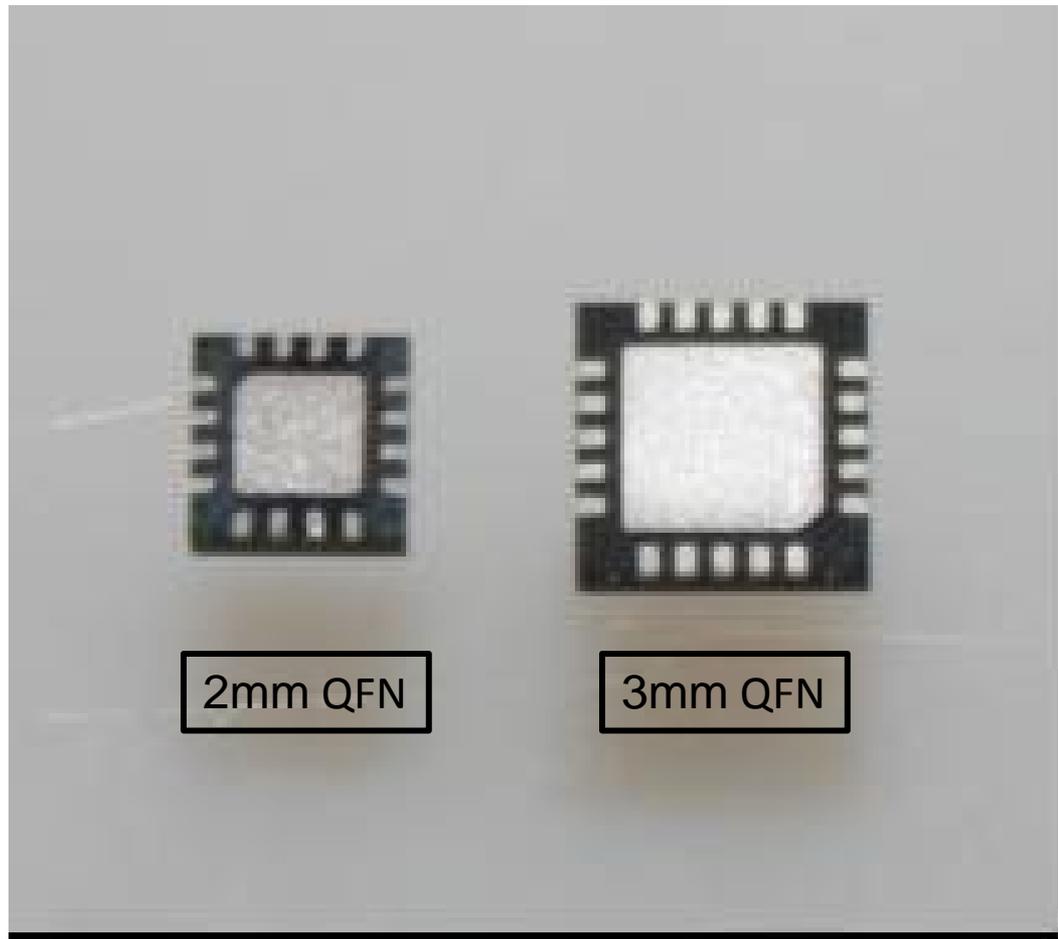
Leads and Ground Plane are flat on bottom of package

Typical Size range 2mm to 12mm

Typical Thickness .85mm

Typical Pitch .4mm / .5 mm

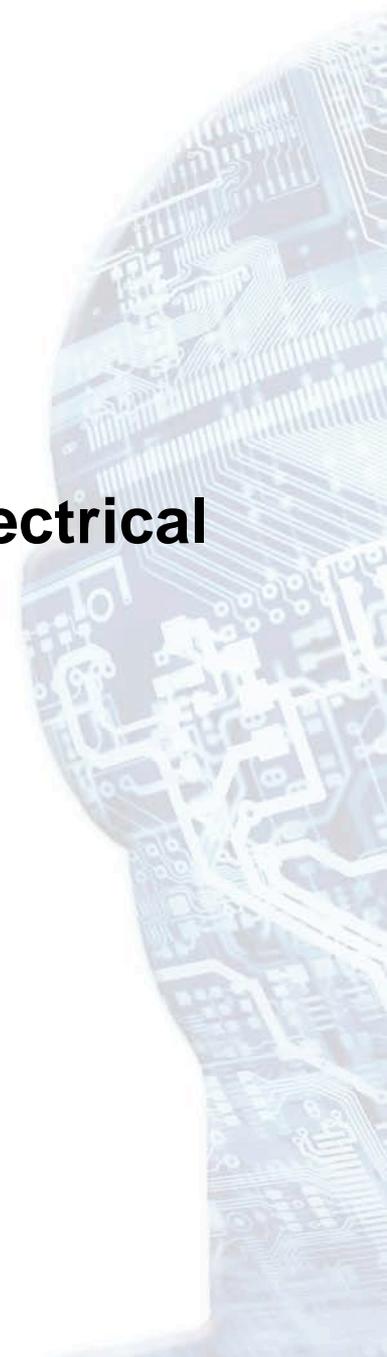




QFN Packages

Advantages of QFN Devices

- **Very Small Form Factor**
- **Ground Plane affords excellent thermal and electrical Conductivity**
- **Packages are small and light**



Printing Challenges:

- **Package floating during reflow**
- **Solder Mask Configurations / Stencil Design**
- **Apertures typically short and narrow / Area Ratio**
- **Solder Mask Height**
- **QFN Repair**

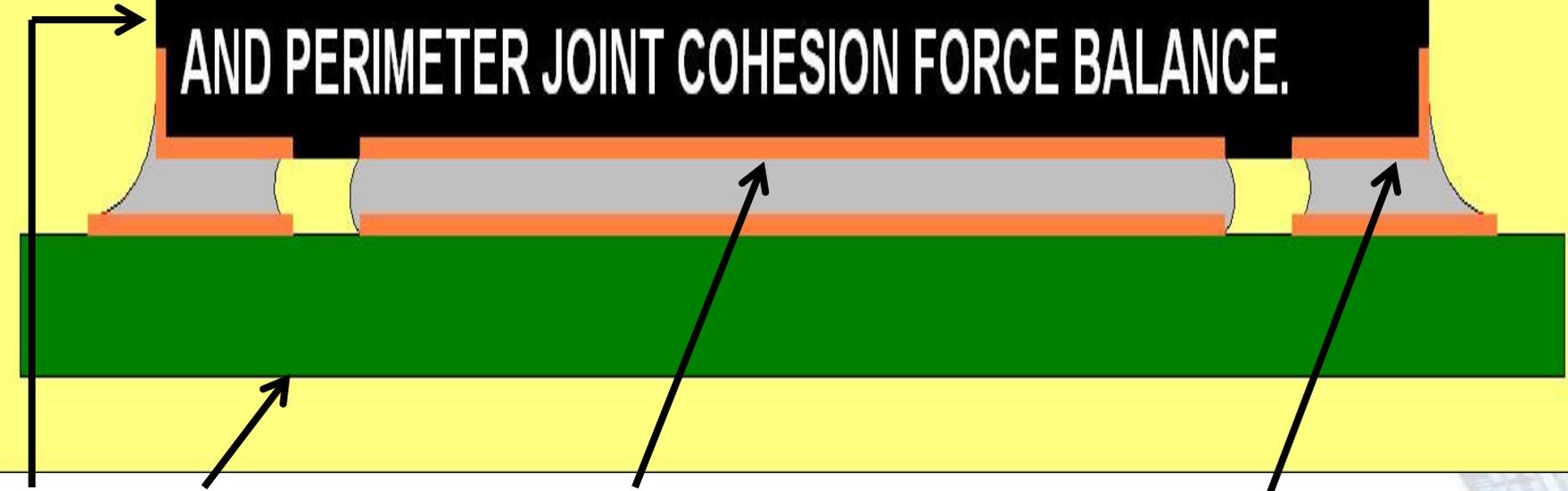
SURFACE TENSION IN REFLOW CAUSES A LARGE CENTER DOT TO LIFT ABOVE THE PERIMETER DOTS.



**WINDOWING EVENS THE LIFTING FORCE AND
ALLOWS CONTROLLED OUTGASSING.**



QFN / DFN STANDOFF HEIGHT IS A FUNCTION OF CENTER AND PERIMETER JOINT COHESION FORCE BALANCE.

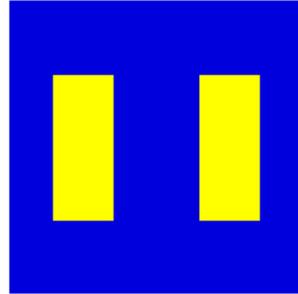


IC PCB Center Pad Perimeter Pad

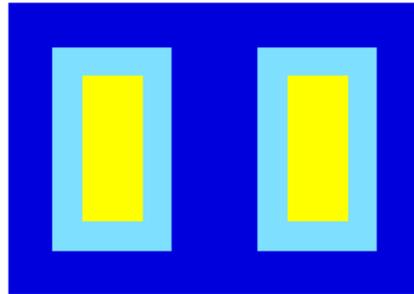
Benefit of Window Pane Ground Plane Apertures

3 Solder Mask Types

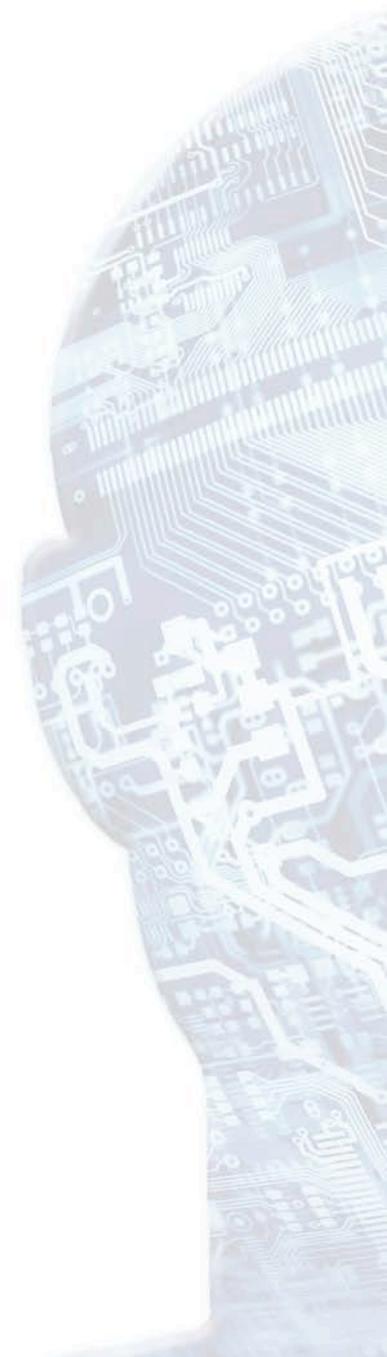
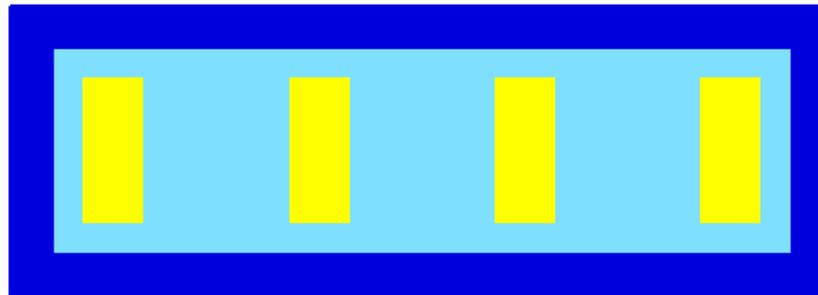
SMD



NSMD



NSMD-WINDOW



Stencil Design for Typical QFN Apertures (NSMD)

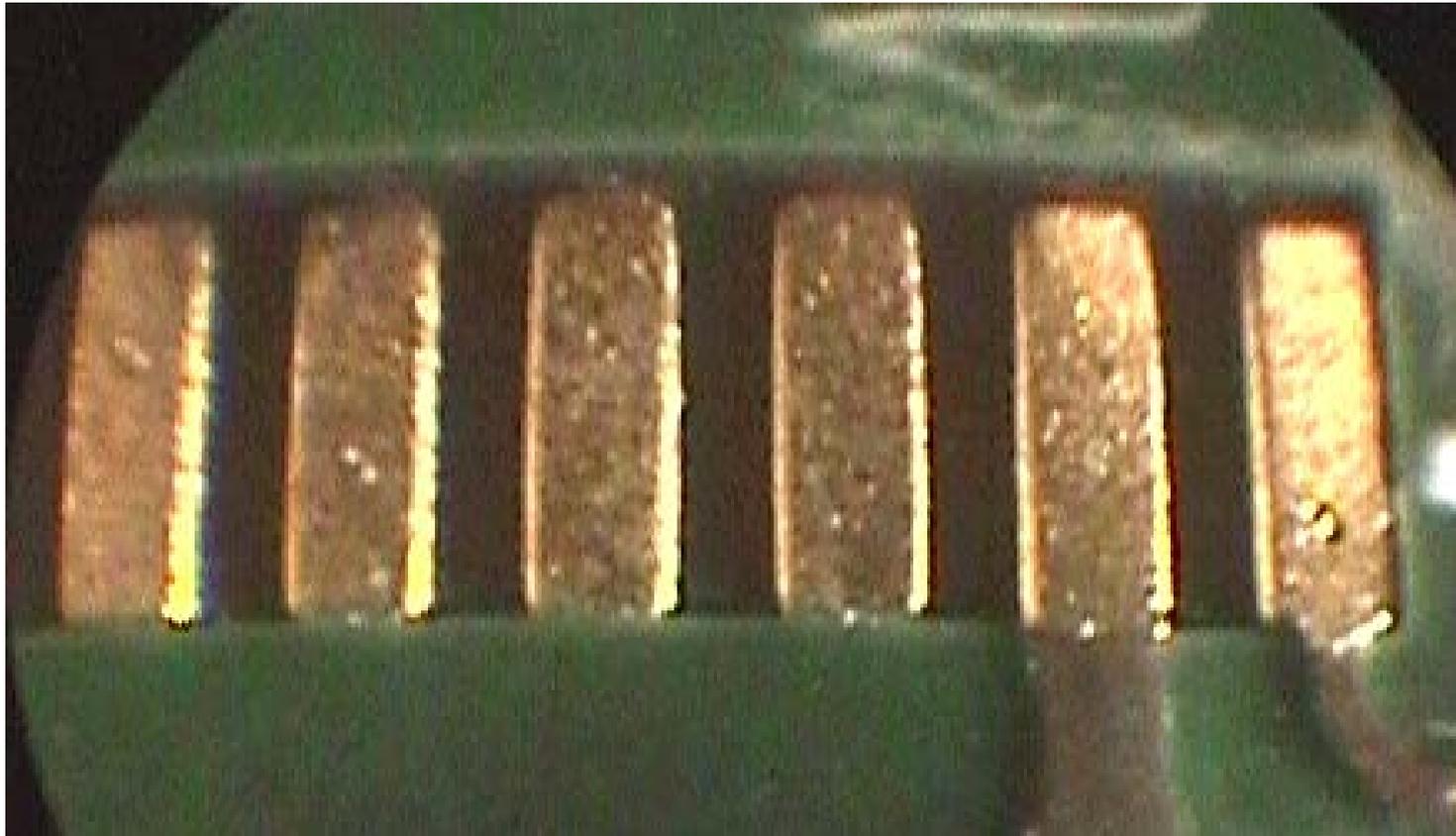
Package	Pitch	I/O	package lead width	package lead length	PCB	PCB	Aperture NSMD	Aperture NSMD	Stencil Thickness	Area Ratio
3mm	.5mm	12	.23mm	.55mm	.23mm	.75mm	.23mm	.75mm	.125mm	0.70
4mm	.5mm	20	.25mm	.40mm	.25mm	.60mm	.25mm	.60mm	.125mm	0.71
7mm	.5mm	44	.25mm	.55mm	.25mm	.75mm	.25mm	.75mm	.125mm	0.75
10mm	.5mm	72	.23mm	.40mm	.25mm	.60mm	.25mm	.60mm	.125mm	0.71
12mm	.5mm	80	.25mm	.55mm	.25mm	.75mm	.25mm	.75mm	.125mm	0.75

Stencil Design for Typical QFN Apertures (SMD)

Package	Pitch	I/O	package lead width	package lead length	PCB	PCB	Aperture SMD	Aperture SMD	Stencil Thickness	Area Ratio
3mm	.5mm	12	.23mm	.55mm	.23mm	.75mm	.18mm	.70mm	.125mm	0.57
4mm	.5mm	20	.25mm	.40mm	.25mm	.60mm	.20mm	.55mm	.125mm	0.59
7mm	.5mm	44	.25mm	.55mm	.25mm	.75mm	.20mm	.70mm	.125mm	0.62
10mm	.5mm	72	.23mm	.40mm	.25mm	.60mm	.18mm	.55mm	.125mm	0.54
12mm	.5mm	80	.25mm	.55mm	.25mm	.75mm	.20mm	.70mm	.125mm	0.62

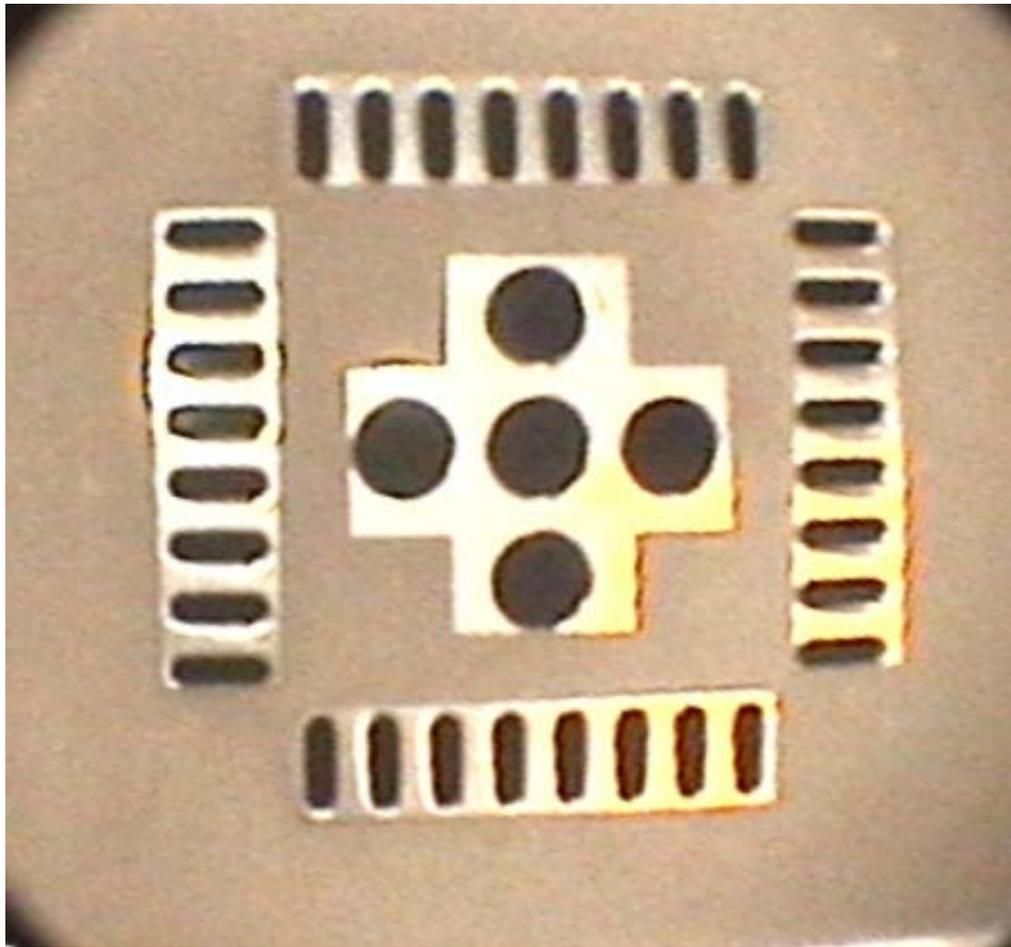
Stencil Design for Typical QFN Apertures (NSMD window)

Package	Pitch	I/O	package lead width	package lead length	PCB	PCB	Aperture SMD	Aperture SMD	Stencil Thickness	Area Ratio
4mm	.4mm	32	.175mm	.45mm	.175mm	.610mm	.175mm	.560mm	.125mm	0.53
4mm	.4mm	32	.175mm	.45mm	.175mm	.610mm	.175mm	.560mm	.100mm	0.67



NSMD Window with Mask to pad gap of .03mm

Problem: Stencil can't make contact with pads causing paste smear on bottom side of stencil.

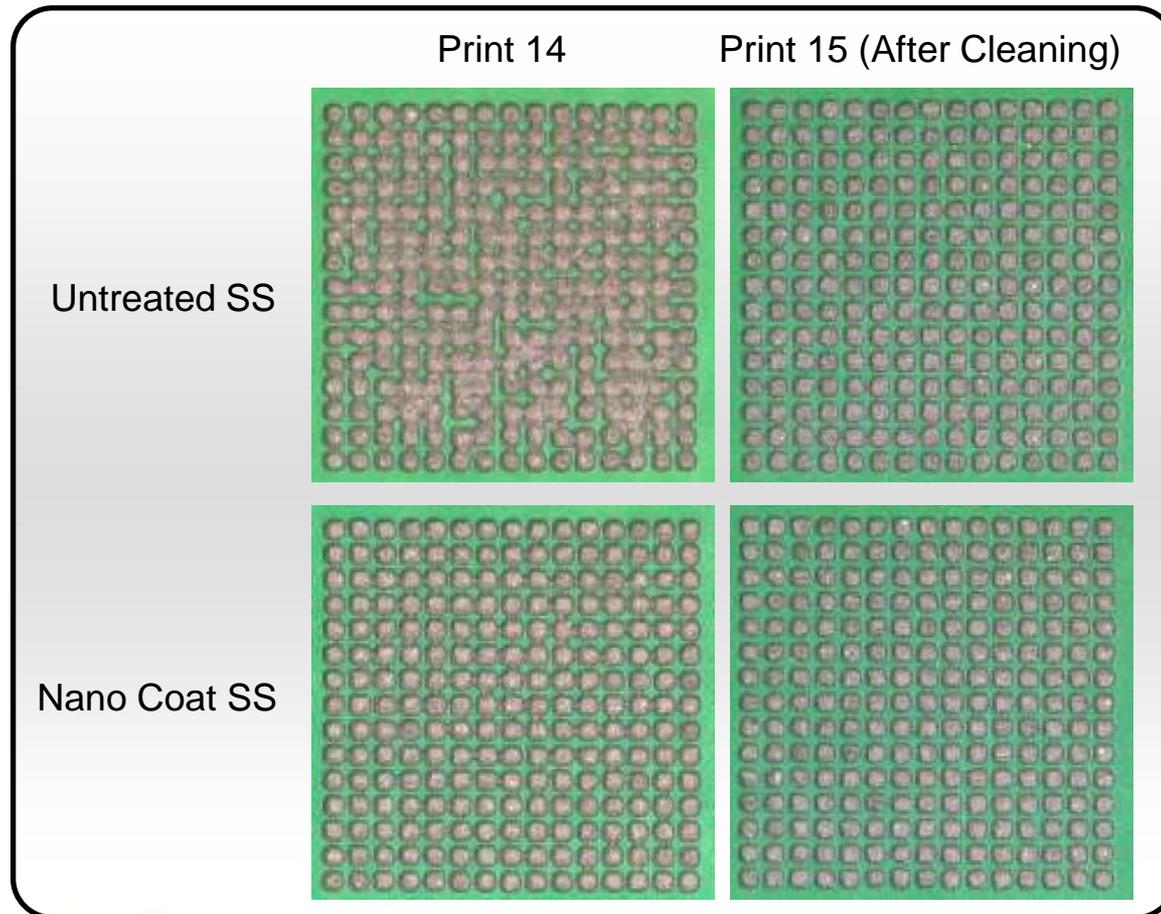


Step Electroform Stencil on PCB side - .1mm thick around QFN apertures and .08mm elsewhere for all other apertures.

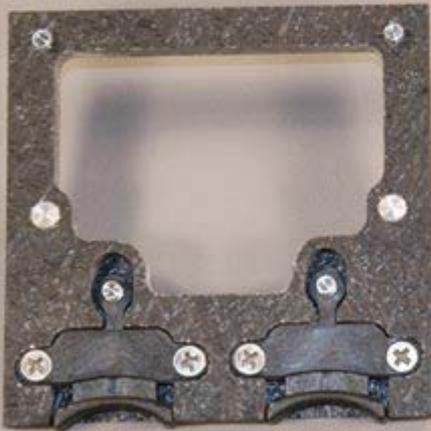
Alternative Solution: Nanocoat .1mm thick Stencil w/o Step

Cleaner Frequency Test Results

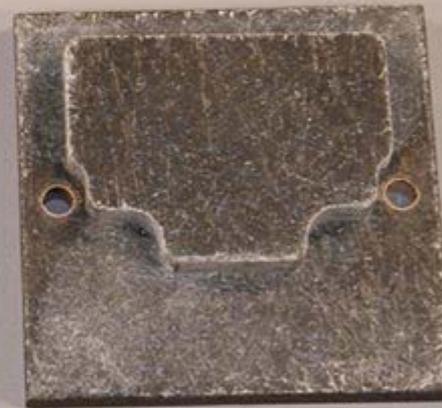
The images were taken of a 400µm CSP on the test board after print 14 and 15, before and after the cleaning cycle.



QFN Repair Tool

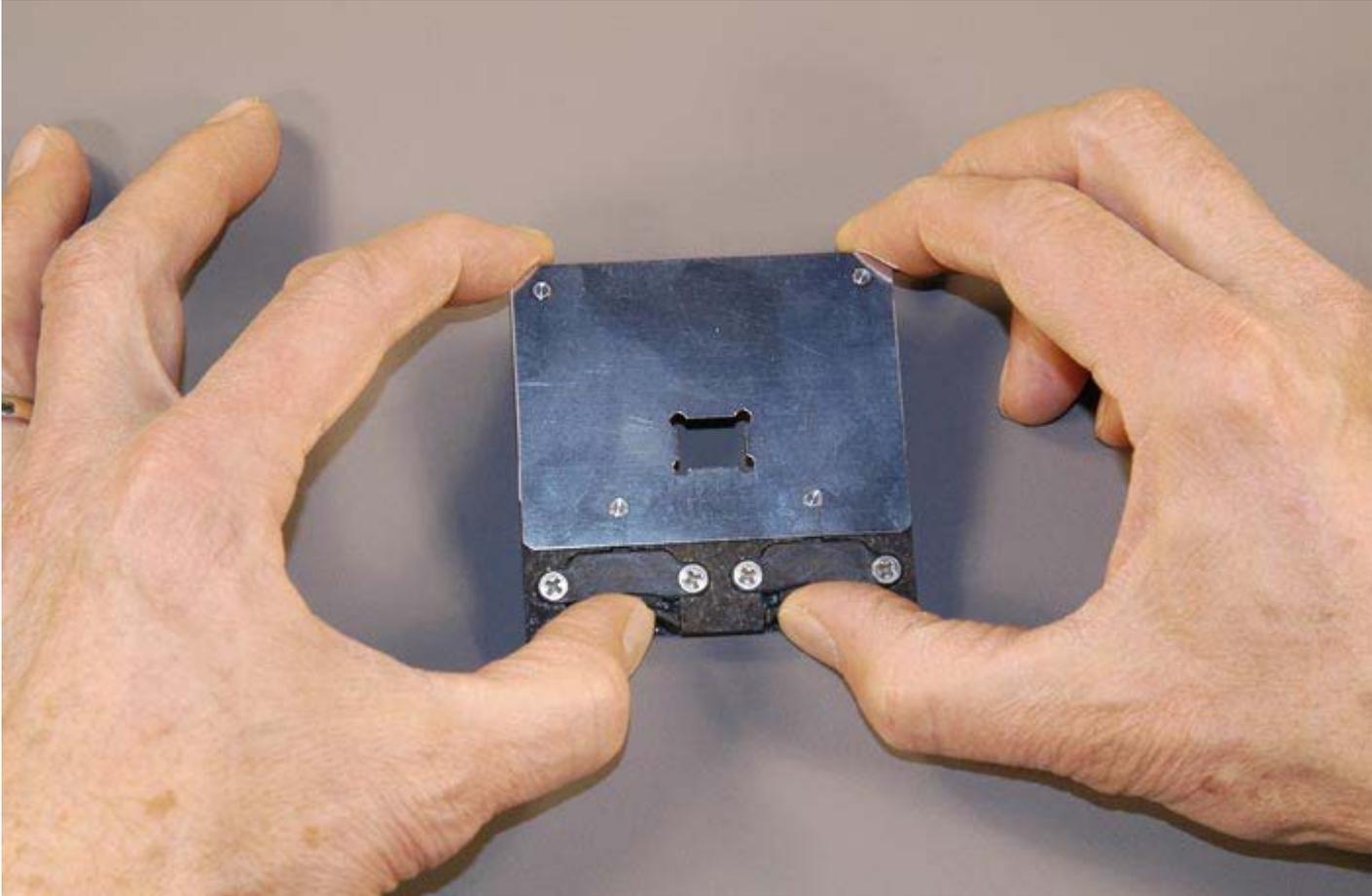


Stencil Holding Fixture

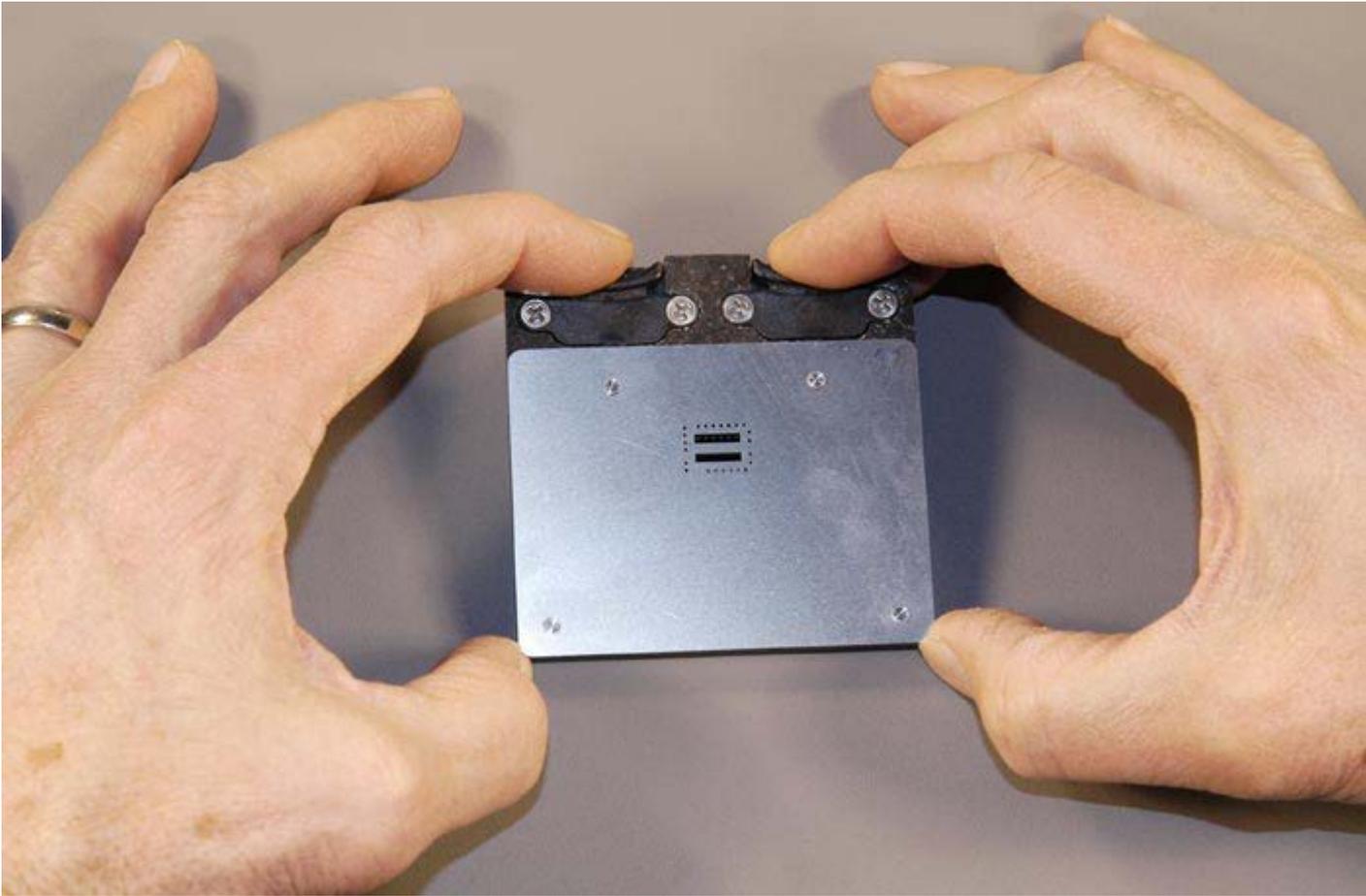


Package Hold-Down Fixture

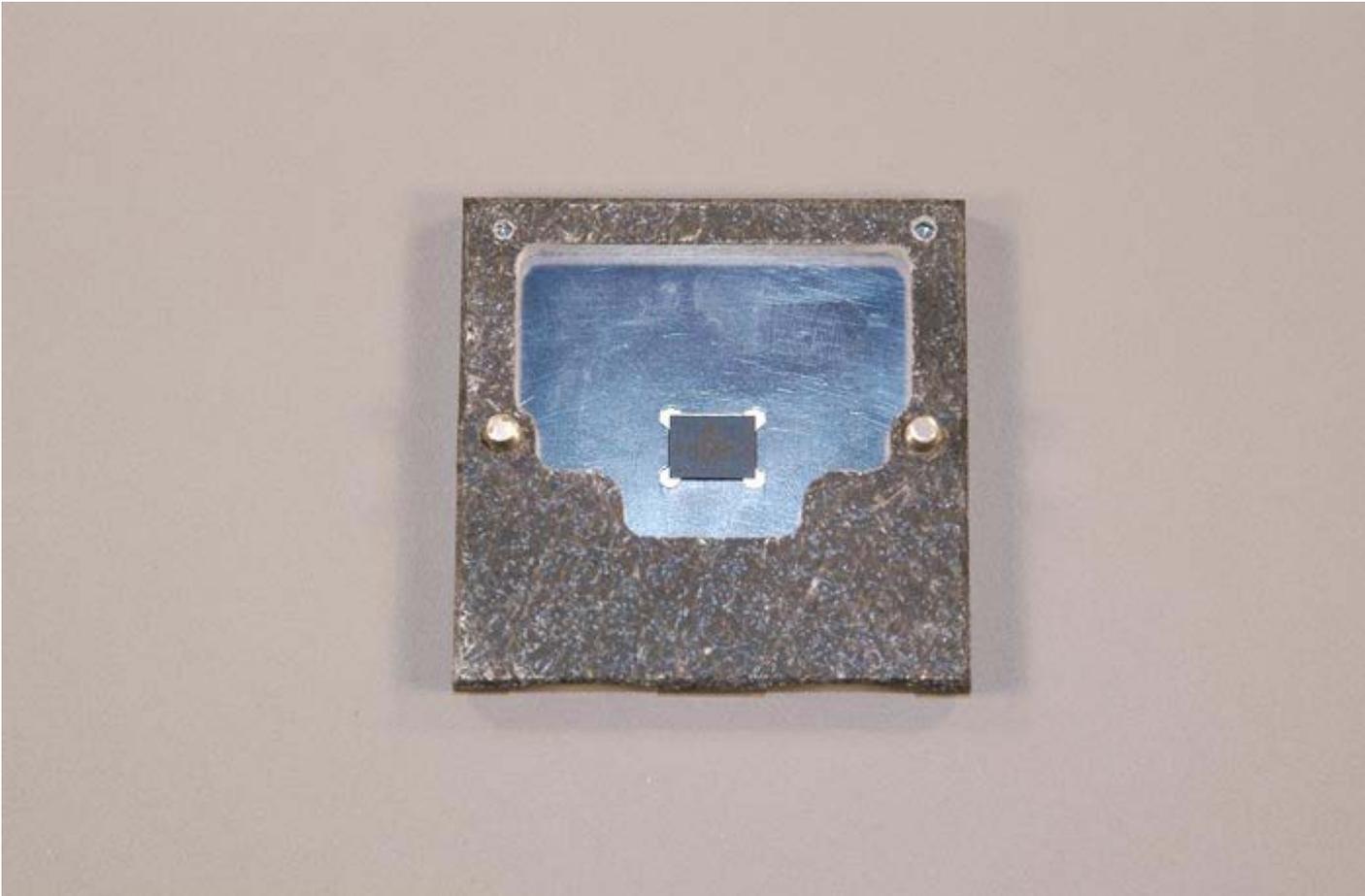
Package Holding Fixture



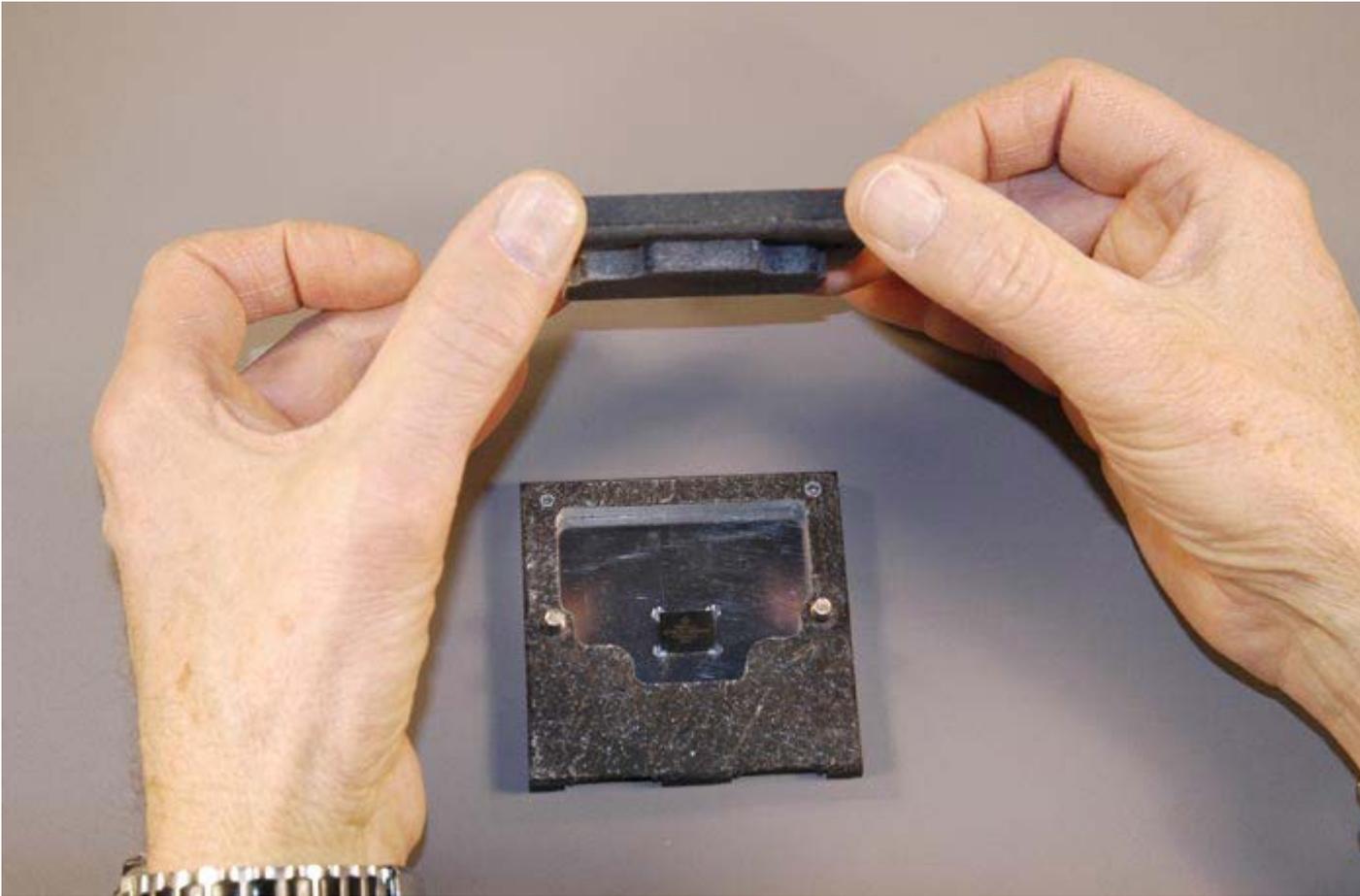
Stencil placed on alignment pins



QFN placed in Package Holder



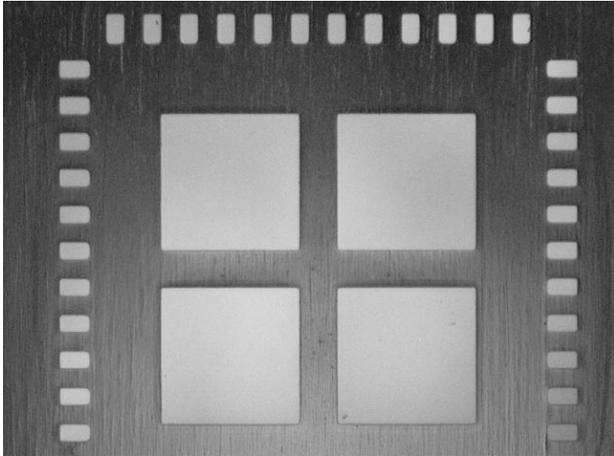
Package Hold-Down fixture is snapped into place



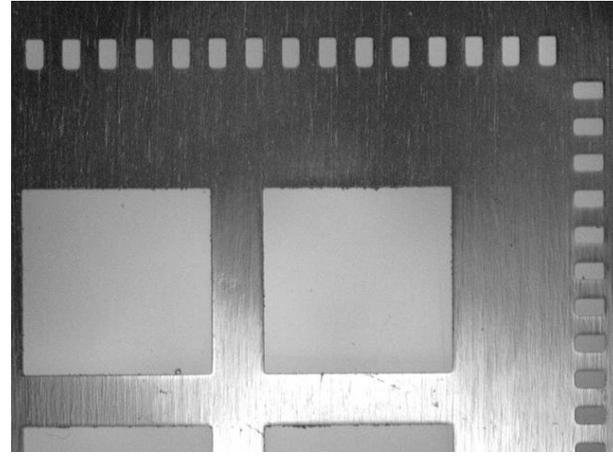
QFN held in place just prior to printing solder paste



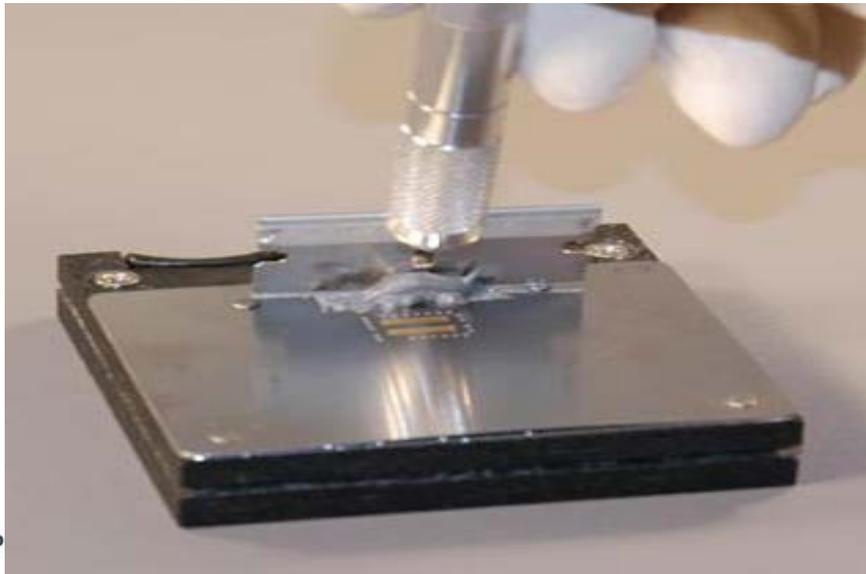
7mm repair stencil



10mm repair stencil



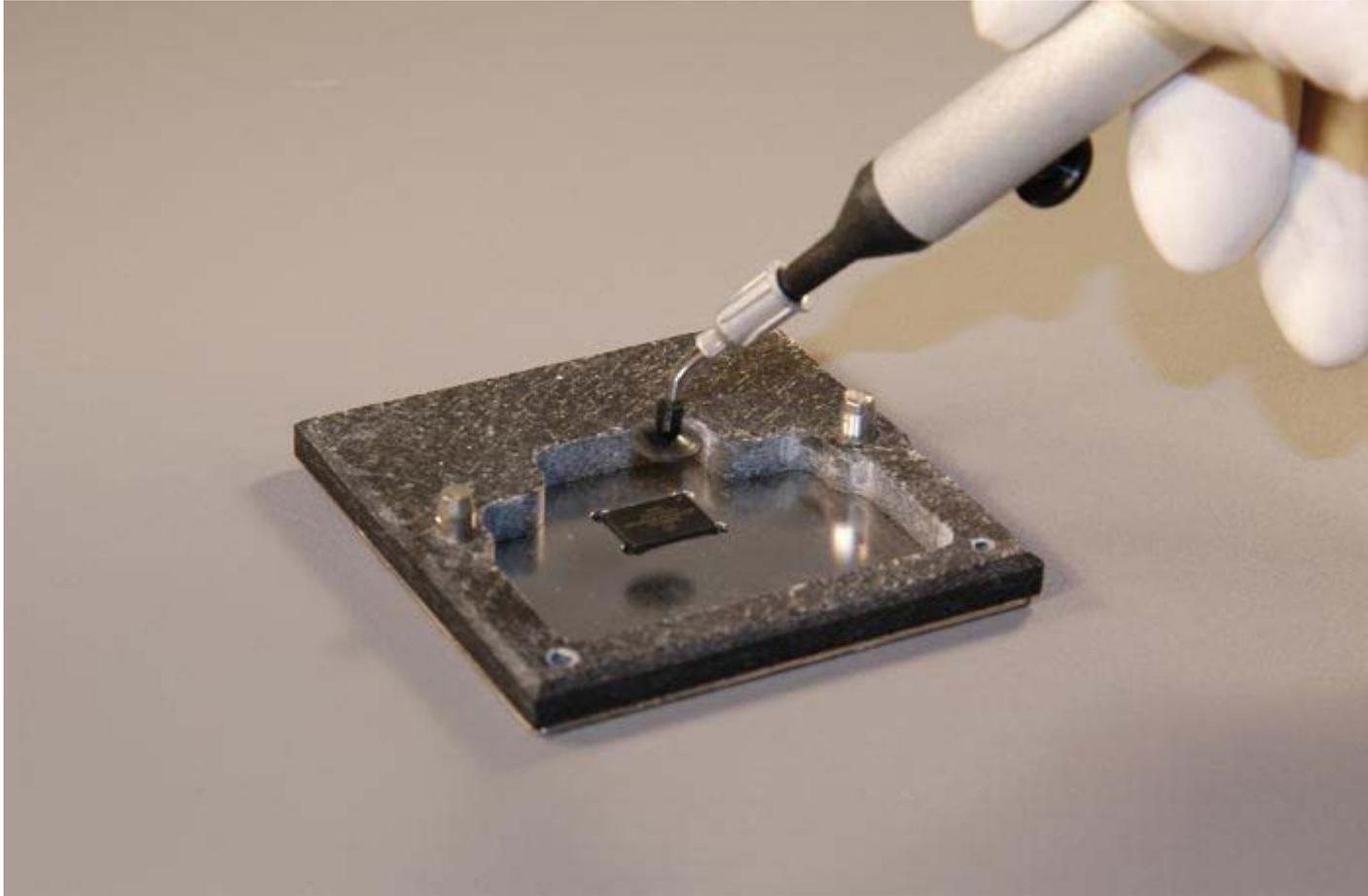
Printing Solder Paste on QFN device while in holding tool



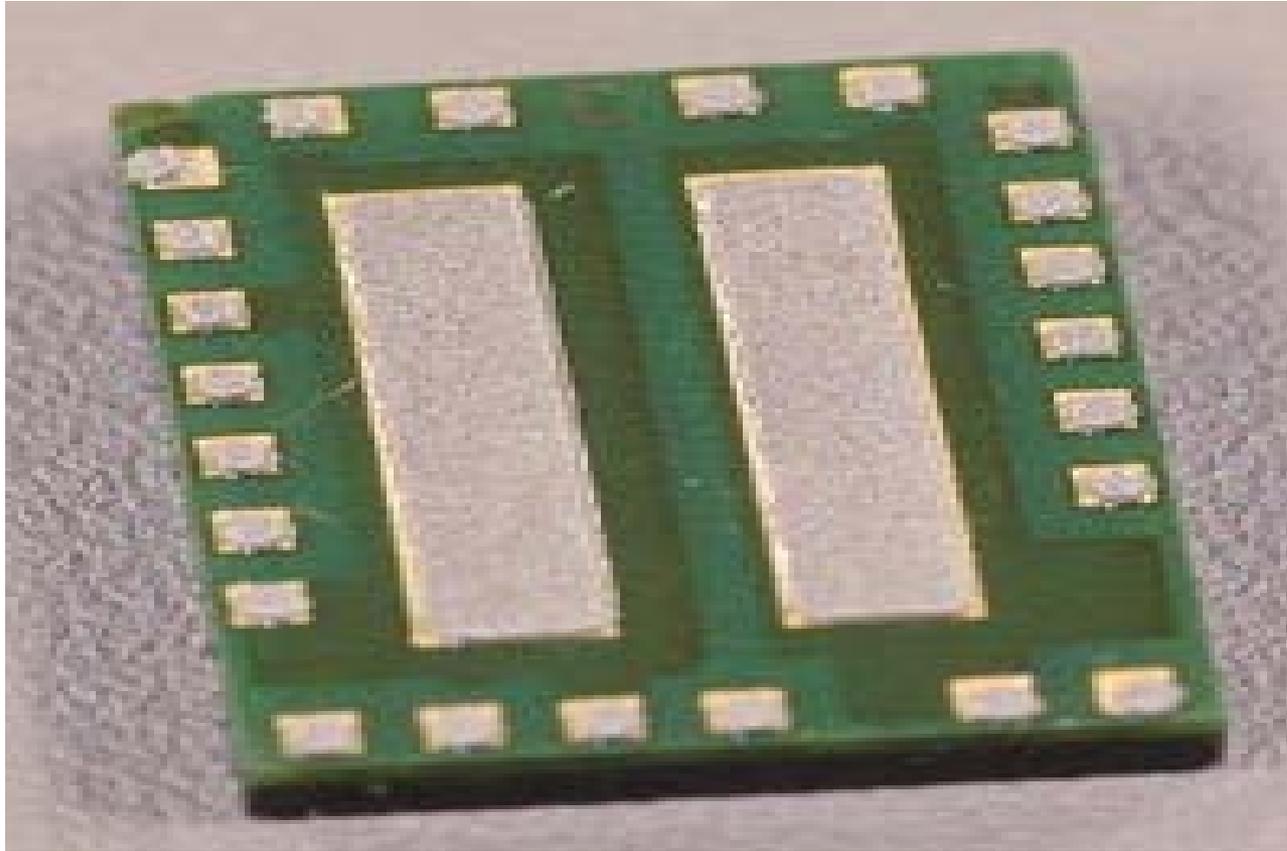
After Solder Paste Printing



Package Hold-Down fixture is removed and Vacuum Pick places QFN on PCB



Solder paste printed on QFN before placement on PCB for rework



Conclusion:

Although QFN devices present a challenge to the SMT assembly process with proper stencil design, proper stencil technology selection (Laser, Electroform, Nano-Coat), and proper PCB solder mask layout these challenges can be overcome.

The most popular QFN repair seems to be to print solder paste directly onto the QFN leads and ground plane.

References:

- **Private communication with Greg Kloiber, Manufacturing Engineer Plexus Corp.**
- **“BGA and QFN Repair Process” William E. Coleman, APEX 2008**

General QFN References

- **“Rule of thumb guide for Practical DFN/QFN Printed Circuit Board and stencil Design” James R. Staley, Linear Technology application note**
- **“PCB Land Pattern Design and Surface Mount guidelines for QFN Packages”, Intersil Technical Brief TB389.6**
- **“QFN Layout Guideline”, Texas Instrument Application Report SLOA122**

Thank You

Questions??

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