A Simple and Innovative Method for the Manufacture of Discrete Capacitors within Multilayered PCB's

Lionel Fullwood
WKK Distribution Ltd.
Kowloon, Hong Kong

This work initially started with some research into ink jet technology materials for legend printing. Our company in Hong Kong was working at the time with a Japanese company with the end goal being the development of a new machine for PCB legend printing. As part of that project, we were developing a new TiO2 based ink for white legend printing.

As part of the total process, we wanted to obtain electrical data on the materials we had developed, and included capacitance as one of those items. This was accomplished by coating the materials between two copper plates. We were quite surprised to find reasonable and repeatable values. Please note from Figure 1 that this was really quite a sloppy initial test.

Figure 1 – Test Plates used to Initially Confirm that the Material could Function as a Capacitor

For a number of years it has been technologically feasible to place distributive capacitors as layers within an MLB, but I felt that the ability to lay down individual capacitors of different values within the same circuit layer was infinitely more valuable. Thus started our work that is described in this paper.

The values obtained really started me thinking about the possibility of using ink jet technology for the precision deposition of capacitive materials for the manufacture of discrete capacitors in MLB's. If we could also use other materials than TiO2, then it might be possible to fabricate capacitors with different values on the same plane or layer within the MLB.

The major problem was the necessity to build a test structure that was robust and stable during the necessary heat excursions required for the external population of the finished MLB. After many attempts, we determined that the best approach was to use a pre-preg package for both layer-to-layer adhesion, as well as encapsulation of the individual capacitors. This would provide a coherent package, and one with excellent adhesion qualities. I have tried to provide this concept pictorially in Figure 2.

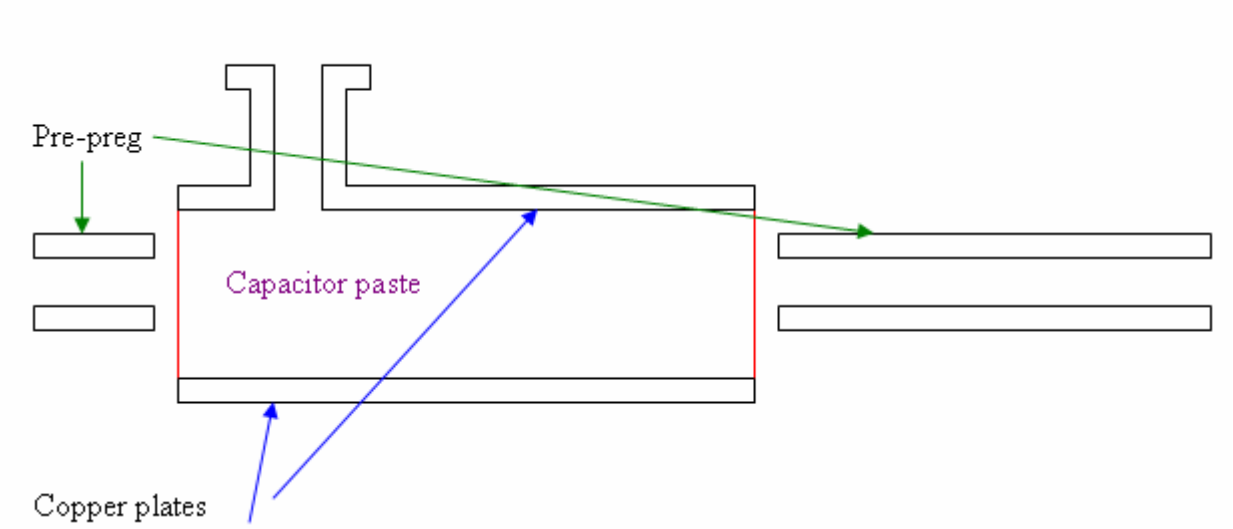

Figure 2

However this concept required that the pre-preg should not be applied in a continuous sheet, but should instead encapsulate the capacitor package. We eventually came up with a test pattern that allowed us to locate incrementally larger copper planes to test the concept. This would allow us to determine the linearity of the resultant capacitor units and predict also reproducibility.

Mirror images were exposed on sequential layers 2 and 3, (Figure 3) so that copper pads were imposed directly above and below each other, and functioned as capacitor plates. The sizes of the five pads were: 1sq. cm; 2 sq. cm; 4 sq. cm; 6 sq. cm; and 9 sq. cm.

Contact needed to be made to adjacent layers for capacitor function, and so we made the following A/W layers for interconnection purposes on layers 1 and 4 (Figure 4).

The following pictures indicate our test pattern:

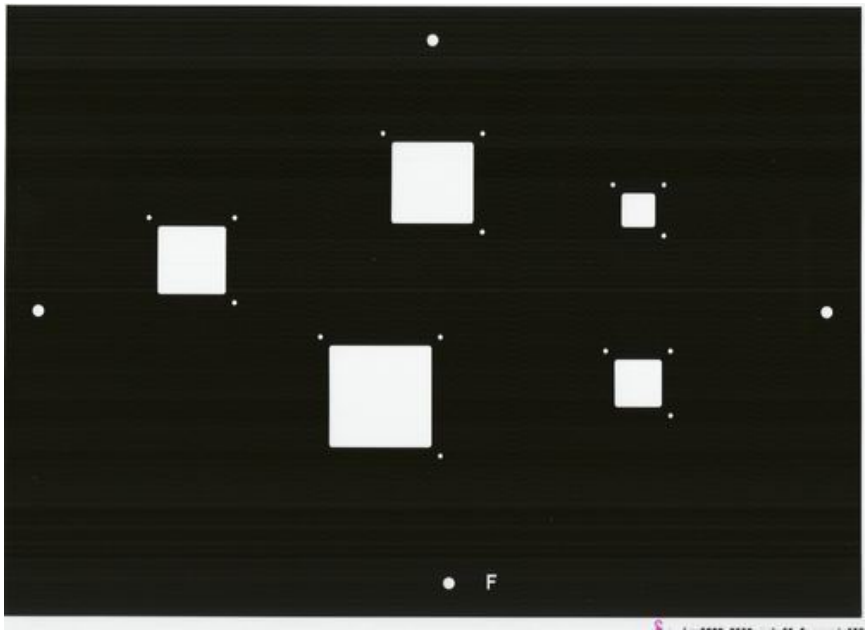

Figure 3 - Layer 2 and 3

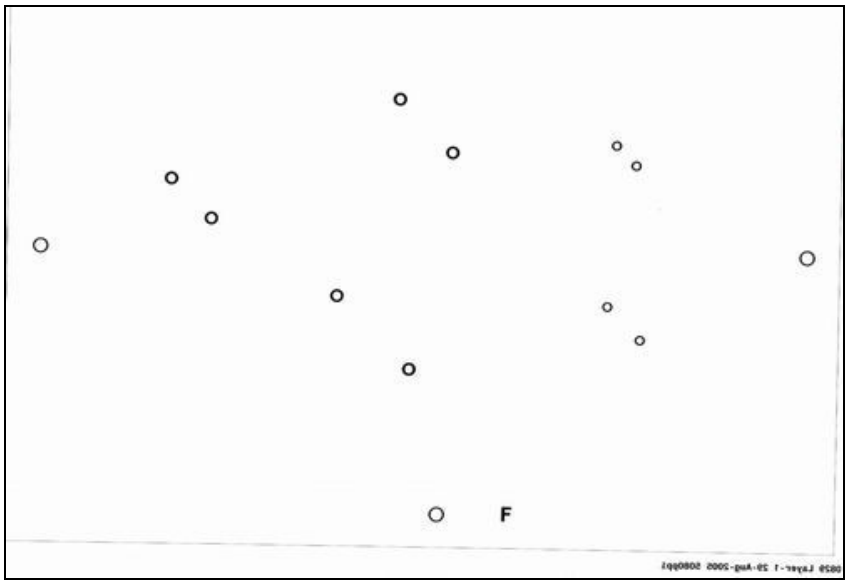

Figure 4 - Layer 1 and 4

For the basic testing we had the pre-preg sheets CNC routed, to provide the correct cavity size. For small volume runs, a steel rule die could be used, and for volume manufacturing, a normal die set would probably be used. We chose to size the dimensions of each opening as 0.003" (75 microns) larger per side than the etched plates in the substrate. The result was that the etched plate and the capacitive material were encapsulated by the cured pre-preg, as well as the distance between the layers fixed, based upon the pre-preg chosen. We used 1020 type materials with a no-flow resin, as this would maintain the layer-to-layer spacing most easily.

As part of the program, we manufactured a set of press plates for the size panels being run. These press plates were fitted with tooling pins that corresponded to the tooling
Holes in the art work layers and the pre-preg. Thus we were able to register all components of the package together.

The goal was to be able to lay down capacitors that were +/- 15% of the nominal value both during initial MLB fabrication, and also after heat cycling.

The Japanese company we worked with was having ongoing problems with their ink jet machine and this caused us not to trust the results obtained. We chose not to delay the testing further,. and therefore used a silk screen image to lay down the capacitive material. The actual manufacturing process follows:

1. Cut laminate to size.
2. Drill tooling holes.
3. Pumice scrub.
4. Coat with dry film.
5. Expose panels with one panel being layer 1 / 2, and the second panel being layer 3 / 4.
6. Develop and plate through holes for contact with the capacitor plates.
7. Strip and etch panels, and remove tin protective layer.
8. Either brown or black oxide treat the panels.
9. Align and silk screen layers 2 and 3 with capacitor material.
10. Air dry for 1 – 2 hours. Note: in production mode, this would be a short oven bake at 40 – 50 º C.
11. Lay up package with 2 sheets of router cut 1020 no flow pre-preg as the separator sheets and bonding layer.
12. Load in the ML press. Note: it is felt that a vacuum press is mandatory so as to remove the residual solvent in the capacitive material.
13. Complete press cycle, and cool to room temperature.

We built 4 sets of samples and tested them for capacitive values. The results are shown in Table 1 and Figure 5.

Table 1 – Samples Built and Tested for Capacitive Values

Copper area	*Capacitive values in pf*				
	Set 1	Set 2	Set 3	Set 4	Average
1 cm2	34	32	35	36	34
2 cm2	67	64	69	70	67.5
4 cm2	142	138	140	142	140
6 cm2	187	183	205	210	196
9 cm2	283	301	320	315	305

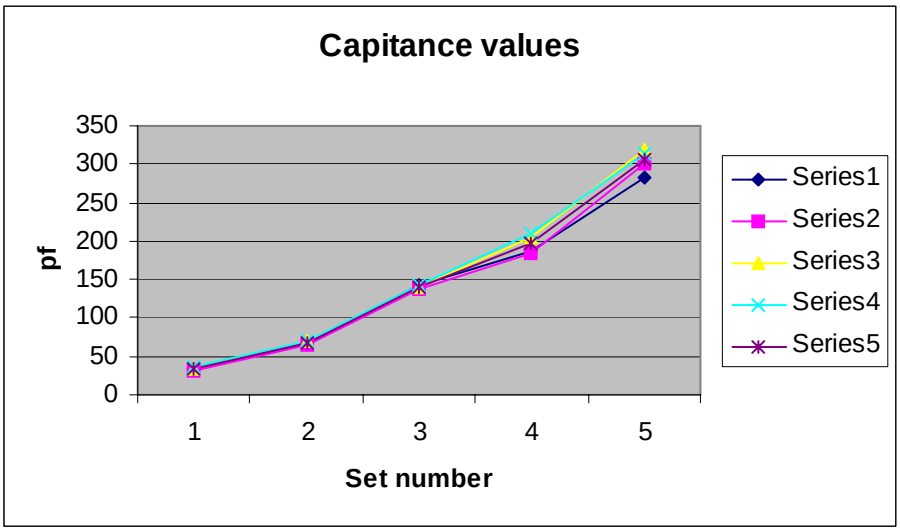

Figure 5 – Capitance Values

At this point, the results were extremely encouraging. We built 3 more sets, and the data paralleled the initial results. However at this point we had not demonstrated that the values obtained were stable. It was therefore necessary to subject the samples to a heat profile program.

As there was no PCB facility with production equipment available in Japan that I could use, I made arrangements with a colleague at the Tyco Electronics facility in Logan, Utah, to run the panels through the HAL line at that facility. The unit was a TET-Halco horizontal HAL line. The temperature setting of the machine was 300º C, about 40 degrees higher than I would have chosen. As this unit was the production machine and was in operation 24 / 7, we agreed to use the normal line parameters.

The panels were conditioned by a pre-bake at 150º C for 2 hours. Due to a handling error, set 3 was lost in the machine, and so we only could provide data for sets 1, 2, and 4. The panels were allowed to normalize to room temperature for about 10 minutes, and then passed through the HAL machine twice.

The data obtained is shown in Table 2.

Table 2 – Data Passed Through HAL Machine Twice

Copper area	*Capacitive values in pf after HAL treatment*				
	Set 1	Set 2	Set 3	Set 4	Average
1 cm2	36	35	lost	39	37
2 cm2	69	62	lost	75	68
4 cm2	152	141	lost	140	144
6 cm2	187	190	lost	207	194
9 cm2	273	290	lost	322	295

Again the information is shown in Figure 6:

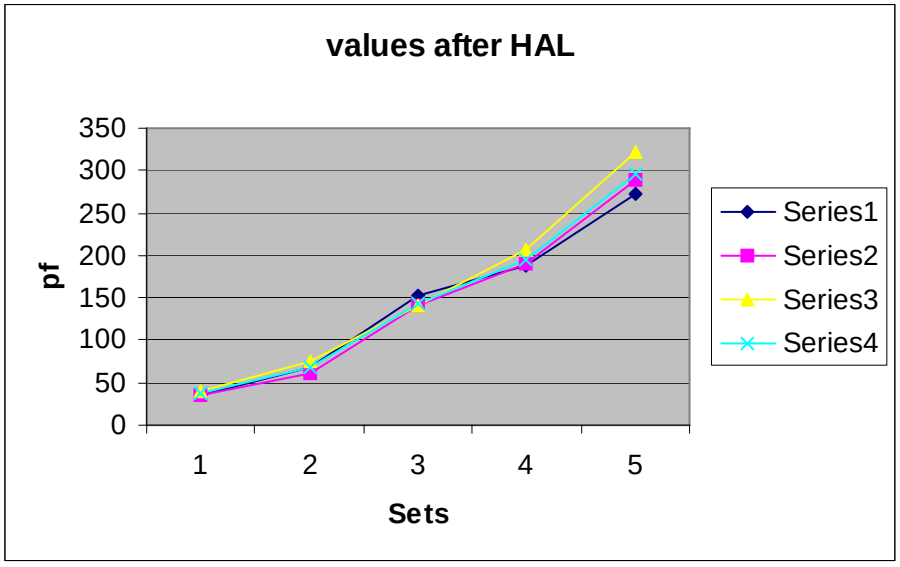

Figure 6 – Values of HAL

We were extremely satisfied with the results obtained. All values were within the 15% tolerances we had set as a goal. The substrates were able to withstand a rigorous heat profile cycle and still retain the initial values obtained after lamination.

Recently checks were made with a commercial formulation of capacitor paste ED 8080 from Electra Polymers of the UK. It appears that this manufacturing process should result in a value of about 850 pf per sq. cm., thus providing for production values for practical system capacitors to be embedded within the substrate. In fact, it was possible to use separate screenings of TiO2 based paste and ED 8080 paste on the same layers and obtain functional capacitors with widely differing values.