Optimized System Design Through Industry Benchmarking of Fabrication Tolerances and Material Properties

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Abstract
Benchmarking of industry fabrication capability, feature tolerances and material property variation is essential to aligning product requirements and industry capability. Statistical based characterization of feature tolerances and material properties are being used to optimize system and silicon designs. Assessment of industry capability is used to validate process improvements and ensure alignment with product.

Introduction
Current computer performance trends have propelled digital signaling frequencies into the GHz range for a variety of CPU, memory and peripheral interconnect schemes. At these signaling frequencies the portions of timing errors and signal losses associated with the PCB interconnect can be the dominant performance limiter. Improving system interconnect performance requires accurate high-frequency modeling of the system design including all the physical and electrical properties of the PCB interconnect.

These models are dependent not only on the nominal physical properties of the package and/or board materials; but, also on the statistical variations of each parameter. The variations that affect the performance of high speed interconnect include vendor-to-vendor, batch-to-batch and even localized spatial variation across a given package or PCB board. Accurate characterization of these variations is a prerequisite to correctly model the PCB interconnect and, thereby enabling predictable system designs.

This presentation describes some of the key elements and learning's from fabrication tolerance and material property benchmarking at Intel. Proper benchmarking techniques have been essential in developing electrical models that not only model impedance variation; but, also model interconnect loss, coupling, mode conversion, and crosstalk by incorporating data on spatial Er variation, local and global trace tolerances, and plating thicknesses, etc. The incorporation of global and local variation data from benchmarking has dramatically improved model correlation to actual performance and allowed designers to better optimize system performance. These characterization results are also being used to target future high frequency performance improvements in the PCB interconnect through a combination of better system designs, silicon design, and industry process improvements.

Benchmarking Philosophy
Intel's approach to Printed Circuit Board (PCB) technology development is multi-faceted. Assessment of the supply base, both technically and commercially is contrasted against the projected product needs to understand what gaps or barriers to product exist. Risk analysis is completed for each gap by examining the gap vs. industry trends and in relation to opportunities to overcome the gaps. Risk analysis is used to determine whether a technology is ripe for intercept in product. At the same time, assessment data is used to update internal design models to better predict performance limits and understand what design tradeoffs can be made and where there is a true need. The understanding of the need for a technology intercept is as important as the readiness of the market to meet it. This approach is depicted in Figure 1.

The key to the whole process is accurate, comparable data. Intel has three primary sources of assessment data: **1**) Surveys and questionnaires, **2**) Test vehicles, and **3**) Product. All three data sources are incorporated in benchmarking activities. **Surveys** are extremely flexible and cover all aspects of the business from cost, availability, quality and technology. Surveys are always a good starting point but require some level of verification to be reliable. Surveys used in conjunction with supplier audits are an integral element in determining the cost and availability of any demonstrated capability determined from test vehicles. **Test vehicles** provide a good method for verification of surveys or "paper data" and gathering data for statistical analysis and technology trends. Test vehicles are utilized to provide sufficient data for product simulation. **Product** data and product qualification data is used to monitor yield and cost and provide a high volume comparison to the test vehicle results. Surveys provide the necessary information for categorizing or defining test vehicle and product data. The benchmarking vehicles Intel uses fall into three main categories: 1) Fabrication capability and tolerances, 2) Material performance, and 3) Design interaction/optimization.

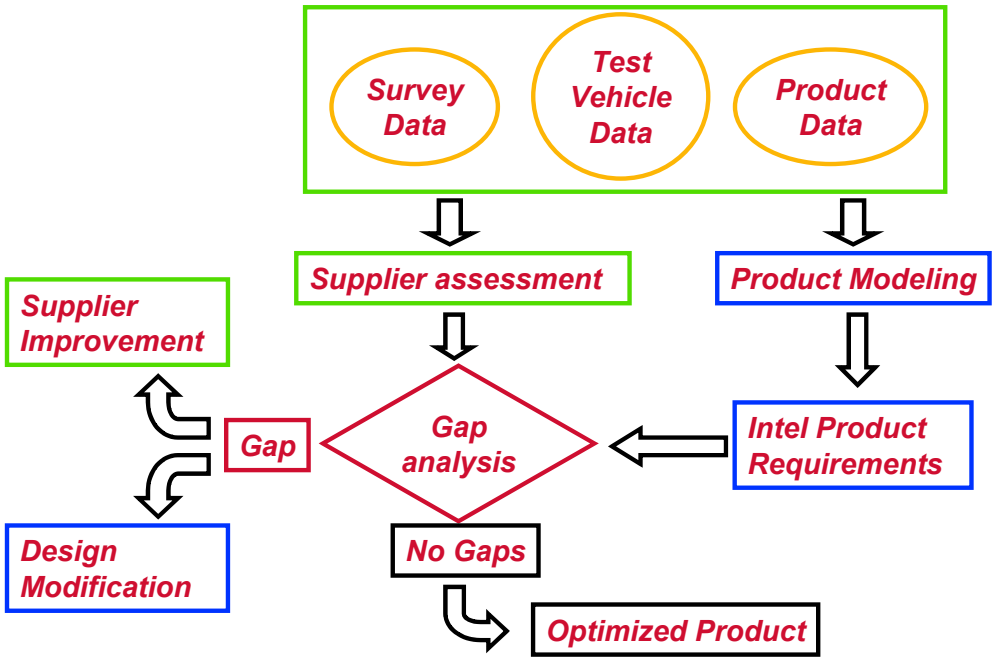

Figure 1 - Benchmark Data Flow

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Fabrication capability testing currently takes the form of using the IPC PCQR^2 database test designs to assess supplier's Process Capability, Quality, and Relative Reliability (hence the name PCQR^2). Product features for specific market segments of interest are matched to the design features of the available test boards. Intel used an internal program of similarly designed test vehicles prior to subscribing to the IPC database. The database designs provide a holistic approach to assessing fabrication capability looking at a range of performance within each category, examining the tolerances, and providing a measure of reliability for the test board. The key to capability data is to collect multiple sets, both from different suppliers and the same supplier at different times. Also key to capability testing is testing each site of an individual supplier and performing a coordinated audit or survey to understand the fabrication capacity represented by the test board. Experience has shown that multiple years of data are necessary to assess technical trends, and testing the same supplier on a periodic basis tends to eliminate special practice issues. The supplier develops familiarity with the testing and delivers results representative of actual production practices, eliminating the J-curve phenomena, Figure 2 (initial good performance, followed by a dip, and then sustained improvement).

Material performance testing takes the form of test board designed to capture electrical, mechanical, and reliability data for the comparison of different materials. The focus of this material evaluation board is material properties and variation, but some measure of process capability such as line widths, registration, and plating thickness are included in the test board to validate fabrication interactions such as via reliability. To improve the understanding of material variation, care is taken to review material variation sources as well as variation between PCB fabricators. For example, in testing laminate materials, testing is performed over multiple treater lots and different builds are designed to exercise the range of glass/resin ratios available.

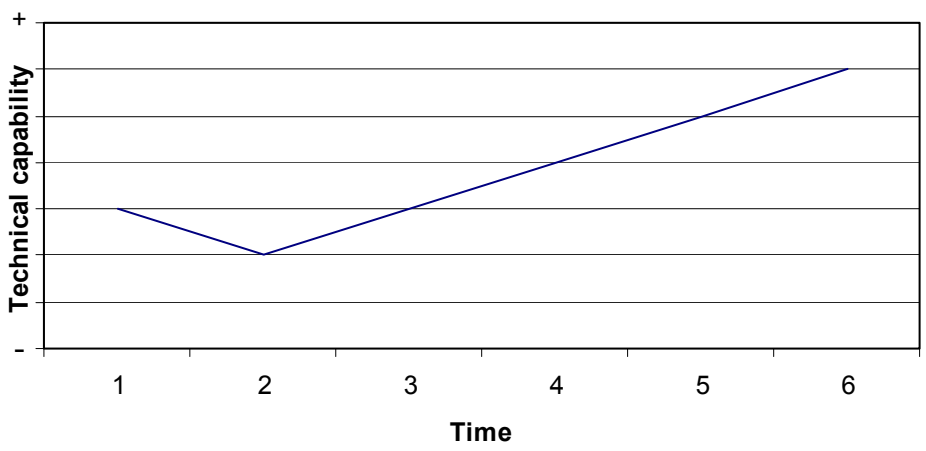


Figure 2 - Historical J-Curve Benchmark Performance

The last category of test vehicles is the design interaction/optimization group. The test boards in this group tend to be more focused on a specific design issue or product format and are optimized to verify performance or investigate potential options. The intent is to collect a lot of focused data with a minimum amount of resources consumed. The designs in this category are specific to the design optimization goal and typically focus on quantifying differences between small design changes.

An important aspect of Intel's testing programs is providing feedback to suppliers and the market on performance. We currently have a Technology Improvement Program where supplier's capability is continually compared to projected technical needs, and suppliers are expected to give feedback and show development plans and progress in meeting those needs. Intel has also shared material, metrology, and equipment feedback with industry participants based on material and focused design testing. The goal is to enable the industry to meet current and future product needs.

Fabrication Capability Board

Fabrication capability testing focuses on both the manufacturing yield and manufacturing tolerance/variation around a target. The goal of capability testing is to determine the maturity of a technology, improve product design tools, and provide input basis for supplier technology improvement plans. Recent uses of the capability test board at Intel include optimizing BGA package pitch, determining optimal anti-pad sizes for reliability, industry capability to control impedance, and maturity of uvia technology. The fabrication capability elements tracked are as follows:

Yield
- Trace/Space by Cu thickness
- Drill registration
- Soldermask Registration

Tolerance Data
- Etch tolerance by Cu thickness
- Cu Plating Thickness by aspect ratio
- Impedance

Target to Nominal
- Trace/Space Average vs. Target
- Impedance Target vs. Trace

Over the years, there has been a natural evolution of the fabrication capability benchmarking activities at Intel. The test vehicles initially were developed internally with designs modified on an annual basis. The initial activities were focused on validating a particular product design and involved only current fabrication suppliers. The current activities rely on the IPC PCQR^2 program. PCQR^2 designs are selected based on match to product design and target markets. Scope has also expanded to include beyond current fabrication suppliers to selecting and sponsoring additional fabricators based on presence within target market segments. The IPC PCQR^2 programs allows for consistent designs over time that allow for better continuity in technology trend analysis. The IPC PCQR^2 program also allows benchmarking to additional fabrication suppliers outside the existing supply base.

In the transition to utilizing the IPC PCQR^2 program, extensive correlation analysis was done between internally developed test vehicle results and IPC PCQR^2 data. The correlation analysis included comparison of metrology

methods, Metrology Capability Analysis (MCA) to quantify metrology accuracy and repeatability, and sample data comparisons of reported nominal values as well as supplier and panel variation for consistency.
Fabrication capability data for each supplier is analyzed and extracted by the PCB technology team into industry status reports for internal design groups, product teams, and commodity management. Care is taken during the analysis phase to review all yield, nominal, and variation data across the reported elements for interactions. If interactions are found, results are adjusted accordingly. The most scrutinized element is the extent of under/over etching. Registration results based on electrical continuity metrology as well as impedance tolerance results and yield are highly influenced by nominal trace width to target differences. Over-etching improves registration by artificially growing the clearance area and impacts impedance co-variance data by shifting impedance higher.

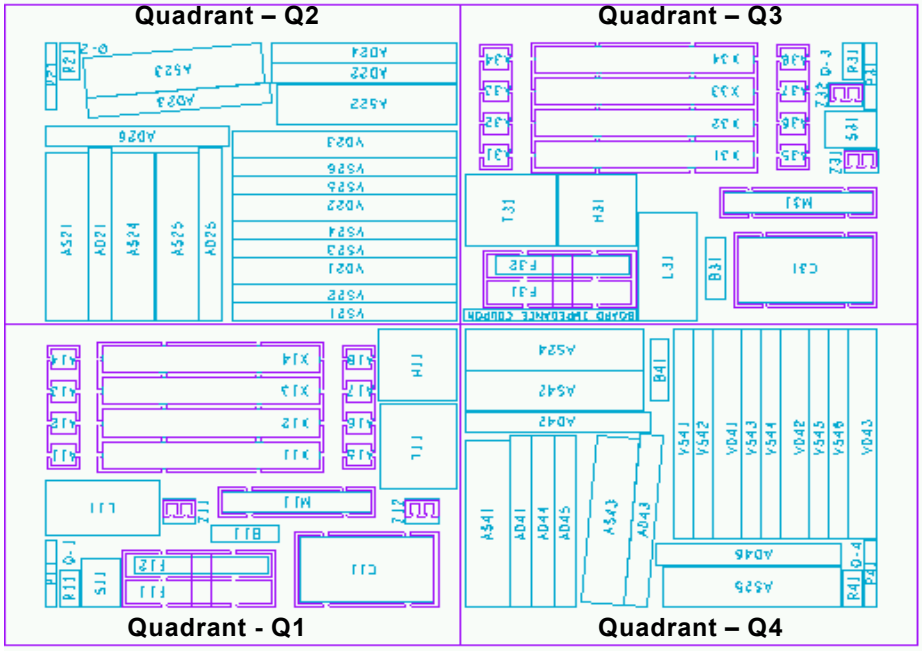
Materials Evaluation Board
Materials evaluation testing focuses on three main areas: 1) Characterizing the electrical properties of the material sets being used, 2) determining the mechanical properties and limitations, and 3) measuring the reliability of the material sets vs. design features. Uses of the test board at Intel include looking at material options for Lead-free assembly and high temperature survivability, high-speed low loss signaling, glass styles, copper foil, new soldermask, and green product (halogen-free). As sufficient data has been captured to provide baseline performance levels, the Material Evaluation Board is now starting to be utilized in assessing impact of process changes to the material properties. Recent examples include assessment of new bonding treatment, new plating process, new drilling equipment, and lamination process changes. The test elements incorporated in the Intel Material Evaluation Board design are as follows:

Mechanical/Physical
- Registration
  - Drill
  - Image
  - Soldermask
  - Material Quality
  - Copper Peel strength
  - Solder mask adhesion
- Via quality
  - X-section
  - Thermal stress
- Thermal Properties
  - T260
  - CTE
  - Tg
- Flex Modulus
- Moisture Absorption
- Trace and space capability

Electrical
- Dk of Material
- Loss
- Impedance control
- SIR/ MIR
- CAF
- Dielectric Withstanding (Hi-Pot)

The design of the Materials Evaluation Board is such that the entire working panel at the fabricator is analyzed. See Figure 3. The test board is segmented into four quadrants (two each for primarily electrical testing and two for primarily mechanical/thermal testing). The quadrants can be separated to facilitate testing of multiple elements at the same time. Further, many of the mechanical coupons are tab routed to remove for individual testing. Test structures are designed to use standard IPC test methods or other industry recognized test practices. Many of the electrical and mechanical tests are performed vs. temperature conditioning to plot properties vs. temperature. Data collection is automated where possible to enhance the magnitude and quality of the data. The intent of the test board is to have a common platform where material sets can be compared and contrasted against each other. Intel has also created a baseline for common materials to which to compare the same material against in the future. The goal is to develop statistically sound material variation data that can be input into design models to accurately predict product performance. The test plan for a particular material would include building multiple lots from different treater lots to capture all the material process variation. Once material variation is established by building at one supplier, builds at multiple suppliers are necessary to capture supplier process influences. The test board design is flexible in that it can accommodate different thicknesses, layer counts, and constructions with minimal editing of the Gerber. Equipment sets needed to evaluate the Materials Test Board include: TDR, VNA, Pull force tester, TMA, DMA, DSC, Optical measuring equipment, cross-sectioning equipment, IST tester, Temperature and humidity chamber, CAT test equipment, Perfect test equipment, Hi-pot tester, scale, tape, and CAF tester. Precision measurements are preferred over quantity, but both are desirable. Samples sizes are a product of risk averseness weighed against resources. A single build would consist of three lots of 10 panels each for a total of 30 panels. Test results are

coupled with survey data on material characteristics and processing conditions to get a complete picture of all material driven issues. Survey data would include processing parameters for the material, material costs, material specifics, and process results. Standardizing our test structures and methodologies allows for greater comparison of results, both within Intel and external.



Coupon Designations

A – X-Section Coupon
AD – Differential Impedance
AS – Single Ended Impedance
B – RF Coupon
C – CAF Coupon
F – Flex Modulus Coupon
H – Hi Pot Coupon
L – Line and Space Coupon
M – SIR/ MIR Coupon
P – Via/Drill Registration Coupon
R – Outerlayer Registration Coupon
S – Soldermask Registration Coupon
T – Cu Peel Strength
VD – VNA Differential Impedance
VS – VNA Single Ended Impedance
X – Via Reliability Coupons
Z – TMA Coupons

Figure 3 - Material Characterization Board Layout

Design Interaction / Optimization Test Vehicle

Design interaction and optimization test vehicles focus on technology integration issues and board assembly risks associated with a particular PCB design recommendation. Each design is unique for the issue being investigated or product design being optimized. Examples include via fill percentage vs. via size for Via-In-Pad (VIP) designs, assembly reliability vs. BGA pad and via pad diameters, line width vs. impedance and loss targets for a specific package routing scheme. Many of these test vehicles are based on DOE principles with the investigation of multiple variables at multiple levels. In some optimization testing, the test vehicle design incorporates many increments of an individual variable. For example, line widths at 0.5mil increments over a range of 5-10mils have been used to optimize trace/space for differential impedance and loss optimization. The results of these optimization test vehicles are used to validate design models to ensure correlation over a wide input range. This is especially important in the non-linear, multi-variable models.

Data Collection Metrics

Capability and material property data is used extensively by system designers to optimize PCB layout and by IC designers to develop solutions for high-speed bus architectures. When designing critical high speed interconnects it is critical to simulate the correct range of expected values. Underestimating the proper range of tolerances leads to designs that may not function properly or lead to issues that limit ability to source product from multiple vendors. On the other hand, over estimating the parameter window unnecessarily constrain the performance and potentially result in higher cost solutions.

Designer's request data tailored to the problem at hand. Daughter Card and Add-in Card designers care about vendor to vendor differences as their product must function when connected to a third party design. Designers optimizing high-speed IO busses between the CPU and memory controller on a single PCB are primarily concerned with variation between individual IO nets on the same PCB. As a result, all data is analyzed and described in terms of its nominal panel value by supplier and variation around the nominal value. Variation data is further broken down into; variation across a single 18x24" panel layer, variation in nominal panel value from board to board within an individual lot, and variation in nominal panel value from lot to lot within an individual supplier. The data analysis is performed so that the three variation components are additive. In many cases, the lot-to-lot variations and board-to-board variations are combined into a panel-to-panel metric for the designers.

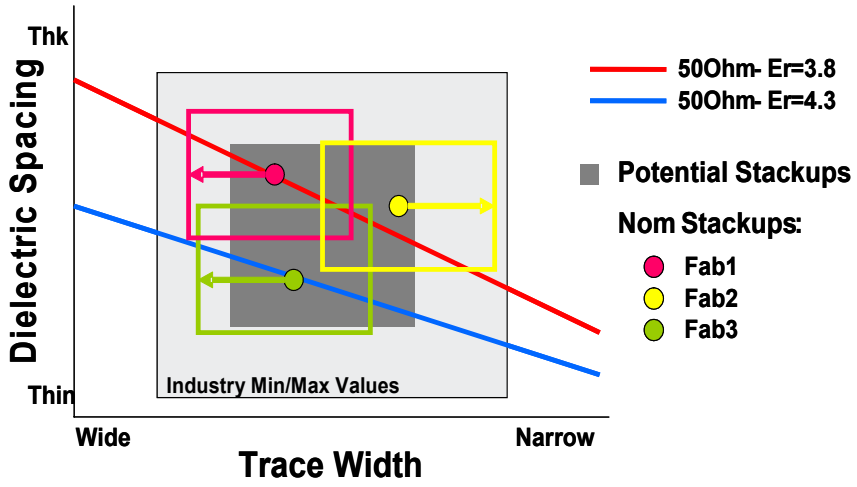


Figure 4 - Industry Range vs. Fabricator Design Space

In the case of impedance control and signal integrity simulations, designers have historically selected the worst-case design corners for analysis from a set of potential stack-ups or applying a tolerance to an optimized stack-up. This meant that designers either only considered one of the vendors shown in Figure 4 or analyzed the full Industry Min/Max ranges both of which had negative design implications. With the new benchmarking metric, designers now perform impedance control and signal integrity simulations by a three-step process. First, the potential stack-up space is determined with input as to the relationships of dielectric material thickness and dielectric constant and supplier allowance for adjusting line widths to meet impedance targets. Second, board-to-board and lot-to-lot variations are used to determine nominal conditions for an individual PCB. Third, the within panel tolerance variation values are included to provide simulation conditions for an individual interconnect or bus. Depending on the goal of the simulation, analysis is then completed on selected worst-case individual PCB scenarios or by performing Monte Carlo simulations across all scenarios.

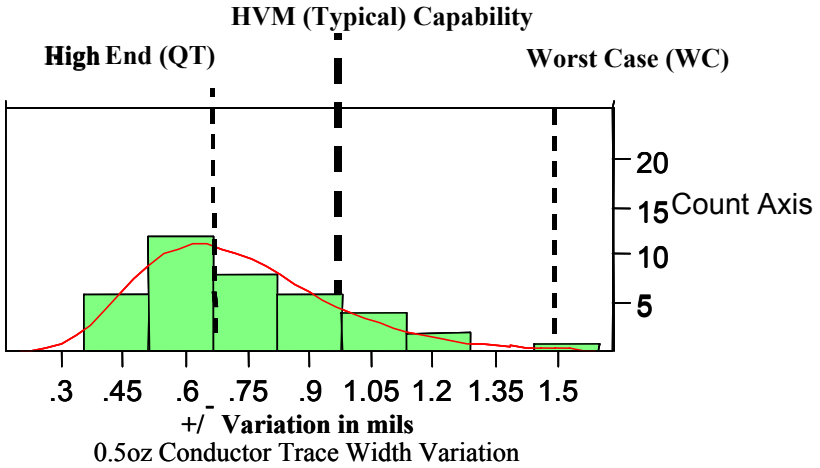


Figure 5 - Sample Parameter Distribution for Industry

Providing designers a single accurate value for a parameter is problematic as different suppliers have different capability and different product teams will target different markets or segments within the supply base based on cost/performance optimization. Within the benchmarking group, the parameter data by vendor is plotted as a distribution as shown in Figure 5. From this industry distribution, three values are determined based on percentile; worst case industry value, high volume capability, and high-end capability. The percentile definitions for each are based on results from cost, availability, and yield data. The spread between the three values are also analyzed in conjunction with survey data for technology trend potential and technology limits. Narrow spread typically indicates a material or process limit while wide spreads generally point to opportunities to improve capability through process controls.

In the past, design teams have also back calculated physical feature tolerances based on what a fabricator claims they can achieve for impedance control. These back calculated or inferred tolerances are usually significantly less than measured through the benchmarking activities. As a result, designers initially did not want to utilize the larger tolerances from benchmarking as they resulted in simulations having lower design margins and models that did not produce impedance simulations that matched fabricator claims. Efforts then proceeded to compare incoming product to benchmark data. By utilizing automated TDR systems, large quantity characterization of incoming product was performed. This included measuring all impedance traces on a PCB, comparing results to coupon results, and tracking variation data across an individual board and within a manufacturing lot and finally comparing results to benchmark data from the same fabrication suppliers. This activity demonstrated that the variation impedances realized on product was indeed higher than expected and that correlation between product and simulation tools was only possible by using benchmark fabrication capability data. Table 1 and Figure 6 demonstrate a sample of differences in claimed capability obtained through survey vs. assessed capability through benchmark efforts for differential impedance.

Table 1 - Differential Impedance Survey Data

PCB Supplier	PrePreg Type		Trace/Space 100ohm Diff	Cost Rank	Supplier Stated Control on Dif Imp
1	2116	6 / 5	4 / 7	2	10% impedance tolerance on all targets
2	2116	5.5	5.25	2	10% impedance tolerance on all targets
3	2116	4	3.5	2	10% impedance tolerance on all targets
4	2116	6 / 8	4 / 8	1	imped tolerance by column: 20%, 15%
5	2116	8 / 10	5 / 12	1	10% impedance tolerance on all targets
6	2116	8/10	5/12	1	10% impedance tolerance on all targets of Dif Imp Lines and <10% on single ended.
7	2116	6.8 / 5.3	5.3 / 6.7	n/a	+/-12% on differential, +/-10% on others.

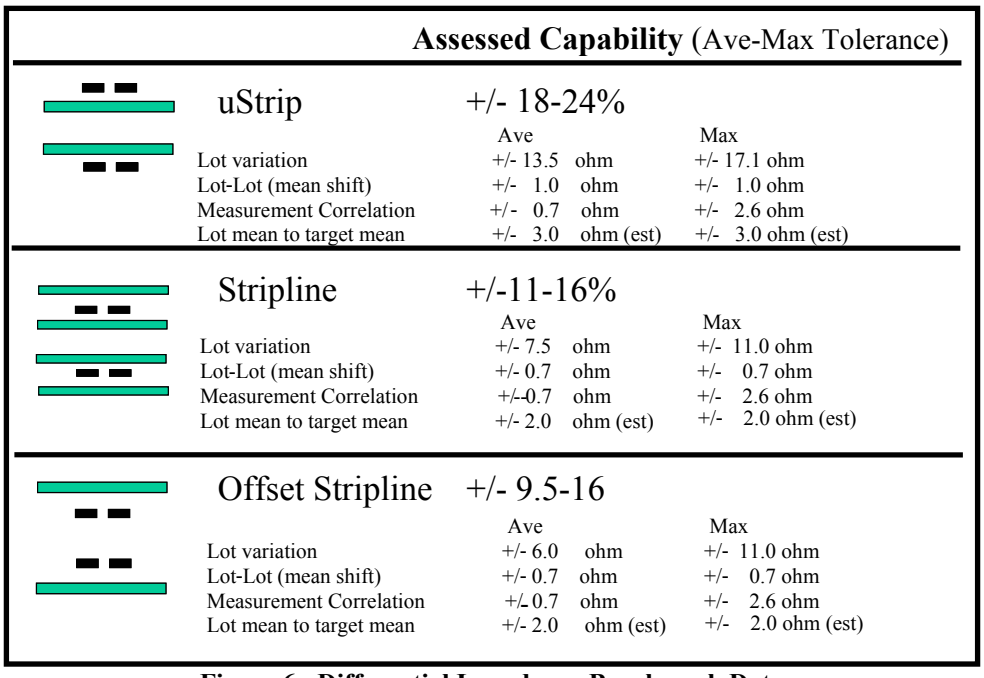


Figure 6 - Differential Impedance Benchmark Data

Summary
Benchmarking activities have greatly improved many facets of product design, supplier management, and technology development. Data on tolerances have improved the ability of signal integrity designers to build models that correlate and reflect what is being built into product and better model the expected differences between multiple material choices. These improved models have helped designers deal with issues before product testing and help develop more accurate technology requirements. Data on yield, capability, and capacity are key elements in identifying when a technology is ready for deployment by end product market. Material characterization benchmarks combined with fabrication capability benchmarks provides key metrics and baseline conditions by which process and material change is managed with supplier and technology development team gauge improvement.

References
1. R. Sakelson, "PCB Database Provides Board Buyers with All the Facts"; Circuitree, July 2002.
2. H. Holden, "The New Printed Circuit Design Framework-Predictive Engineering", Circuitree, Dec. 2000.
3. D. Wolf, T. Estes, R. Rhodes, "Benchmarking PCB Process Capability, Quality and Reliability Becomes a Reality", IPC EXPO 2003.
4. S. Gold, R. Sakelson, "Are PCB Fabricators Ready?" Circuitree, Dec 2000.
5. D. Wolf, T. Newton, "Printed Board Process Capability, Quality and Relative Reliability ($PCQR^2$) Benchmark Test Standard", IPC Annual Meeting Proceedings 2001.
6. W. Chen, B. Bjorndahl, R. DePase, B. Parrish, B. Birch, R. Carter, "PWB Reliability Evaluation Using IST", IPC EXPO 2003.