A Case Study of an OEM's Program to Assess Supplier Capabilities, Technology Availability, and Reliability for Advanced Printed Circuit Boards

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Abstract
Teradyne, Inc. has been involved with Conductor Analysis Technologies, Inc. (CAT Inc.) for over 4 years and the IPC D-36 Subcommittee for over 2 years. This paper describes the initial motivation for selecting "CAT" test vehicles and testing and the project involvement. We relate some of the findings from the latest test project and discuss some of what we have learned. This paper shows a few of the ways that CAT/IPC D-36 testing has been used to determine supplier process capabilities, technology readiness, and design feature parameters. We provide an overview of how supplier management utilizes the test results to evaluate existing and potential suppliers; to drive for quality improvements; and to align parts to suppliers. Last we comment on the strengths and weaknesses of the current state of the program from Teradyne's perspective.

Introduction
How did Teradyne come to be involved with Conductor Analysis Technologies' standardized test vehicles and testing? The initial motivation was for a technology assessment of laser ablated microvias and high aspect ratio plated-through vias, exceeding 10:1 aspect ratios. Teradyne had not yet designed with laser formed blind microvias but new designs were to be so dense with multiples of high-pin count BGAs that microvias would be needed to route the boards. There was no history in the company to extract design rules or quantify reliability. The CAT test method allowed for various microvia structures to be run simultaneously with controlled impedance structures and other important attributes, such as high aspect ratio through holes with signal pad diameter variations, on a suitably complex 24-layer board that would be a close approximation to Teradyne's intended PCBs.

A standardized test board, with multiple levels of values for the technologies of interest, which would be evaluated by 100% electrical testing (efficient, accurate and repeatable), and having a population of sampling sites sufficient to calculate levels of defects per million opportunities (DPMO) by feature and value was ideal to answer our questions: How robust is this technology; what should be the design rules; and who can do it? Our expectation was that CAT testing could provide the data to establish the supply base capability; the data to inform the design decision on what types and geometries of microvias to use, and would be the test vehicle to qualify suppliers for microvias.

The Initial Projects
Teradyne and CAT designed a process capability panel, unique to Teradyne, to test certain design parameters in increments until the feature of interest would fail, thereby establishing the actual process limits. Three suppliers participated in this exercise. All three suppliers had previously indicated that the feature parameters were within their process capabilities.

The data showed high defect levels indicating poor manufacturing capability at the values which were the initial design targets, especially for the microvias. One-layer deep microvias (Layer 1 to Layer 2 connection; "Level 1 microvias") at 0.5:1 aspect ratio (hole depth divided by hole diameter) yielded moderately, but nothing with a higher aspect ratio was acceptable. Two-layer deep microvias (Layer 1 to Layer 3 connection; "Level 2 microvias") had unacceptable defect density levels at all aspect ratios. The design rules were changed to limit microvias to one-layer deep and not less than 0.006" diameter or greater than 0.5:1 aspect ratio. Design rules were also adjusted for minimum PTH size, minimum pad diameter, and minimum outer layer spaces.

By the second process capability design, 8 suppliers would "sign up" to submit panels. This time the element of stress testing was added to gauge reliability and complement the static continuity testing. A subset of the panels would be measured for via net resistance values then subjected to 3 assembly heat cycles. Those nets would then be measured again recording the absolute resistance, the delta resistance, and the percentage of nets exhibiting a 5% or greater resistance increase.

The IPC and CAT Partnership

The formation of the partnership between CAT, Inc. and IPC to develop an industry standard for process capability test panel designs (IPC-9151) and a database of printed circuit board supplier capabilities was welcomed and supported by Teradyne, which purchased an OEM annual subscription to the test service and database.

The proposed Printed Circuit Process Capability, Quality, and Relative Reliability database ($PCQR^2$), populated with the test data from many suppliers could provide a view to inflection points in the industry for various design features and criteria. This would assist us to align the use of technology to our customer requirements without compromising cost or reliability. These inflection points could constitute an industry design for manufacturability guide for higher yielding designs. Our thinking was that higher yielding designs would be more cost-effective for Teradyne, would improve our product reliability in the field, and would aid predictable deliveries while providing an opportunity for suppliers to make a reasonable return.

Additionally, the database would allow us to impartially benchmark our suppliers to the industry based on data. That data would come from a repeatable parametric test process with all suppliers manufacturing identical boards. This would be true for our advanced design suppliers, but would also provide a wealth of information for suppliers in the lower technology segments.

The IPC-24-125-HB Project

When the 24-layer high technology test vehicle design data and specification was released, Teradyne had 9 suppliers who were eager to prove their process capabilities and product quality by making and submitting the required number of panels to CAT testing. Teradyne's Enabling Technology group had a clear deliverable to the company for the return on the subscription investment: to report on the technology parameters and capable suppliers for high aspect ratio holes and blind microvias in time for a new product design.

We learned, again, that although all the suppliers' literature claimed "volume" capability in all or most of the technologies, putting those technologies together onto one 24 x 18" test vehicle was very challenging. It was 20 to 26 weeks from the release of the IPC-24-125-HB design to the suppliers before they shipped their first good batches of boards. Today we pre-qualify suppliers through a rigorous interview in an attempt to determine if they do in fact have the process underpinnings to succeed, hopefully minimizing lost time to both of our resources and to our schedule.

Once we had the data and reports from the suppliers who had submitted the required number of panels, we concluded that the suppliers' demonstrated performance frequently did not match their posted capabilities. We believe that suppliers genuinely overestimate their capability based on limited quantitative data for the newer or more demanding technology attributes. With no or very little data it is not possible for them to project DPMO or sigma levels. And so the results, usually less than the supplier expected, were mostly a surprise. Those results also had ramifications to our Approved Supplier List and the Technology Roadmap, which will be discussed later.

For the technology which initially drew us to CAT testing, the laser ablated microvias, the new test data indicated progress had been made. However defect levels for some microvias were still too high. It would be entirely possible for inadequately plated vias to make it through the suppliers' electrical testing - which would decrease Teradyne's assembly yields and even potentially escape to the field, a risk to quality and customer satisfaction. We were also concerned that the suppliers' yields would be too low for them to produce our products at competitive prices with reasonable margins.

For Level 1 microvias, the data indicated that at 0.75:1 aspect ratio the capability of our supply sample stratified into those who could and those who couldn't. There were less than half, only 4, who could deliver less than 100 DPMO at 0.5:1 aspect ratio. At 1:1 aspect ratio there was only one supplier who could deliver quality Level 1 connections with less than 100 DPMO, and only 3 in total with less than 1000 DPMO.

Assessing the data for the PTH vias we found an outstanding supplier who could deliver up to 12.5:1 aspect ratio with 0 DPMO, and an additional 2 suppliers that could deliver up to 10.4:1 at 0 DPMO. The stratification that we saw in the microvias was becoming apparent here also: a group who could, a group who couldn't, and a group that might make the top tier with some process improvement projects.

At this point we could take a snapshot and identify those suppliers who were basically good at making and plating holes (Table 1), but there were some interesting twists. One supplier who was very good at all the PTH and Level 2 microvia aspect ratios nevertheless was struggling with the Level 1 microvias with greater than 0.5:1 aspect ratio. Another supplier who was very good at all the aspect ratios for the Level 1 and Level 2 microvias, had trouble at the 10.4:1 PTH aspect ratio. Given the process, material, and equipment variables that go into "holes" these seeming contradictions can be explained (consider: type of laser; horizontal or vertical microvia plate; prepreg selection; pulse or non-pulse plate; a panel strike plate process, etc.). An obvious lesson here is that capability in one "style" of via doesn't necessarily extend to capability in other via structures.

Table 1 - DPMO for Holes by Supplier , Type and Size

Supplier #	PTH via diameter				Level 1 microvia diameter				Level 2 microvia diameter			
	.010"	.012"	.0135"	.0145"	.003"	.004"	.005"	.006"	.007"	.008"	.009"	.010"
1	73	15	0	0	3977	2120	517	78	66	28	19	9
2	44	0	0	0	18762	3356	158	0	3905	28	0	19
3	205	73	44	44	581	84	39	28	699	57	19	19
4	1630	15	0	0	3287	17	11	6	569	917	748	518
5	2947	1013	268	173	2355	576	238	90	308	566	30	20
6	0	0	0	0	112	39	6	11	9	0	0	0
7	30	0	0	0	235	34	6	0	117	19	19	0
8	250	176	44	44	6	0	0	0	209	0	0	0

PTH vias into .125" thick 24 layer MLB, ~ 68.8K vias per diameter, total population.
L1 microvias .003" deep, ~ 36k vias per diameter, total population.
L2 microvias, .007" deep, ~ 20.4k vias per diameter, total population.

The conductor, space, and conductor height capability data was similarly analyzed, with subgroups of inner layer and outer layer; then within inner layer by half and one-ounce per square foot copper foil weights. All suppliers were capable at down to 0.005" lines and most could also do a credible job at 0.004", but we found that only 3 could really lay claim to 0.003" wide external trace capability.

Spaces, however, were an entirely different story with only 1 supplier that could deliver less than 100 DPMO on a 0.007" space (we were taken aback by that; it was much worse than anticipated). Most of the suppliers who had low DPMO on the 0.007" spaces had low but fractionally higher DPMO on the 0.006" spaces. At 0.005" spaces only 3 could deliver at less than 1000 DPMO. (Table 2)

Table 2 - DPMO for Outer layer Spaces by Supplier

Supplier	.005" Space	.006" Space	.007" Space
-	4738	391	306
'	663	451	317
/	1354	1077	1563
\	832	522	526
*	37826	1094	44
#	1083	306	131
~	2327	349	219
=	258	130	131

Outer layer conductor height variation was a major supplier-to-supplier variable. Not only was there significant variation (process capability, Cp, less than 1.0), with only one exception, but mean value also varied considerably supplier-to-supplier, with over a mil of difference from the lowest to the highest nominal value. This would in turn limit the capability for controlled impedance surface microstrip lines.

Almost all suppliers had a 0 DPMO for all inner layer conductors on 1 ounce copper foil; only 2 did not have perfect scores, but they did achieve less than 100 DPMO. Defects increased modestly when the foil thickness was 1/2 ounce. All but one supplier could deliver to less than 100 DPMO down to 0.003" wide conductors. Counter intuitively, spaces on 1 oz. copper were also higher yielding than spaces on 1/2 oz. copper.

Inner layer trace height variation was minimal with most process capabilities at or exceeding 2.0 Cp. Although two suppliers had particularly low minimum thickness values, maybe due to rework since the Cp for the lot was also low. Similar to the "holes capability" we could take a snapshot and identify those suppliers who were basically good at making conductors and spaces.

Looking for the suppliers who could or could not make "everything we could throw at a board" we simplistically lumped all vias together and all lines together and summed the DPMOs. When looking at this list the 3 tiers of suppliers become apparent (those who can, those who are struggling, and those who can't). This little chart, Table 3, also illustrated to a non-technical audience why not all technologies should be at state of the art on the same board. No supplier has every process at state of the art capability (although Supplier "A" is clearly an exception being at the forefront on both via and line process capability).

Table 3 - Total DPMO by Supplier

Supplier	Lines DPMO	Holes DPMO	Total DPMO
A	46	649	695
B	3839	498	4337
C	2951	1892	4843
D	4408	748	5156
E	814	7718	8532
F	184	8505	8689
G	551	12533	13084
H	5	27091	27096

There are many data points in a typical report and many interactions or angles from which to view those data. Different views of the data might provide information more relevant to a particular OEM. Another capability which we had been discussing, and for which some suppliers' stated capabilities seemed to indicate we might be able to tighten our design rules, was on pad and clearance diameters for the vias - but the data didn't support reducing pad sizes. Improvements in registration were lagging, or so it seemed to us. Not only did the data not support reducing pad sizes, it pointed to larger pads as being more prudent. Innerlayer pad registration would prove to be a major issue for producing multilayers with higher layer counts.

We did discover, however, that target pads for microvias could be slightly reduced. We attributed the tighter registration window to the short travel distance to the target layer, the top-down registration using optical alignment techniques, and the lack of drill wander.

Controlled impedance results were not encouraging. Even at +/- 10% of nominal, Cp on 0.005" surface microstrip lines was less than 1.0 for all but 1 supplier. Most faired reasonably well at 0.005" symmetric striplines and edge-coupled differential symmetric striplines, but half that group fell out at broadside coupled differential striplines. These results clearly indicated a capability gap to design engineering's requests for tolerances of +/- 7.5 or 5%, and confirmed our guidance to avoid routing critical signal lines on outer layers.

Simulating Early Infant Mortality and Reliability

Adding a stress test of 6 reflow simulations provided a screen for robustness of the total interconnect: the sum of the lamination, hole formation, and plating influences on a hole's ability to survive assembly operations. This stress test afforded a comparative measure between the suppliers' PCBs for propensity to early interconnect failures.

Looking at the pre and post stress resistance readings for the 0.0145", 0.0135", and 0.012" drill size PTH via nets, the readings show little change; however the 0.010" drill size via nets from some suppliers had changed dramatically, with some nets showing resistance changes up to 25 ohms in one case; 19.8 ohms in another; and 2 more at greater than 5 but less than 10 ohms. For those boards which had nets with resistance increases, anywhere from 12 to 24% of the nets exhibited a resistance change of greater than 5%.

The data from the stress test on the blind microvias was disquieting. The Level 1 microvias from this group of suppliers varied from mostly good except for 2 suppliers on the 0.6:1 aspect ratio with a 0.005" via, to only 2 suppliers with less than 5% resistance change on the 0.75:1 aspect ratio with a 0.004" via (Table 4). Many nets

involved in the higher resistances increased by over 25 ohms (with some catastrophic failures now evident) and up to 60% of the nets were impacted. For the 0.003" diameter via with a 1:1 aspect ratio there was only one supplier whose vias did not increase in resistance after stress test. Reviewing the post-reflow results to the continuity tests on the as received PCBs, we determined that there was correlation. Suppliers with high DPMO on continuity also had large resistance changes and many nets impacted with these higher resistances. Lower quality vias as indicated by high DPMO scores on panels as received would translate to lower reliability as indicated by higher resistance changes on many nets on the panels after 6x assembly simulation.

Table 4 - Net Resistance in Ohms by Supplier
Pre and Post 6x Reflow

Supplier	As Recv'd Max net R	Post Reflow Max net R	% Nets >5% Inc R
S	18.1	115.2	20
T	1.8	8.8	16
U	15.0	60.6	60
V	1.1	27.6	19
W	1.0	0.3	0
X	1.1	0.8	0
Y	1.8	36.2	5
Z	17.6	72.2	67

Data for .004" vias, .003" deep (0.75:1 aspect ratio)
~ 36k vias; 232 vias per net

The results were discussed with each supplier in turn both in their absolute numbers and in a relative manner by relating if they were generally better than, worse than, or similar to other suppliers. From these discussions we believe we identified two additional elements that contributed to either better than or worse than results.

Suppliers who had implemented Interconnect Stress Test (IST) as a process or product quality assessment tool had better overall via test scores than those who had not. We attributed the robustness of their holes to the advantage of having a quantitative (cycles to failure) measure of the interconnect, and then using that data (increasing or decreasing cycles to failure) to isolate and then optimize various process or material options.

The other element that segmented the suppliers into groups was the choice of laminate and prepreg by brand. Suppliers were allowed to select any "FR-4" material to build on, and reported the material used. Suppliers using a particular brand of material generally had higher DPMO on the higher aspect ratio holes. The correlation of aspect ratio and reliability by material type was later validated outside the CAT/IPC process and an appropriate change was made to Teradyne's approved laminates' list.

Teradyne PCB Technology Roadmap, Risk Assessment Process, and Design for Manufacturability
The data from the testing is summarized in graphical format and presented to Design Engineering; in fact Design Engineering now has representation on the team that administers the program. Based on the high quality of information received in prior CAT tests, Design Engineering staunchly supports continuation of the program and some decisions regarding specific design details are held back until the data are in.

Operations and Design Engineering now have agreement on risk levels for new or state of the art technologies, based on the data.

Several items which are tracked on internal PCB technology roadmaps were more realistically aligned to the demonstrated capabilities, and the projected availability dates for some new technologies or technology extensions were pushed out to later time periods. The Roadmap is a key communication tool to and with senior management in Operations and Engineering and is used in part to determine gaps to future design needs – those gaps being now more evident and at an earlier date. This in turn fosters risk reduction plans to either design out or around the technology or to kick off a development project with a selected supplier partner.

After a review of the capability indices of the supply base as a whole, CAD design rule constraints are codified and those parameters become the current Design for Manufacturing (DFM) requirements.

Supply Base Management
Based on the data from the initial projects that one of our suppliers had vias that were prone to rapid and catastrophic degradation after assembly simulation, Teradyne stopped putting any new part numbers or significant reorders into that particular facility. The data, coupled with the supplier's unwillingness to accept the validity of the results and provide corrective actions, drove us to this decision.

These parts were in turn resourced to another facility which had done well, commensurate with the requirements of the parts we were resourcing. Actually over the past 2 years as various suppliers or particular facilities have been decommissioned, our resourcing strategy has been guided, in part, by CAT test results.

After the last round of testing on the IPC-24-125-HB, one supplier who did well in most categories but was lagging in one, took it upon themselves to improve. They came to us and said: "we know we can do better than that", and "we know that's not good enough" and proposed a corrective action plan to remedy their performance and demonstrate process improvement - which they subsequently completed. Another supplier who had very poor results in a particular category reported that they had tried "something new" with these lots - that this wasn't representative of their normal and usual process. After impressing on them that a process benchmarking test vehicle was not the ideal method to proof out new processes, we agree with a corrective action plan both for the lack of rigor in making the decision and for the lack of quality in the parts submitted. They currently have their capability capped at below the IPC-24-125-HB design parameters pending comprehensive corrective actions.

At this time any new supplier or new facility for an existing supplier, or supplier capability rating upgrade needs to be preceded with submittal of the appropriate level of CAT/IPC test vehicles. And so in addition to technology availability assessment, reliability risk assessment and supplier process capability assessment, we have now expanded the utility of the CAT/IPC test vehicles to that of qualification test vehicle.

Teradyne's Supply Line Management organization assigns a technology code to every new or reissued part number. Also every supplier is assigned a capability code corresponding to their rating on the Supplier Capability Index, which is a summarization of key elements of the CAT/IPC test scores. New designs can be bid only by suppliers with capability codes aligned to the part's technology code.

The IPC-36-250-HB Project
The IPC-36-250-HB design is a 36-layer board which is .250" thick and has 18.5:1 plating aspect ratios. It is currently being built under Teradyne sponsorship at several suppliers, some who are on our approved supplier list and others, potential suppliers, who profess leadership in this technical segment. Our future high end work will be awarded to the one or ones who can show the best process capability for these foundation processes.

There are attributes that we envision on our future designs that are not incorporated into the IPC-36-250-HB design for various reasons. These additional process capabilities will be developed with the suppliers who "make it" in the CAT/IPC preliminary selection.

Future Needs
One of the strengths of this program, the standardization of the test vehicles, is also a weakness in terms of not being flexible to model the particular combinations of technologies that are used on any particular segment of our products. Another strength, the statistical validity of the defect level projections, is also a weakness in terms of the sheer number of panels that need to be provided. Thirty panels of high performance laminate materials at 36 layers is a substantial cost and one that suppliers cannot frequently repeat; also the cycle time to produce the panels is significant.

We would encourage development of mini-lots or mini-test vehicles in combination with highly accelerated thermal stress coupons to fine-tune some of the interactions, for instance the stackup; or a particular material selection; or some of the secondary processes. These would augment, not replace, the process capability panels which would form the baseline against which to compare results for changes to the materials or feature specifications.

Summary
Over the past 4+ years Teradyne has benefited as the understanding of the power and utility of standardized testing has become embedded in our culture. The CAT/IPC test vehicles have given us the data to make informed technology deployment decisions; the data to determine higher yielding design parameters; and a de facto early

involvement program that brings elements of Engineering's next design technologies to our supply base earlier in the design cycle. This affords us some time to either work out process development issues or determine if, at the current time, there is a quality or reliability risk that is unacceptably large. It allows the suppliers to exercise the fabrication learning curve earlier, make inputs to increase manufacturability, and hence increase yields which results in a win-win outcome of higher supplier margins and lower OEM costs.

The database provides an impartial and level method to assess suppliers' capabilities and points to areas that need improvement projects. The data can be summarized according to what is important to an OEM and reduced to indices of capability by supplier by technology element; these are useful to align new part numbers to the most able set of suppliers.

A CASE STUDY OF AN OEM's PROGRAM TO ASSESS SUPPLIER CAPABILITIES, TECHNOLOGY AVAILABILITY, AND RELIABILITY FOR ADVANCED PRINTED CIRCUIT BOARDS

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TERADYNE, INC.

Technical Conference
IPC Annual Meeting
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PCB SUPPLIER CAPABILITY ANALYSES

OVERVIEW:

- BACKGROUND
- INITIAL PROJECT GOALS
- INITIAL PROJECT FINDINGS
- CAT / IPC STANDARDIZATION
- IPC-24-125-HB PROJECT GOALS
- IPC-24-125-HB PROJECT FINDINGS
- USING THE IPC-24-125 HB DATA
- IPC-36-250-HB PROJECT DESCRIPTION
- FUTURE NEEDS
- SUMMARY

PCB SUPPLIER CAPABILITY ANALYSES

BACKGROUND:

PAST COMPANY PRACTICE FOR THE INTRODUCTION OF NEW PCB TECHNOLOGY WAS TO:

1. **SELECT ADVANCED OR DEVELOPMENT FEATURES FROM KEY SUPPLIER'S CAPABILITY LISTS AND ROADMAPS…**
2. **INCORPORATE "ALL OF THE ABOVE" IN A SINGLE 16.0" x 20.0" x 0.125" PCB…**
3. **BUY A FEW, POPULATE, POWER UP, RELEASE TO PRODUCTION**
4. **WORK FRANTICALLY WITH PCB SUPPLIERS TO RESOLVE PROBLEMS DURING PRODUCT RAMP!**

PCB SUPPLIER CAPABILITY ANALYSES

INITIAL PROJECT GOALS:

- PROACTIVELY ASSESS RISKS AND INFORM THE DESIGN RULE DECISIONS FOR 1999/2000 PLATFORM BOARDS WHICH WOULD HAVE MULTIPLE 1.27mm BGAs
- "CAT" METHODOLOGY SELECTED TO TEST:
  - LASER FORMED BLIND VIAS
  - 10:1 ASPECT RATIO THROUGH VIAS
  - SOLDER MASK REGISTRATION
  - HOLE TO INNER LAYER PAD REGISTRATION
  - ON 24 LAYER 16.0" x 20.0" X .125" CIRCUIT

PCB SUPPLIER CAPABILITY ANALYSES

INITIAL CAT PROJECT FINDINGS:

- DATA INDICATED LOW CAPABILITY FOR THE INITIAL DESIGN ATTRIBUTES
  - DESIGN/CAD RULES WERE CHANGED TO:
    - RESTRICT DEPTH AND ASPECT RATIO FOR LASER VIAS
      - LIMIT BLIND VIAS TO ONE-LAYER DOWN
    - INCREASE MINIMUM DRILL SIZE ON BGA THROUGH VIAS
    - INCREASE OUTERLAYER TRACE/SPACE MINIMUMS
    - INCREASE VIA “PAD STACK” DIAMETERS
- VIA DEFECT DENSITIES CAUSED CONCERN FOR RELIABILITY
  - ADDED VIA RESISTANCE TEST
    - COMPARE NET R “AS RECV’D” TO AFTER 3 REFLOWS

PCB SUPPLIER CAPABILITY ANALYSES

CAT / IPC STANDARDIZATION:

- WE WELCOMED THE FORMATION OF AN INDUSTRY STANDARD FOR TEST METHODOLOGY AND TEST VEHICLES
- OUR EXPECTATIONS AND MOTIVATIONS
  - DETERMINE INFLECTION POINTS FOR TECHNOLOGY IN INDUSTRY
  - OPTIMIZE USE OF TECHNOLOGY IN OUR DESIGNS
    - REDUCE TIME TO VOLUME
    - INCREASE INITIAL QUALITY & LONG TERM RELIABILITY
    - INCREASE COST- EFFECTIVNESS USING YIELD AS AN INDICATOR
  - BENCHMARK OUR SUPPLYBASE AGAINST THE INDUSTRY

PCB SUPPLIER CAPABILITY ANALYSES

IPC-24-125-HB PROJECT GOALS:

- PROACTIVELY ASSESS RISKS AND DEVELOP DESIGN RULES FOR 2003/2004 PLATFORM BOARDS WHICH WOULD USE MULTIPLE 1.00 mm BGAs
- IPC-24-125-HB SELECTED TO TEST:
  - LASER BLIND VIAS (REVISIT)
  - CONTROLLED DEPTH DRILLED BLIND VIAS
  - > 9:1 UP TO 12.5:1 ASPECT RATIO VIAS
  - HOLE TO INNER LAYER PAD REGISTRATION
  - SOLDER MASK REGISTRATION
  - CONTROLLED IMPEDANCE VARIATION
  - NET RESISTANCE AFTER ASSEMBLY “PRECONDITIONING”
  - ON 24 LAYER 18.0” x 24.0” X .125” PANEL

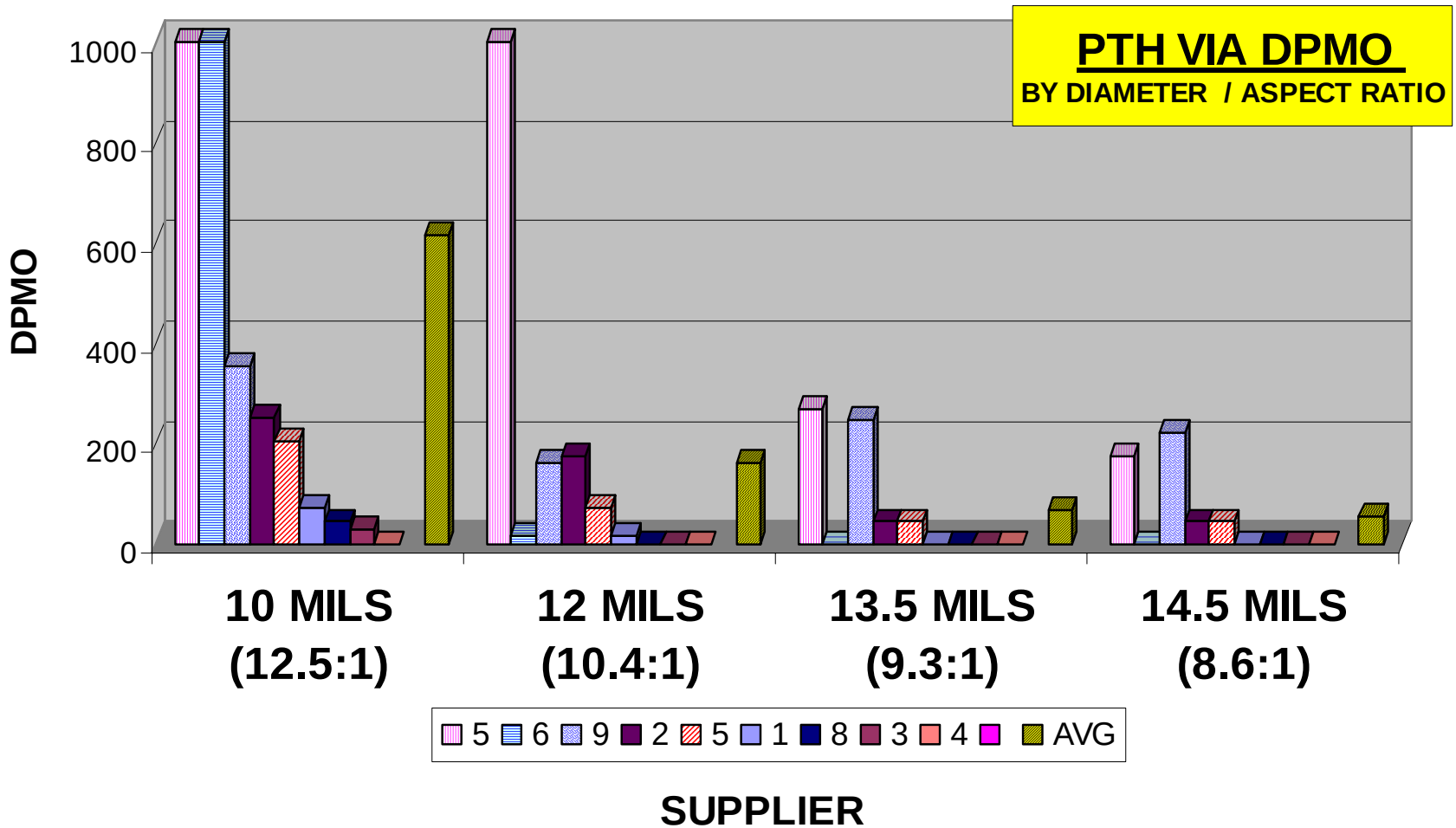
PCB SUPPLIER CAPABILITY ANALYSES

IPC-24-125-HB FINDINGS

- SUPPLIERS DEMONSTRATED PERFORMANCE DID NOT MATCH POSTED CAPABILITIES (AGAIN)
  - SUPPLIERS OVERESTIMATE CAPABILITIES
- DEFECT LEVELS FOR MICROVIAS BETTER BUT STILL TOO HIGH
- 10:1 ASPECT RATIO VIAS MUCH BETTER
  - 12:1 NEW DIFFERENTIATOR
- NO SIGNIFICANT IMPROVEMENTS IN
  - HOLE TO PAD REGISTRATION
  - OUTERLAYER MINIMUM LINE/SPACE/LINE
  - SOLDERMASK REGISTRATION
  - IMPEDANCE CONTROL TOLERANCE

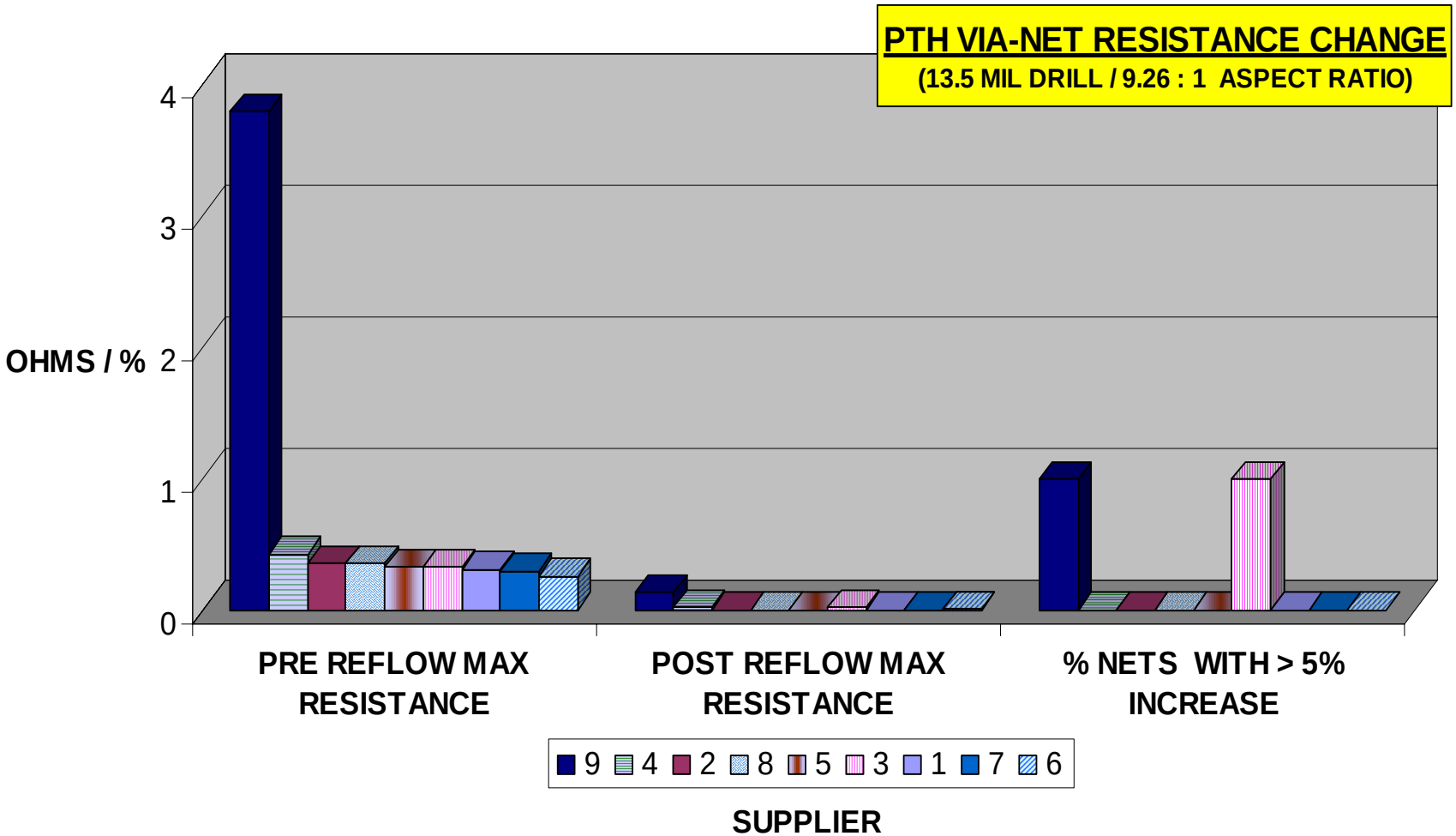
PCB SUPPLIER CAPABILITY ANALYSES

IPC-24-125-HB FINDINGS



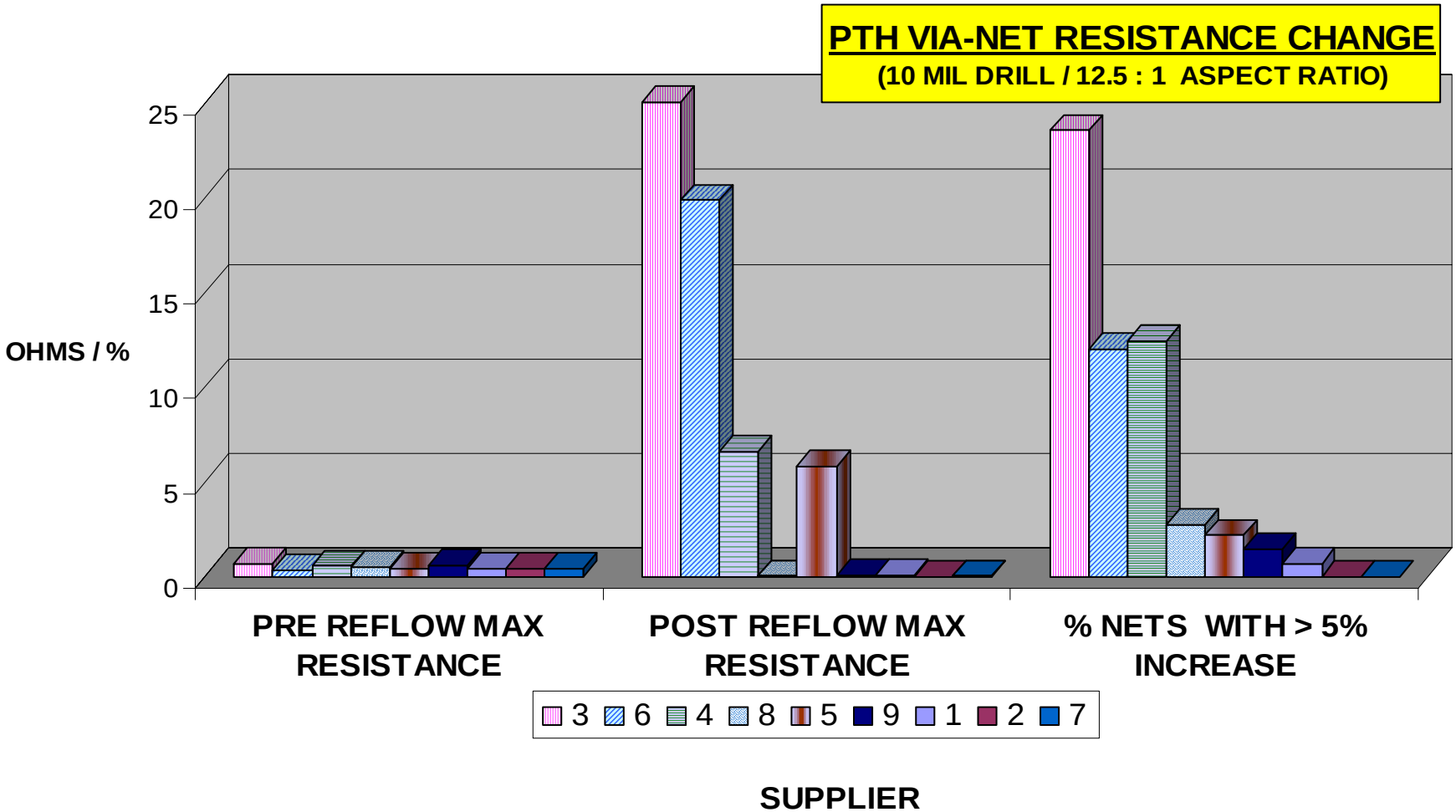
PCB SUPPLIER CAPABILITY ANALYSES

IPC-24-125-HB FINDINGS



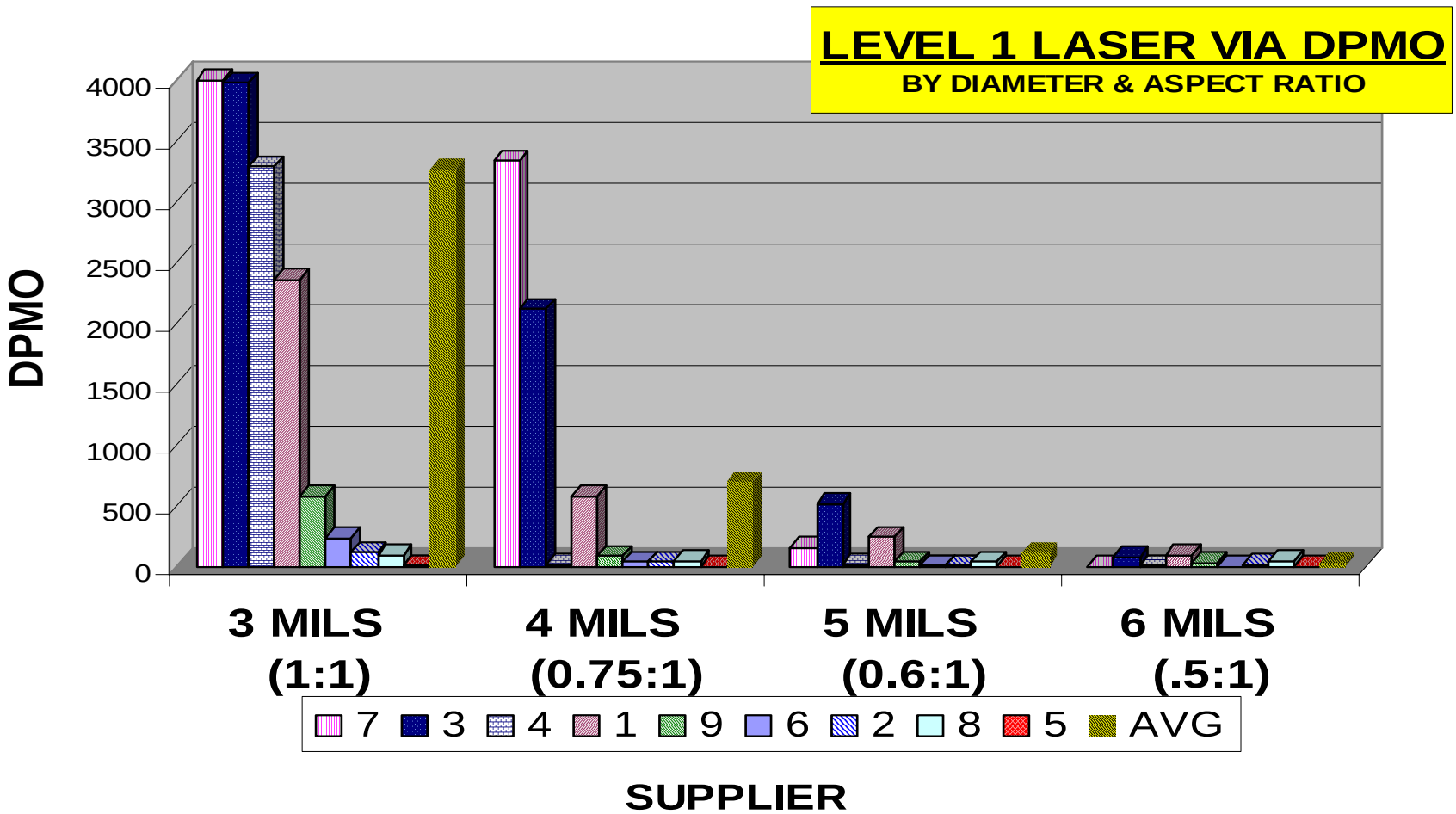
PCB SUPPLIER CAPABILITY ANALYSES

IPC-24-125-HB FINDINGS



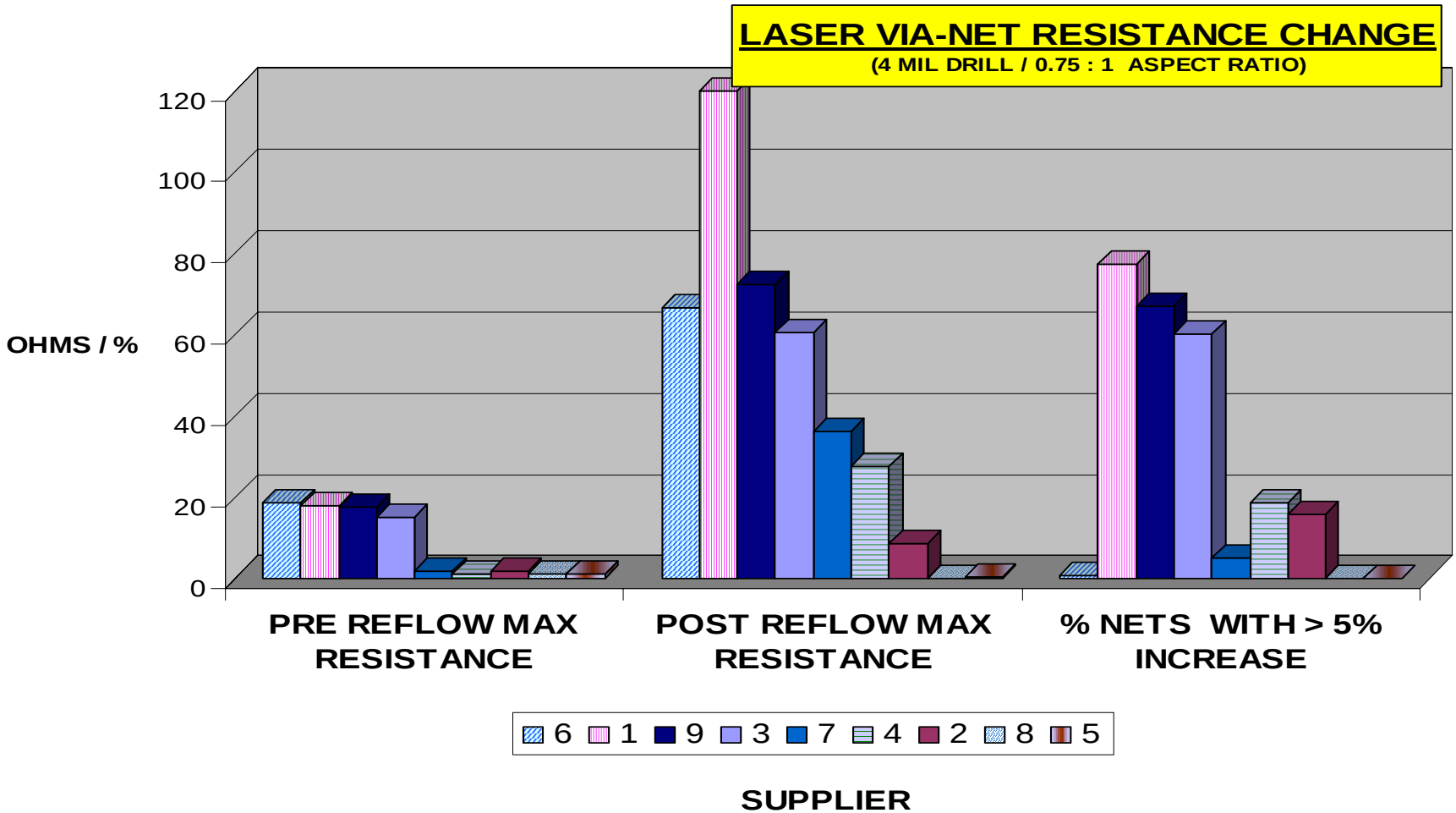
PCB SUPPLIER CAPABILITY ANALYSES

IPC-24-125-HB FINDINGS



PCB SUPPLIER CAPABILITY ANALYSES

IPC-24-125-HB FINDINGS



PCB SUPPLIER CAPABILITY ANALYSES

USING THE IPC-24-125 HB DATA

- "2002 PCB SUPPLIER CAPABILITY ASSESSMENT"
  - (SOME GRAPHS IN THIS PRESENTATION ARE EXTRACTS)
    - ALLEGRO/VALOR DRCs (SEE EXAMPLE OF LINE/SPACE PAGE)
    - DFM GUIDELINES
- SUPPLY BASE MANAGEMENT
  - SUPPLIER CAPABILITY INDICES
    (SEE EXAMPLE OF CONTROLLED IMPEDANCE INDEX)
  - NEW SUPPLIER QUALIFICATION
  - EXISTING SUPPLIER TECHNOLOGY "UPGRADE"
  - PART QUOTATION AND SOURCING
- INFLUENCE DESIGN
  - PCB TECHNOLOGY ROADMAP
    - GAP ANALYSIS
      - DEVELOPMENT PROJECTS

PCB SUPPLIER CAPABILITY ANALYSES

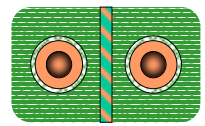
USING THE IPC-24-125 HB DATA

TRACE SPACE DESIGN RULES:

OUTERLAYERS

TRACES:	.003”	.004”*	.005”	.006”
SPACES:	.005”	.006”*	.007”	

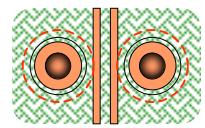
1 TRACK ROUTING



INNER LAYER – 0.5 Oz

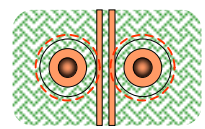
TRACES:	.002”	.003”*	.004”	.005”
SPACES:	.003”	.004”*	.005”	

2 TRACK ROUTING
1.27mm Pitch



6 / 4 / 5 / 4 / 6
(Mils)

2 TRACK ROUTING
1.0 mm Pitch

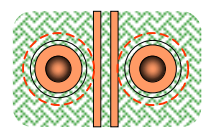


4.5 / 3 / 4 / 3 / 4.5
(Mils)

INNER LAYER – 1.0 Oz

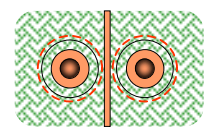
TRACES:	.003”	.004”*	.005”	.006”
SPACES:	.003”	.004”*	.005”	

2 TRACK ROUTING
1.27mm Pitch



6 / 4 / 5 / 4 / 6
(Mils)

2 TRACK ROUTING
1.0 mm Pitch



6 / 7 / 6
(Mils)

** (USE ONLY FOR LIMITED ESCAPE ROUTING)*

PCB SUPPLIER CAPABILITY ANALYSES

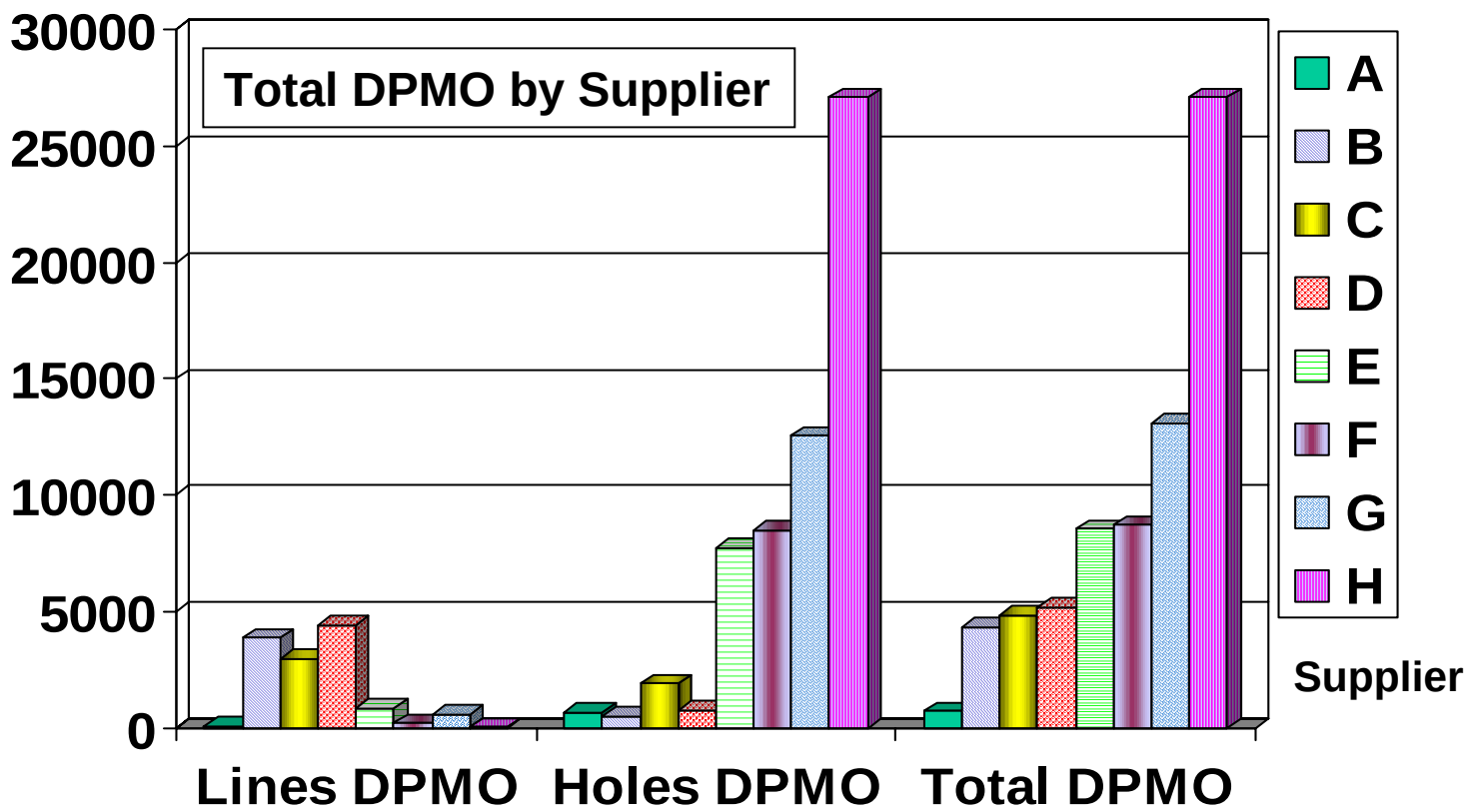
USING THE IPC-24-125 HB DATA

Supplier Capability Index
Impedance Capability (Cp)

	Impedance Capability (Cp) @ +/- 10%						
	.005" Surface Microstrip	.005" Embedded Microstrip	.005" Symmetric Stripline	.005" Offset Stripline	.005" Edge-coupled Differential Symmetric Stripline	.005" Edge-coupled Differential Offset Stripline	.005" Broadside-coupled Differential Stripline
Supplier 1	**0.77**	**1.28**	**1.15**	**1.20**	**1.09**	**1.15**	**0.86**
Supplier 2	**0.84**	**1.63**	**1.25**	**1.83**	**1.69**	**2.11**	**1.12**
Supplier 3	**0.46**	**1.55**	**1.33**	**1.44**	**1.24**	**1.15**	**1.31**
Supplier 4	**0.76**	**1.55**	**1.76**	**0.68**	**1.88**	**0.85**	**1.54**
Supplier 5	**0.79**	**1.39**	**1.61**	**2.04**	**1.60**	**1.80**	**0.86**
Supplier 6	**1.22**	**0.90**	**0.78**	**0.98**	**0.87**	**1.00**	**0.45**
Supplier 7	**0.59**	**1.07**	**0.92**	**0.74**	**0.97**	**0.83**	**0.68**
Supplier 8	**0.61**	**0.99**	**0.83**	**0.83**	**No data**		
	3 sigma	**4 - 5 sigma**	**6 sigma**				

PCB SUPPLIER CAPABILITY ANALYSES

USING THE IPC-24-125 HB DATA



PCB SUPPLIER CAPABILITY ANALYSES

IPC-36-250-HB PROJECT DESCRIPTION

- 36 LAYER 18.0” x 24.0” X .250” CIRCUIT
- LASER BLIND VIAS 1 AND 2 LAYERS DEEP (REVISIT)
- CONTROLLED DEPTH BACK-DRILLED VIAS
  (STUB DRILLING 2 LENGHTS: ~ .050” and ~ .180” DEEP)
- 14:1 UP TO 18.5:1 ASPECT RATIO VIAS
- BURIED VIAS (OPTIONAL BY SUPPLIER)
- HOLE TO INNER LAYER PAD REGISTRATION
- SOLDER MASK REGISTRATION
- CONTROLLED IMPEDANCE VARIATION
- NET RESISTANCE AFTER ASSEMBLY “PRECONDITIONING”
- HIGHLY ACCELERATED THERMAL STRESS TEST

PCB SUPPLIER CAPABILITY ANALYSES

FUTURE NEEDS

AUGMENT CURRENT TEST PANEL METHODOLOGY WITH:

- **SMALLER PANELS**
  - **SAVE $$ OR**
  - **CONCENTRATE ON FEWER DESIGN FEATURES**
- **SMALLER LOTS**
  - **SAVE $$**
  - **SAVE TIME**
- **MORE USER VARIABLES (FLEXIBILITY)**
  - **USERS' "DESIGN OF EXPERIMENTS"**
- **HIGHLY ACCELERATED THERMAL SHOCK (HATS) TESTING**

PCB SUPPLIER CAPABILITY ANALYSES

SUMMARY

- DESIGN DECISIONS INFORMED BY DATA; OPTIMIZED FOR
  - PRICE
    - SUPPLIER COST
  - YIELDS
    - INITIAL AND LONG TERM QUALITY
    - TIME TO VOLUME
- SUPPLYBASE DEPLOYMENT
  - SUPPLIER CAPABILITY MATCHED TO DESIGN COMPLEXITY
- TECHNOLOGY DEPLOYMENT
  - ROADMAPPING; GAP ANALYSIS; DEVELOPMENT PROJECTS

THANK YOU

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S01 Benchmarking and Process Capability

IPC Annual Meeting Technical Conference
October 2003, Minn, MN.