Challenges in Bare Die Mounting

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Abstract
Traditionally, the evolution of advanced IC assemblies has been due to defense and aerospace applications, where reliability, size and weight were at a premium, and cost was a secondary consideration. In the 1980's, high performance computing became the advanced packaging development stimulus. That world changed again in the late 1990's with the emergence of ubiquitous digital content, providing impetus to the consumer markets of digital cameras, cellular phones, portable computers, PDAs and other similar high volume applications; these have now become the "driver" for advanced assemblies of semiconductors. Assemblers of state of the art consumer products are developing sophisticated packaging and interconnect approaches that more and more rely on the use of die products for these types of applications. Die products are defined as bare die, bumped die or "wafer level packaged die" that change the overall "footprint" on the mounting substrate when the die size changes. This paper reviews several of the die products technologies, and outlines mounting challenges to their use.

Introduction
Bare die mounting on multi-device substrates has been in use in the microelectronics industry since the 1960s. The aerospace industry's hybrid modules and IBM's Solid Logic Technology were early implementations that were developed in the 1960's. The technologies progressed on a steady level until the mid 1990's when, with the advent of BGA packaging and chip scale packages, the microelectronics industry started a wholesale move to area array packaging. This paper outlines the challenges for both traditional wire-bond die attached to a printed wiring board (pwb), to the more recent applications of bumped die attached to a high performance substrate.

Die Product Technologies
The several technologies that are considered die products are bare die with aluminum wire bondable I/O and power pads, bumped die with interconnections structures on the I/O and power pads, and wafer level packaged die that have a relaxed pitch,, mechanical protection on the surface of the die, optional rerouting of I/O and power pads, and formed with interconnection structures on the I/O and power pads. These are termed die products because they are sold to customers as a product and are available through normal IC distribution channels.

Bare Die
The most readily available form of die products are termed bare die. These die are identical to the die that are used in the vast majority of single chip packages today as they are wire bonded to a lead frame or interconnecting substrate. The use of wire bonded die mounted directly to the pwb is termed chip-on-board, (COB). COB is the most mature and largest part of the bare die market. Chip on board technology is characterized by the following factors:

- Bare die mounted on interconnecting substrate or pwb
- Die are mechanically attached to the substrate using conductive or non-conductive epoxies
- Die are electrically connected to the substrate using wire bonding
- Die are encapsulated with a protective shell

Figure 1 shows a pwb with 4 chips mounted directly on the board.

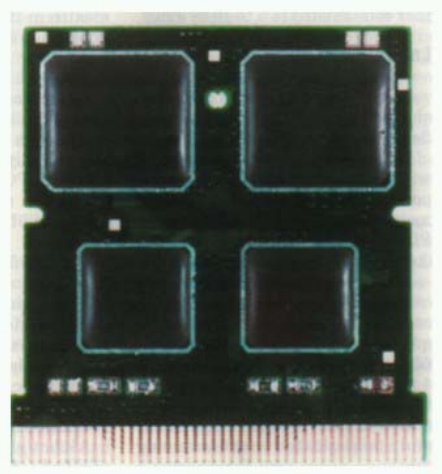

Figure 1 - Bare Die Mounted Directly on the Surface of Low Cost Laminate Substrates is the Highest Use of Bare Die in Products Presently

The COB assembly process consists of three basic steps; die attach, wire bond and encapsulation. Figure 2 shows a schematic cross-section of the COB assembly. Die attach provides mechanical adhesion of the chip to the intended substrate and requires an adhesive application followed by precision chip placement; then curing of the adhesive. Once firmly in place the wire bond process electrically connects the die bond pads to the associated wiring pattern on the substrate. The wire bond machine welds fine wires, typically of Al or Au, between each pad on the chip and the appropriate pad on the substrate. Wire bonding demands clean pads on both the chip and the substrate to ensure strong bonds as well as high production yields. Finally, encapsulation protects the die and bond wires from mechanical damage during handling and additional processing. In some cases, particularly for system in package applications, the encapsulation also provides the finished surface for component marking. Encapsulation employs either liquid dispensing or transfer molding depending on the specific application.

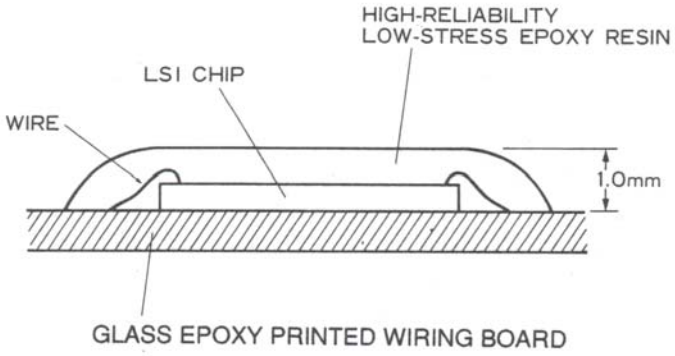

Figure 2 - Schematic Cross-section of a COB Mounted Die

Designing a COB assembly process sequence can be critical, particularly for applications where die products and surface mount (SMT) components are combined on a single substrate. In principle, the COB process may either precede or follow the SMT assembly process. Generally however, SMT processing first provides a simpler process flow particularly if the COB process employs a good cleaning process. A process step such as plasma cleaning to prepare the bonding surfaces is recommended. Process characteristics and considerations for COB assembly are detailed below and provide specific information for understanding, selecting and specifying the COB process.[1]

Cleaning

Wire bonds will exhibit low yield and poor reliability unless the surfaces are clean when bonding occurs. Until recently, there was little consideration given to a cleaning step specifically designed to improve the yield and reliability of wire bonds. The high-reliability hybrid industry has pioneered the use of molecular cleaning methods before bonding. Although some contaminants can become chemically bound to bond pads and thus require cleaning at the wafer level, most bondability problems are caused by organic contaminants, which may be effectively removed with plasma cleaning gases, such as Oxygen or Argon, as well as the simpler UV-ozone approach, applied

at the die packaging level. In one study[2] few angstroms thick film of carbon was found to impair bondability, whereas a cleaned gold film (<1 Å carbon) was reliably bonded at 150ºC, which is a low temperature to be used in thermosonic bonding. Figure 3 shows a typical yield curve for plasma vs. non-plasma cleaned surfaces. It portrays the situation with wire bond defects vs. energy level for cleaned and uncleaned surfaces.

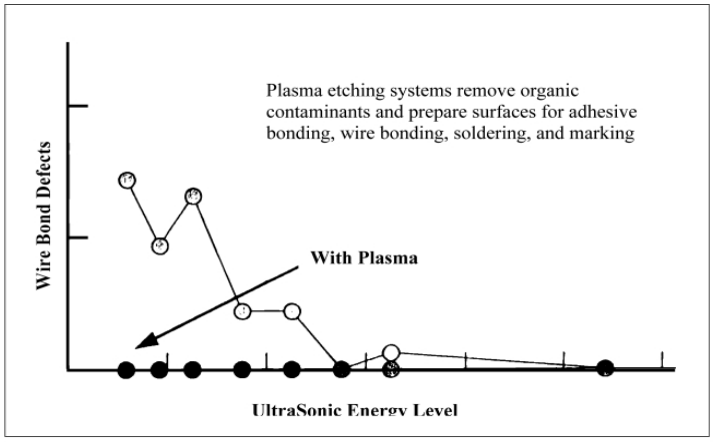

Figure 3 - Graph Depicts Number of Wire Bond Defects as a Function of Energy Level for both Plasma Cleaned and Uncleaned Surfaces. (Courtesy of Techlead Corporation)

Visual Inspection

The quality and yield of a COB process is dependant on good manufacturing practices, and visual inspection is critical to success. The interconnecting substrate, die attach, wire bonds, and encapsulation defects may all be detected by visual inspection, including those that would not be detected by other means, such as electrical testing.

Die Bonding

If the die are to be interconnected to the substrate via wire bonds, the die is first attached with the backside to the substrate by a suitable adhesive and the wire bonds are then made. Die bonding adhesive requirements include high adhesion, high thermal conductivity, high electrical conductivity and acceptable process temperature. The most common die attach material is a silver-based epoxy, but other materials are used, including silver-glass pastes and liquid solder, employed most often for high-power applications. Table 1 shows typical die attach materials and compares advantages and disadvantages of each.[3]

Table 1 - List of Die Bonding Materials and Summary of Advantages and Disadvantages of Each

Bonding Materials	Advantages	Disadvantages
Organic Adhesives	Low processing temperature	Poor thermal stability
Metal-filled epoxies	Stress relief, low cost	Low thermal conductivity
Glass adhesives	Good thermal stability	High processing temperatures
Soft solders (Pb-Sn, Pb-In)	Stress relief, low cost	Thermal fatigue, creep
Hard solders (Au-Sn, Au-Si, Au-Ge)	No thermal fatigue, High strength	No stress relief, High cost

Dispensing, stencil printing or pin transfer of adhesive to the substrate may be used depending on die size. Dispensing is the most popular transfer method, except for film type adhesive. Dispense patterns depend on die size and shape but all must ensure a void free bond line.

Die Placement

Die placement into the dispensed adhesive demands accuracy as well as proper orientation and planarity control. Over pressure to set the die into the adhesive will ensure good adhesion and establishes the bond line thickness. Orientation and accuracy of placement directly impact the bond pad to substrate wire length and the "keep out" or die spacing requirements. Post placement operations such as underfill must be taken into consideration during the placement operation.

In general terms, a die placement cycle consists of the following steps:

- Pattern recognition of the substrate using global or local fiducials (or the circuit itself)
- Picking of the die (either single or gang picking)
- Imaging and theta correction
- Placement of the die

Whatever die placement techniques are used, die presentation and substrate handling issues are shared by all. Die may be presented for placement in various ways, such as in wafers, waffle packs, and tape and reel. Choosing the optimum die-feeding scheme depends on various factors, such as upstream processes, wafer yields, die sizes, and die sorting requirements.[4]

Wire Bonding

Wire bonding has been practiced in the microelectronics industry since the 1960s. The vast majority of IC devices in the industry are wire bonded onto lead frames or substrates today. The exceptions are those devices that have interconnection structures, such as bumps, on the "bond pads" to be mounted in a flip chip manner.

Ultrasonic wedge bonding was introduced to the industry in the 1960s and became dominant until gold ball thermocompression bonding became prevalent. Ultrasonic wedge bonding is done at room temperature. It is used primarily to bond Al wire to either Au or Al bond pads. The ultrasonic weld is formed by the application of ultrasonic energy while applying a clamping force.

Today, however, the majority of interconnections made to ICs are made with Au thermosonic ball bonding. This method uses a combination of ultrasonic and thermocompression welding that optimized the best qualities of each. Thermosonic welding requires lower temperatures than thermocompression welding, making this technique suitable for bonding plastics, laminates as well as sensitive die.[5]

- Gold Ball Bond Parameters
  - Advantages: high throughput, high strength, omni-directional, fine pitch
  - Disadvantages: elevated temperature, increased material cost, intermetallic potential
  - Process Considerations: temperature, power, force, time, wire diameter, wire length, metallurgy, pitch, bonding surface conditions, bonding area
- Aluminum Wedge Bond Parameters
  - Advantages: room temperature processing, lower material cost (wire), fine pitch
  - Disadvantages: Strength, throughput, not optimum for non-hermetic applications
  - Process Considerations: power, force, time, wire diameter, wire length, metallurgy, pitch, bond angle, forward/reverse bonding, bonding surface conditions, bonding area

Encapsulation

Either liquid encapsulation or transfer molding is generally required to provide physical protection for the die. Larger modules and die mounted to large, mixed technology substrates usually require liquid encapsulation.

Material requirements for encapsulation include low moisture permeability, excellent mobile ion barrier, good Ultraviolet-Visible and alpha particle protection, excellent mechanical, electrical and physical propertied. The encapsulant must have a low dielectric constant to reduce device propagation delay, and excellent thermal conductivity.[6] It is important to choose a product that is adapted to the application and the conditions under which it is to be subjected.

Flip Chip Mounting

Flip Chip is a term used to describe the multiplicity of mounting technologies that orient the face of the die toward the interconnecting substrate. Although flip chip technology was inaugurated by IBM and Delco in the 1960's, it is now poised to become the interconnection method of choice for many die devices. The parasitic electrical elements introduced by the bumps presents the best interface to the board, the ability to place power and ground connections throughout the face of the die, the fact that this is, in general, a "gang" bonding technique, are all playing a role in the conversion of wirebond devices to flip chip.

In addition to these advantages, one of the most important is the fact that the bonding pads are not required to be placed at the periphery of the die – and in fact, the preferred arrangement is an array configuration over the face of the die. Array I/O also improves power delivery, high speed performance and provides relaxed pitch for ease of die product assembly. Some of the technologies finding favor now are solder ball flip chip and adhesive flip chip. Figure 4 shows the impact of using area array pad configuration vs. peripheral configuration.

As IC feature sizes continue to shrink according to Moore's Law, area array pad configuration can keep the device size from becoming I/O limited.

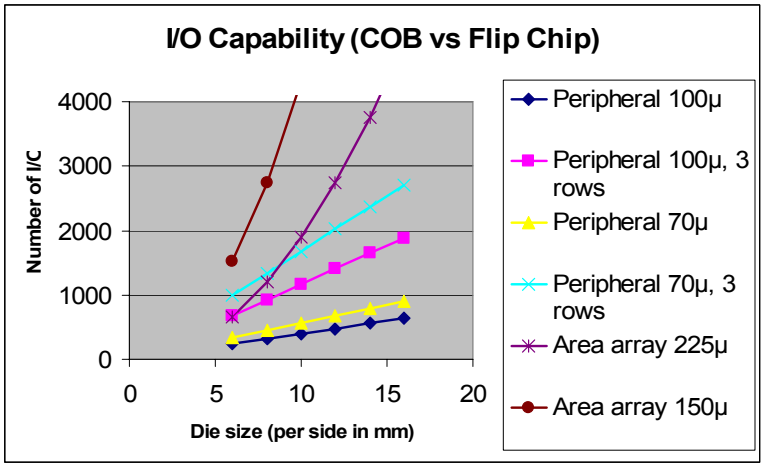

Figure 4 - I/O Capability of Flip Chip at Today's Pitches vs. Peripheral Location of Bond Pads Illustrates the Much Higher Capability of Flip Chip to Accommodate High Pin Count Devices

Solder Flip Chip

Solder bumped flip chip has been in use at IBM since the 1960s. The IBM solder bumping process, termed C4, utilizes a high melting point solder which, if used on a low tg board such as FR-4, cannot be reflowed. However, the bumps can be utilized as standoffs, and joined to a thin layer of eutectic solder that is applied to the surface of the pads on the interconnecting substrate. The other option is to form eutectic bumps to the die and reflow directly onto the prepared pads of the interconnecting substrate. This method of flip chip mounting is directly compatible with surface mount processes. Figure 5 shows the process flow for a eutectic solder flip chip line.

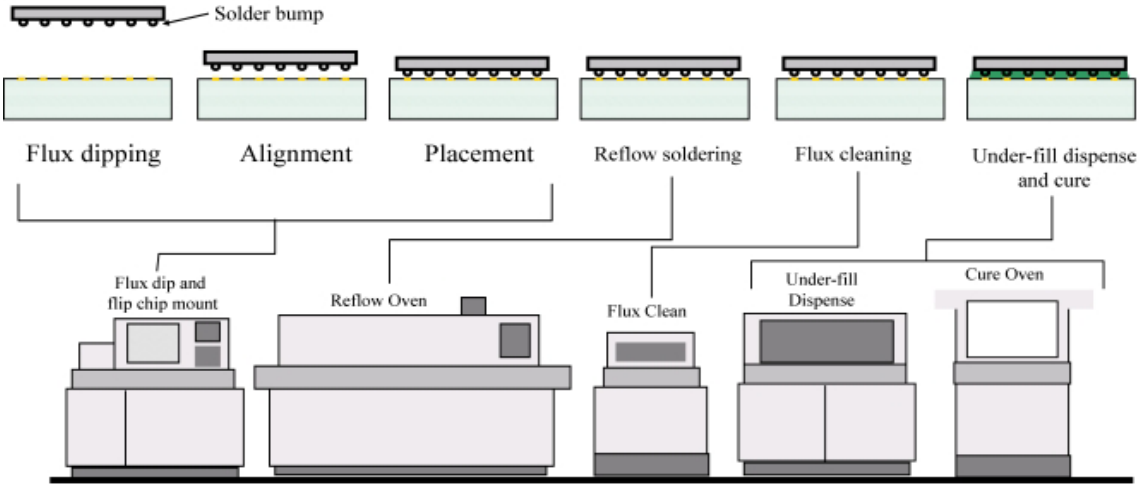

Figure 5 - Process Flow for Mounting Solder Flip Chip Devices (Courtesy of National Semiconductor)

Underfill Encapsulation

One of the additional steps used for flip chip mounting is the need for underfill. Its main purpose is to reduce the effect of the CTE mismatch between the silicon die and the organic substrate. Recently underfill is also seen as being a requirement in mobile electronics systems to provide a "shock" mounting for the die, especially in a 3D stack. Once the underfill is cured, the chip, underfill, and substrate deform together as a unit keeping the relative deformation between the chip and the substrate very small, so the shear strain in the solder joint is small.[7] The most desired features of underfill are:

- Low Viscosity (fast flow)
- Low curing temperature/fast curing time, which can reduce cost and be less harmful to other components
- Low TCE, which can reduce thermal expansion mismatch between the chip, solder bumps and the substrate.
- High modulus, which leads to good mechanical properties
- High glass transition temperature, which enables endurance of higher temperature environments
- Low moisture absorption, which can extend shelf life
- Good adhesion, which can improve product life time

A recent advance in underfill encapsulation is the so-called "no flow" underfill. In this process, the underfill is applied to the substrate prior to the chips being placed. A typical process is a follows:

- A controlled volume of no flow underfill material is dispensed over the bond pads on the substrate
- Solder paste is printed onto the board for SMT component assembly
- SMT components are placed
- Bare chips are then aligned using a vision system to orient the chips, relative to bond site fiducials on the substrate.
- The chips are placed on the substrate, compressing the no flow liquid underfill to form a compression bond to the substrate
- The solder interconnects are reflowed simultaneously while fluxing and polymerization of the no flow underfill takes place

No-flow underfills can have a significant advantage over standard underfill processing by eliminating the lengthy capillary flow times needed with large devices. In addition, process speed is increased by having the no flow material completely cured during the reflow step, thus eliminating a timely post bake batch process.[8]

Adhesive flip chip

Another form of flip chip mounting that is gaining favor in the portables world today is adhesive flip chip. There are several forms of this technology, depending on the requirements. A form of flip chip using non-conductive adhesive film to directly bond a stud-bumped IC to a fine line circuit board has been reported.[9] Because the adhesive film does not contain conductive particles, as in the case of conductive adhesives, it can be used for smaller pad pitches. The film also acts as a encapsulant, or underfill material, for thermal-mechanical management.

The other form of adhesive flip chip mounting utilizes an anisotropic conductive material, in either a film (ACF) or adhesive (ACA) form, as the electrical and mechanical joining agent. Anisotropic conductive film looks like paper and consists of thermosetting adhesive, conductive particles, and release film.[10] Figure 6 is a schematic representation of anisotropic conductive film flip chip technology. Anisotropic conductive adhesive looks like paste and consists of thermosetting adhesive and conductive particles.

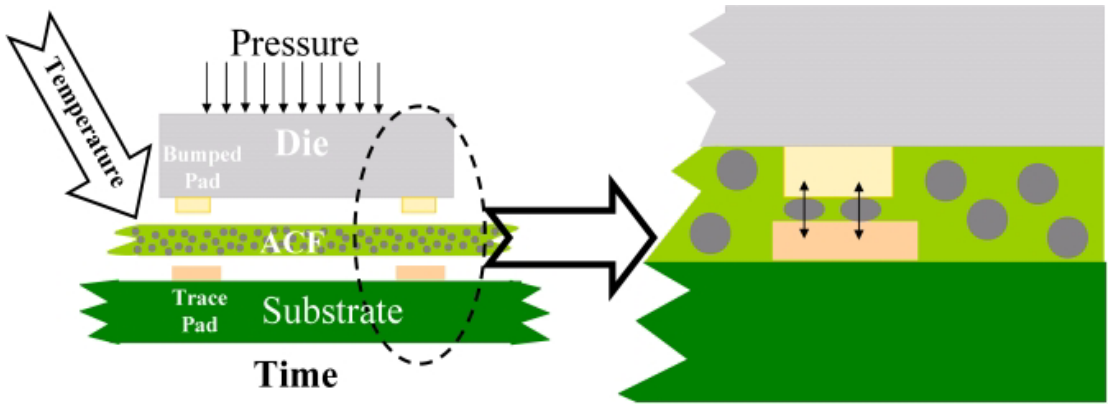

Figure 6 - Cross-section of Adhesive Flip Chip

Several advantages to adhesive flip chip mounting technologies are noted. In general, the pad pitch of the die is finer than possible with solder flip chip. The cleaning step is not as rigorous as with solder based systems, it eliminates process steps such as coating the interconnect pads with solder and eliminates the use of lead. The bumping process may be simplified by the use of stud bumping, which utilized the same processes and equipment to form a bump as to wire bond to a IC pad. Thermocompression and ultrasonic energy are used to form a gold ball bond on the IC pad; the wire is cut at the top of the ball and leveled, creating a gold bump suitable for ACF bonding to a substrate.[11]

Wafer Level Packaging

The drive to flip chip assembly is being supported by wafer level packaging approaches. Wafer-level packaging (WLP) is an advanced packaging technology in which the die terminals are manufactured and tested on the wafer, then singulated by dicing for assembly in a surface-mount line. The die terminals are characterized by wider pitch and larger ball structures than associated flip chip structures. Wider pitches are advantageous for integrating these technologies into a standard surface mount line. Larger diameter balls support the mechanical requirement to reduce TCE mismatch strain between the IC and the interconnecting substrate.[12] Greater standoff height reduces the strain

within the interconnecting structure – e.g., individual solder balls for solder based devices. Table 2 summarizes the key parameters that characterize wafer level packaged ICs.

Table 2 - Comparison of Wafer Level Package and Flip Chip Parameters

	Wafer level package	Flip Chip
Pitch	500 micron min	125 micron
Pin Count	Limited	Unlimited
Availability	Limited	Broad Portfolio
Testability	Fully Tested	Fully Tested
Bondability	SMT Compatible	SMT-like
Thickness	20 – 24 mils	11 mils

Wafer level packaging is a continuation of the trend to achieve the functionality and density of bare die assembly which began in the late 1990s with a series of devices known as Chip Scale Packages (CSP). Several CSP technologies have been developed[13] by the packaging community which are very close to the dimensions of the bare silicon die. CSP technology can ease assembly and test requirements due to larger ball pitch and compatibility with traditional surface mount assembly equipment. Over the past several years, CSP pad pitches have been reducing from 1.0 to .8 to .75mm. Area array pad pitches above .5mm are considered able to be incorporated into the standard surface mount technology manufacturing flow.[14] The wafer level packaging technologies are aimed to take advantage of the standard SMT processes while presenting the absolute minimum footprint to the interconnecting substrate. Of course, economies of batch processing that have driven the Moore's law improvements are at work for the first time in the packaging of the device.

One strong factor in the pursuit of CSP and wafer level packaging technologies is the hope to avoid underfill. Assemblers may underfill devices because of concerns over the CTE mismatch between the silicon and the interconnecting substrate or to provide "shock" mounting of die in portable electronics that may be subjected to drops. The small die typical of the wl-csp process are less exposed to the risk of damage due to these mechanical shear forces, and the need to underfill is reduced.

Conclusion

Driven by the remarkable economies presented by IC manufacturing, the explosion of digital content is fueling a revolution in the expectations of consumers today. Not only are higher bandwidth, greater resolution, and improved quality in digital photography, communications, computation, etc., expected to be developed on a regular basis, but the price must be lower, and reliability higher. Manufacturers of leading edge consumer electronics devices are adopting die products for space and weight savings, product differentiation, functional integration, cost and time to market advantage.

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