What's Wrong With My Surface Finish?
An Evaluation of the Limitations of Common Surface Finishes

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Abstract
This paper will highlight the shortcomings of each of the commonly used surface finishes available on the market today. The goal is to spark the industry interest, that it may double its efforts in resolving the technical issues surrounding the existing processes and to develop emerging products.

This discussion will be from the OEM's point of view, as well as concerns from the Fab and Assembly side of the equation. Finally, the paper will also discuss the industry needs going forward; especially regarding the tight pitch tendencies and higher speed requirements of future systems.

Introduction
Currently, there are over a dozen surface finishes on the market today. All are useful for some applications, but none really fit the category of "universal surface finish." We aim to highlight each of the common surface finishes with regards to advantages and shortcomings, and to itemize what is paramount to the PCB design community when choosing the correct finish for the bare PCBs.

Discussion
The surface finishes profiled herein are:
- HASL
- OSP
- ENIG
- Immersion Silver
- Immersion Tin
- Electrolytic Nickel-Gold
- Electroless Nickel / Palladium / Immersion Gold
- Selective finishes
- Reflowed Tin-Lead

There are certainly more products on the market today that are not contained in the above listing. However, they hold a relatively smaller market share, so will not be part of this preparation. If any of these final finishes are truly universal, according to the needs of the OEMs, then increased marketing and technical forums need to be implemented to spread the word.

As you will see, each finish has distinct limitations which prohibits its use in other, expanded applications. The PCB-PCBA-OEM industry really needs two things from the material vendors:
- A universal surface finish that satisfies all of the requirements of the OEM.
- A surface finish that can be used with high speed applications; that is, signal speeds in excess of 7 Gb/sec.

First, we can divide the OEM requirements for a surface finish into two groupings:

Internal	External
▪ signal integrity	▪ cost, cost, cost
▪ high speed signals	▪ shelf life
▪ EMI shielding	▪ can be re-applied
▪ RF capable	▪ wetting/solderability
▪ high joint strength	▪ good for 5+ yr. EOL
▪ contact resistance	

Secondly, the surface coating must not slow the signal speed of boards that run in excess of the 7 Gb/sec. Immersion silver is the only surface finish that satisfies this requirement, without compromising any of the other

needed characteristics for a final finish. However, tarnish after assembly is still a primary issue and it prevents silver from being utilized as universally as once hoped. We have tested tarnished silver PCBs extensively for loss of functionality and the deposit remains useable. EMI shielding, EMI leakage, contact resistance, signal integrity, solderability, and joint strength have all been profiled in these studies. Despite all of the data, cosmetic issues remain the major cause for rejects for the silver deposit. We are hoping that the new generation of tarnish-resistant silvers being tested will eliminate cosmetic tarnish on immersion silver plated PCBs.

In our discussions surrounding the benefits and limitations of the common surface finishes, it is important to note that the benefits/drawbacks of these deposits may vary according to the PCB & CM processing, and the OEM applications, as shown in Table 1. A good example of this is the use of immersion silver. For most OEMs, tarnish is no issue because there is no exposed silver on the PCB after assembly. However, some OEMs use exposed edge rails and/or uncoated internal pads for NPTHs (non plated thru-holes), and these can exhibit tarnish after assembly or burn-in.

Table 1 - Advantages and Disadvantages for Common Surface Finishes

Surface Finish	Thickness	Advantages	Disadvantages
HASL	50 – 1500 µin	Nothing solders like solder. Easily applied. Lots of industry experience. Easily reworked. Good bond strength. Withstands multiple thermal cycles.	Huge co-planarity differences resulting in off-contact printing & assembly defects. Contains lead. Not suited for high aspect ratios. Not suited for < 20 mil pitch. PWB dimensional stability issues. Bridging problems on fine pitch assemblies. Inconsistent coating thicknesses (on varying pad sizes).
OSP (Benzimidazoles)	0.2-0.6 µm	Flat, coplanar pads. Reworkable (at PWB fabricator). Doesn't affect final hole size. Short, easy process. Cu-Sn IMC formed has been reported to be stronger and more robust than Cu-Sn from HASL & Ni-Sn from Ni-Au.	Assembly line changes may be required; not a drop-in. Question remains over reliability of exposed Copper after assembly. Limited thermal cycles. Cannot be reworked by the assembler. Sensitive to some solvents used for misprint cleaning. Limited shelf life. Test pins cut coating, leaving exposed copper.
ENIG	125-250 µin Ni 2-8 µin Au	Planar surface. Consistent thicknesses. Withstands multiple thermal cycles. Long shelf life. Solders easily. Good for fine pitch product.	Not wire bondable. Expensive. Should not be used on ≤ 1.0 mm pitch; black pad issues. Waste treatment of nickel. Cannot be reworked at PWB fabricator. Nickel is a suspected carcinogen. Not optimal for higher speed signals.
Surface Finish	**Thickness**	**Advantages**	**Disadvantages**
I-Ag	≥ 5 µin	Good for fine pitch product. Planar surface. No black pad concerns. Short, easy process cycle. Eliminates nickel. Doesn't affect final hole size. Long shelf life. Can be re-worked / re-applied by the fabricator. Ok for multiple Insertions. Inexpensive. Drop-in process for the assembler. Good for ultra-high speed signals.	High friction coefficient; not be suited for compliant pin insertion (Ni-Au pins). Some systems cannot throw into blind vias with aspect ratios > 1:1. Tarnishing must be controlled.
I-Sn	25-60 µin	Good for fine pitch product. Planar surface.	Handling concerns. Panels need to be routed and electrically tested

		Eliminates nickel. Can substitute for reflowed solder in selective strip. Inexpensive.	before coating. Contains thiourea. Limited rework cycles at assembler. Horizontal process needs nitrogen blanket.
Electrolytic [hard] Ni-Au	50-200 µin Ni 5-50 µin Au	Plated Ni-Au can be used as etch resist. Available for "mixed technology" products. Au wire bondable.	Exposed Cu sidewalls. Ni slivers after SES. Nickel throwing power issues in small vias. Costly process. Excess gold easily plated on board edges causing poisoning of solder joints.
E-Ni/Pd/I-Au	120-240 µin Ni 10-30 µin Pd 3-8 µin Au	Pd keeps Ni from passivating in presence of "porous" gold coating. Al wire bondable. Planar surface. Good for fine pitch product.	Additional processing step for PCB Mfg. adds cost. Dip tank process. Evidence that Pd poisons the solder paste after reflow. Waste treatment.
SSS (Selective Solder Strip)	See applicable surface finishes	Hot bar reflow for TAB devices. Viable alternative to HASL on thick product.	Multiple resist & photo cycles. Difficulty in controlling plated Sn/Pb thickness. Overlap (butt) line difficult to control. Expensive.
Reflowed Tin-Lead	50 – 1500 µin	Fast process. Inexpensive. Time tested. Good for solderability.	Solder slumping may cause hole size reduction-violation. Reflowing causes uneven deposit thicknesses in the hole. Heavy panels may require automated handling. Not a planar deposit.

Despite the many advantages and drawbacks of each surface finish, there are one or two major defects that preclude its universal or widespread use:

HASL

- Bridging of tight pitch outerlayer traces, and hole plugging on small thru-vias.
- The lack of co-planarity is not the issue it was once thought. The reason is that the newer, horizontal processors have minimized this effect, and the assembler's specification usually allows for a 3 mil standoff, so that issue is unlikely.

OSP

- Lack of robustness of the deposit makes it difficult to re-work, and clean.
- The ET test pins cut through the coating and expose potential corrosion sites.
- To eliminate the issue of the test pins cutting through the coating, many PCB fab houses choose to apply OSP after ET (electrical test). This exposes the bd to defects (such as copper voids in the hole due to over aggressive OSP pre-clean microetch.) that will not be identified until after assembly. At this point the value of the scrap has now risen exponentially.

ENIG

- The rise of black pad defects which cause massive solderability failures.
- Not suited for high speed application >7 Gb/sec: there is evidence that the nickel in the deposit slows down the signal speed.

Immersion Silver

- Tarnish causes many cosmetic failures for boards with exposed silver after assembly.
- Remaining UL limitations on its usage.

Immersion Tin

- Lingering questions surrounding the growth of whiskers and dendrites over time, especially at room temperature.
- Some vendors' processes need a more vigorous deposit: some do not stand up to multiple thermal cycles.

Electrolytic Ni-Au

- Difficult to get the minimum 70 µin of nickel plated in the small thru-vias.
- Nickel slivers cause shorts across traces.

- Excess gold in HCDA (high current density areas) causes gold embrittlement of the solder fillets.

Electroless Nickel-Palladium-Immersion Gold
- -For most OEMs, the cost is excessive.

Selective Solder Strip
- The expense for this process is too great as well. Mostly, it is used because there is no one surface finish that can satisfy all of the requirements on the PCB. At best, it is an expensive compromise.

Reflowed Tin-Lead
- Solder slumping causes hole size violations on thick backpanels.

Surface Finish Selection

Table 2 and Table 3 are examples of charts that are used by some OEMs to identify the proper surface finish to use on PCBs, according to the technology on the boards. As you can see, there is no single finish that satisfies all of the applications for assembly, even if we disregard the [odd] need for wire bonding. Again, silver is the closest to filling the role of universal surface finish, but the tarnish defects preclude that from being the case.

Table 2 - Example of OEM Selection of Surface Finish Based on Board Technology

Surface Finish	Thru-holes	Press fit	SMT	Fine Pitch BGA	EMI Shields	Card Guides	Edge Connectors	Flip Chips	Gold wire bond	Aluminum wire bond
Selective Solder	ok	ok	ok	ok	ok	ok	ok	ok	NO	NO
ENIG	ok	ok	ok	*NO	ok	ok	ok	ok	NO	NO
HASL	ok	ok	ok	NO	ok	ok	ok	NO	NO	NO
Immersion Tin	ok	ok	ok	ok	ok	ok	ok	ok	NO	NO
Immersion Silver	ok	ok	ok	ok	***NO	ok	ok	ok	NO	NO
OSP	ok	** ok	ok	ok	NO	NO	ok	ok	NO	ok
Electrolytic Ni-Au	Not recommended at **XXXXX**								ok	ok
Reflow Tin/Lead	ok	ok	NO	NO	ok	NO	ok	NO	NO	NO

*Not recommended for 1.0 mm pitch or less

**Not the best or more robust choice

***EMI shielding ok, but tarnish forms when left unsoldered/exposed

Table 3 - Common Attributes of Surface Finishes

	Silver	ENIG	HASL	OSP
co-planar deposit	**yes**	**yes**	**no**	**yes**
non-galvanic	**yes**	**no**	**yes**	**yes**
shelf life	**1 yr**	**1 yr**	**9 mos**	**6-9 mos**
Multiple rework cycles	**yes**	**limited**	**limited**	**no**
higher cost savings	**yes**	**no**	**no**	**yes**
CM line changes needed	**no**	**yes**	**yes**	**yes**
doesn't reduce hole sizes	**yes**	**yes**	**no**	**yes**
ok for ≤ 1.0 mm BGA pitch	**yes**	**no**	**no**	**yes**

Keep in mind that the few items that seem to pass the "universal surface finish" criteria have major cost concerns compared to the majority of the coatings listed.

Conclusion

Although the information contained herein breaks no new ground, we strongly believe that it needs periodic review to keep us focused on the need for a universal surface finish, and improvement of existing processes, which should ultimately lead to a paring down of the number of surface finishes employed by the industry.

This would be welcomed by the PCB fab community, who could effect significant cost savings through a reduction in the amount of employees needed in the final finish dept, reduced chemistry and materials acquisition, floor space, and utilities consumed.

The Contract Manufacturing Assemblers would also see substantial benefits by reducing the number of different fluxes needed for all of the surface finishes processed, there would also be "set up" savings, and a reduction in the number of process lines needed (in some cases).
The OEM community would benefit from the reduced number of surface finishes by not having to track which finish is applied to which P/N; and in some cases the same P/N will have differing finishes on multiple lots or date codes. Logistically, much time and money is spent to organize, disposition, and classify when each finish should be used. Funds can also be preserved by eliminating the expense of testing, studying, and qualifying each surface finish on the market.

Finally, our customers would benefit from having uniformity in the PCB coatings which make swaps, replacements, and even reliability matches for the boards in their systems easier to track and predict.