Designing Ceramic Thick-Film Capacitors for Embedding in Printed Circuit Boards

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Abstract
This paper presents an emerging technology for embedding discrete ceramic thick-film capacitors directly into printed circuit boards. Their use frees up surface real estate allowing for smaller boards and/or for more silicon on the board. They also lower inductance, impedance and radiated emissions. Previously, the technology has been limited due to lack of component values, performance and availability of commercial materials. These issues, however, are being eliminated and CTF embedded passives are emerging as a feasible technology. The CTF capacitor materials are robust, and discrete capacitors can be designed to a wide range of values and physical shapes. Materials, processes and design guidelines and manufacturing tolerances are discussed. Drivers are performance, miniaturization, and cost.

Introduction
Ceramic thick-film materials and processes for electronic applications have been around since the mid 1940s where they found applications as simple circuits on alumina. By the mid 1980s the ceramic hybrid industry grew due to demands in automotive, medical, military and aerospace, and consumer applications. Since then ceramic thick-film materials have had over 20 years of use in harsh environments and critical high reliability applications. They are also used in the manufacture of chip capacitors and resistors. Simply stated, they are the sequential printing and firing of conductors, resistors and dielectrics on suitable substrates.

"Suitable substrates" are the key words here. In addition to the right electrical and mechanical properties, the substrate must also be capable of withstanding the ceramic firing process, which is at or above 850^0 C. Hence, ceramic substrates are preferred for ceramic thick-film applications.

Paralleling the growth and enhancement of the ceramic hybrid technology since the 80s, the organic printed circuit board (PCB) technology has also enhanced its materials and processes. PCBs today have become a reliable, high density, stable, and robust product.

Capacitor Materials and Properties
Ceramic thick-film capacitor materials were recently developed by Dupont Microcircuit Materials, partially under a NIST funded consortium known as the AEPT (Advanced Embedded Passive Technology). The materials and their properties have been discussed at length in the last several years (see References 1, 2, 3 and 4).

The capacitors are based on a barium titanate filled ceramic dielectric with a Dk of 1000. The thickness of the material is held constant and the area of the

capacitor is varied such that capacitance values from 60 pF to 100 nF (Reference 5) can be obtained. A summary of the properties is given in Table 1.

Table 1 - Ceramic Capacitor Technical Data (ref 5)

PROPERTY	UNITS	TYPICAL VALUE
Dielectric thickness	microns	16-20 (1)
Capacitance	NF/cm^2	Aprox. 92 (2)
Dielectric constant	--	1800 – 2000 at 100 kHz (3)
Loss tangent	--	0.02 – 0.025 at 100 kHz (2)
Dielectric strength	V/25µ	>50 (2)
Temperature coefficient of capacitance	%	XR7 type behavior +/- 15% (-55^0C to + 125^0C) (1)
Bias test: 85%RH/85^0C/5V/1000hr	Pass/Fail	Pass (1)
Insulation resistance	Ohms	10*e11 (1)
Temperature coefficient of expansion	Ppm/^{0}C	10 (4)

(1)Dupont lab test
(2)ASTM D -150
(3)ASTM D - 149
(4)Calculation

Manufacturing Processes affect Capacitor Design Processes

The manufacturing process for these materials is shown in Figure 1 and involves screen printing the ceramic paste on preconditioned copper foil, firing in nitrogen at about 900^0C, and bonding the foil (printed side down) into a laminate structure used to fabricate innerlayers for a multilayer board. This process has been described in a number of articles (see References 6, 7, 8 and 9).

Many new materials have been introduced to the PCB industry over the years and have been readily integrated into the manufacturing processes with virtually little or no impact on the design process, other than perhaps changing a note here and there. Going from screened epoxy soldermask to LPI, low Tg

FR-4 to 170 Tg FR-4, ED foil to HTE foil, reflowed tin-lead to HASL and ENIG doesn't cause any additional effort on the part of the PCB designer. With the advent of the embedded passive materials and processes, this simple approach is changing. The designer must understand the process implications and must treat the design, lay-out and drawings accordingly.

Since the designer has to design the embedded capacitors rather than pick them from a supplier's catalogue or library of standard parts, more work is required. To design the capacitors may become a specialty. It would have been an impossible task, if at the introduction of SMT resistors and capacitors, for the designer to design (for manufacturing) every SMT resistor or capacitor to be placed on a board. To do that, the designer would have to have developed a level of understanding of an entirely new family of materials and processes. Fortunately, the part suppliers developed and provided the information on properties, dimensions, foot print requirements and part libraries. CAD providers then (meaning a few years later) incorporated this information into the CAD systems including libraries, placement and routing.

The situation is similar today, leaving us with a lot of manual design work to do until CAD tools are available.

The intent here is neither to scare the designer away or to try to cram a lifetime of manufacturing experience into a 45 minute read. The intent is to provide enough information to motivate the designer to ask the right questions and prevent designing into the proverbial corner.

The Manufacturing Process

Figure 1 shows the basic process flow for incorporating embedded ceramic thick-film resistors and capacitors into the organic PWB structure. It is important for the designer to understand that we are merging two different but related manufacturing technologies. They are different in that the ceramic thick-film is an inorganic process using temperatures of 850^0C to 900^0C, and the PWB is an organic process with temperatures rarely exceeding 200^0C. They are similar in that they both use multiple image transfers and the image resolution, registration and repeatability is critical. The unique feature of the process is the printing of the ceramic materials on copper foil and

subsequent firing at 900^{0}C in nitrogen. This printed and fired copper detail is then laminated into a copper clad core structure and processed like a layer in a printed circuit board. References 6, 7, 8 and 9 give a graphic overview of this process flow.

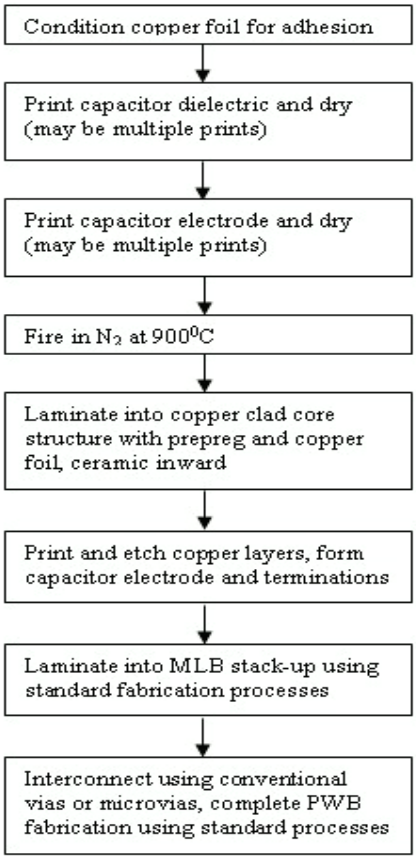

Figure 1 - Basic Ceramic Thick-film Capacitor Process Flow

The following discussion will compare the image tolerances in the PWB process to similar image tolerances with the ceramic process. It is very important to understand the affect of these tolerances in the merging of these two processes, as they establish and limit the design guidelines for size, positioning and termination of the ceramic embedded passives.

Printed Circuit Board Image Process Tolerances

In the PCB manufacturing process, there are 9 primary operations that have dimensional tolerances associated with them, which are listed in Table 2.

Table 2 - Primary Operations in the PCB Manufacturing Process

Well established processes	Mfg. tol. (+/- µm)
CAD inputs and conversion	Virtually perfect
Laser plotter accuracy	6
Mylar film stability	25
Inner layer side-to-side	10
Outer layer photo-tool punching	13
Post etch laminate shrinkage	75
Post etch tooling hole punching	13
Lamination pinning error	13
Laminate instability during press cure	63

Without going into the details of each one of these steps, the sum of the nominal tolerances is over +/-200µ. The largest contributor is post etch laminate shrinkage which alone can be up to +/-75µ. The tolerance is affected by inherent characteristics of the copper clad laminate materials. These are induced by the materials and laminate manufacturing process, including the type of reinforcement, type of resin, copper weight and curing conditions. For some constructions shrinkages are as much as 1mm across a 60cm panel. Others may be a little as 50µ across the same panel. To complicate matters, some constructions actually grow rather than shrink. At this point the reader might wonder, how it is possible to successfully manufacture printed circuit boards, with such extreme tolerances. Without exception, all PCB manufacturers scale artwork based on the predicted shrinkage/growth of the laminate material after etch and lamination. Scaling means to transfer a larger/smaller image to the copper clad laminate such that after etch, it will shrink/grow to size. Board manufacturers would benefit enormously if their suppliers made "sanforized" laminates. However, on the positive side, once the laminate material is characterized, its shrinkage/growth behavior is reasonably predictable. The reality is that tolerances do not all go in one direction, so statistically, any point of our image (after scaling) will fall within +/-75µ of where we want it. This is consistent with IPC 2221 Complexity Level C, High Design Complexity – Reduced. Level B, Moderate Design Complexity – Standard, is +/-100µ.

Ceramic Thick-film Image Process

In the ceramic thick-film process, there are several operations that have dimensional tolerances associated with them, which are listed in Table 3.

Table 3 - Primary Operations in the Ceramic Thick-film Process

Not as well established	Mfg. Tol. (+/- µm)
CAD inputs and conversion	6
Laser plotter accuracy	25
Mylar film stability	75
Screen preparation	25
Screen print dimensional variation (foil 1 to foil n)	25
1st value print to 2nd and subsequent value prints	25
Foil stability during firing	50
Foil stability during lamination	75

The sum of these tolerances is over +/-225µ. They start with laser plotter accuracy, mylar film stability, and screen preparation +/-56µ, followed by screen printing. With optical alignment precision screening equipment it is possible to print images within +/-50µ. When multiple images are required, add an additional +/-50µ. The drying and co-firing process adds an additional +/-50µ. Laminating the foil into the PWB core structure contributes an additional +/-75µ.

Like the PCB image tolerances, the ceramic position tolerances do not all go in one direction, so statistically, any point of our image will probably fall within +/-100µ of where we want it. Please note the emphasis on probably, because, to date, manufacturing data is limited, whereas with the standard PCB process there are many years of history.

Merging the Two Image Processes

The next step is to register the copper termination and circuit pattern to this ceramic dielectric and electrode pattern. The core detail becomes the baseline to which scaling all of the other PCB layers will be referenced. Scaling artwork is not an unfamiliar task for the PCB manufacturer. Using the technique to match the copper layers to the resistor core detail will not be difficult. The challenge is establishing a predictable positional tolerance for the ceramic resistor layer. This is the tolerance that governs the ceramic embedded passive device design guidelines for size, positioning and termination.

The board manufacturers' ability to register the copper image to the ceramic image using x-ray and optical registration tools is +/-175µ. This means that to be sure that the copper termination pattern aligns to the ceramic pattern, the copper features must be 350µ larger than the ceramic feature. Figure 2 shows the tolerance zones for the two image processes. If the tolerances go to the extreme and the termination pad is not sufficiently large to cover the ceramic feature, then an open could occur.

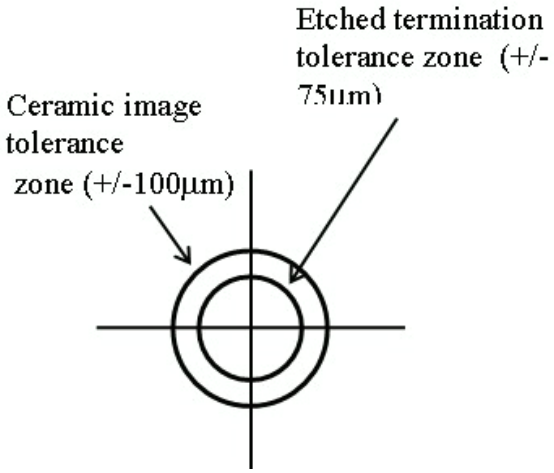

Figure 2 - Tolerance Zones for Two Image Processes

The essence of everything in this paper, to this point, is that manufacturing tolerances affect design. Further, merging the PCB processes with the CTF processes results in a net error of +/-175µ. This must be taken up in the size and positioning of the PCB and CTF features. Studies are in progress that will improve this tolerance. By the end of 2003, the goal is to get down to +/-125µ. Ultimately it is believed that +/-75µ is achievable. For simplicity in the future discussions the +/-125µ tolerance will be used.

Designing Capacitors to Required Values

Following is the logic used in creating a simple single layered CTF capacitor design. Note also that capacitors should be placed on a single layer where possible. Since capacitance of a parallel plate capacitor is directly proportional to the plate area (A) and the dielectric constant (Dk) of the dielectric material and inversely proportional to the thickness (T) of the dielectric, the tolerance of the capacitor will be affected by the area of the plates and dielectric thickness as well as the Dk of the dielectric. Considering these variables is important to the design, especially the effective area of the plates.

The discussion in this paper is based on **a** CTF product in development by Dupont, referred to as EP310, which has a capacitance density of 92nF/cm^2. The high Dk possible with the ceramic materials enables a capacitance density of 92 nF/cm^2. Given this property, it is possible to design discrete capacitors from approximately 60 pF to 100 nF. These would have a nominal size of 0.25mm by 0.25mm to 10mm by 10 mm. When working in nF/cm^2, a constant of 1.450 must be used, i.e., C = (1.450 * Dk * A)/T expressed in nF/cm^2.

Terminology

- CTF – Ceramic thick film
- Plate and electrode – May be used interchangeably
- Controlling capacitor plate – The smaller plate. This is to assure that any mis-registration between the two plates will not change the required capacitance. Designing this plate as the copper etched plate is preferable since the control of area tolerance can be better maintained with the photo etch process than with the ceramic print process
- Printed ceramic conductor plate – The plate formed on the dielectric by the ceramic thick film printing and firing process.
- Printed ceramic dielectric – The high Dk ceramic dielectric formed on copper foil by the ceramic thick film printing and firing process.
- Drill to copper image tolerance – Expressed in mm over the drill to assure drill is at least tangent to the pad.
- Copper image to CTF image tolerance – Expressed in +/-µ is the RMS of the accumulated registration or alignment errors between the two image processes.
- Drill to CTF image tolerance – Expressed in +/- µ is the RMS of the accumulated registration or alignment errors between the drill and the CTF image processes.
- Antipad for CTF – The clearance required to assure drill to printed ceramic conductor clearance. This is equivalent to the drill to CTF image process plus 100µ per side for adequate clearance spacing.
- CAF hole edge to hole edge – Minimum recommended design spacing between hole edges to assure no conductor anodic growth issues.

- Terminations – The method of interconnecting the capacitive elements to the circuit. These can include virtually all possible combinations of using thru vias and microvias within and outside of the capacitor plates.

Design Thought Process

The following input must be determined before the discrete capacitor design can begin:

- The layer the capacitors will be placed on
- The capacitance value required
- The shape of the capacitor
- The controlling capacitor plate
- The interconnection method

Using the following relationships and the process tolerances previously discussed, the capacitor may be designed. (For the moment, allow +/-125µ process tolerance between each image)

C = required capacitance
C_D = capacitance density of selected material
A_S = overall area of the smaller (etched) plate
A_L = area lost by clearance and via
A_{CP} = area of the effective copper in the etched copper plate
$A_{CP} = A_S - A_L$
$A_{CP} = C/C_D$

Design Example

The capacitor will be placed on layer 2
The nominal capacitor value is 0.24 nF
The shape will be rectangular.
Termination to the ceramic plate will be with a thru via within the capacitor connecting to layer 1, and the copper plate will connect to a feature on layer 2 with a trace (layer 2 may be a power plane).

Following these rules, the resulting capacitor is shown in Figure 3.

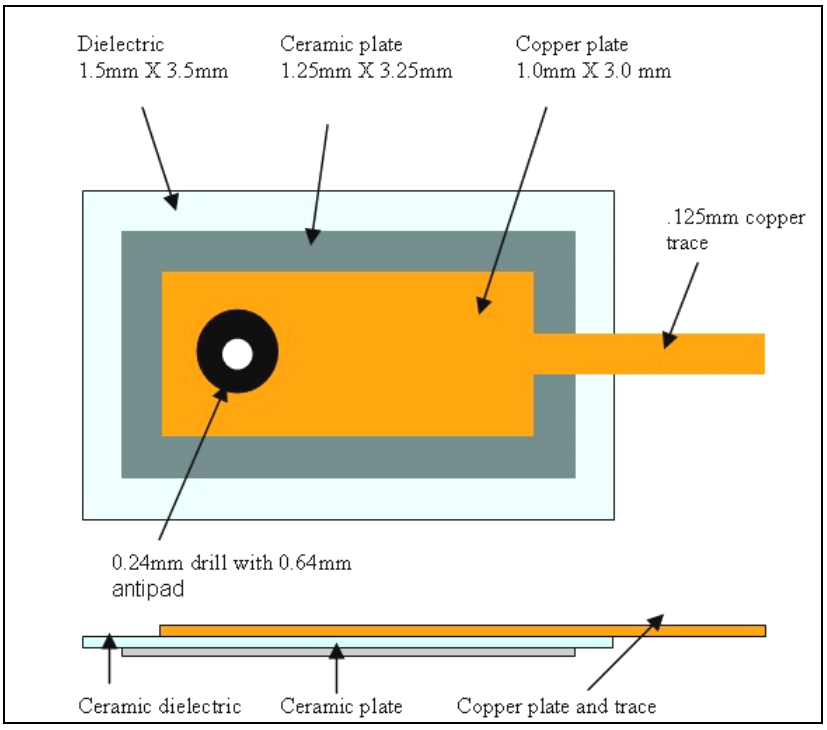

Figure 3 - Resulting Capacitor

Although this example is a very simple configuration, it illustrates the critical features. The rules and concepts used to create it can be applied to any shape and termination scheme. When more experience is gained with the performance of specific shapes, users will narrow down the capacitor choices and standards will develop. In the

meantime, this is an area where a designer can be extremely creative as long as the tolerance considerations are observed.

Conclusion

The opportunities for configurations, terminations and values of CTF embedded capacitors are huge. Currently CAD tools do not do the work. The designer is burdened with the task of creating the parts, associating the elements and embedding them into the appropriate layers. Understanding the PCB and CTF manufacturing processes and incorporating the appropriate tolerances in the design is critical to the success of embedding these parts. Tools will be available, however, in the interim, basic guidelines and experience with a manual process is a feasible approach to designing CTF capacitors into PCBs.

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