Three-Dimensional System-in-Package (3D-SiP) in Japan: The Second Stage of Development

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Abstract
The adoption of three-dimensional System-in-Package (3D-SiP) is progressing rapidly, driven primarily my mobile electronic applications such as mobile phones, PDAs, digital still cameras, and digital video recorders. The underlying, enabling Chip Size Packaging (CSP) technologies can be broadly classified into two types: chip-stacking and package-stacking. In Japan, both of these stacking methods have reached maturation in terms of the fundamental manufacturing processes required for cost-effective mass production. Meanwhile, chaos reigns on issues such as supply logistics and IP ownership.

This paper and presentation will focus on the examples of increasingly high-function mobile electronics applications enabled by 3D-SiP being developed and released into Japanese and overseas markets, as well as the accompanying demand for continued 3D-SiP technology development based upon industry-wide standards in order to encourage and support rapid adoption in the marketplace.

Introduction
The world's first chip-stacked Chip Size Packaging (CSP) was developed by Sharp and was used in Japanese mobile phones in April 1998. That product used a combination memory made up of 16 Mb of flash memory and 2 Mb of SRAM. Subsequently, virtually all mobile phones adopted combination memory that used the chip-stacked CSP technology. It would not have been possible to build the latest mobile phones without that technology.

As the functionality of mobile phones has increased, the number of chips stacked in one combination memory CSP has increased year by year to the point that packages with 3- or 4-chip layers are the norm. At the same time, there has also been a steady increase in stacked-chip products that combine logic ICs and memory, heralding the era of true SiP. At last year's IPC Annual Meeting 2002 and Technical Conference, held in New Orleans, the author gave a presentation entitled "3-D System In Package (SIP) Era Driven by Mobile Phones."[1] In this paper the author discusses subsequent SiP growth in Japan. (3-D SIP= 3D-SiP)

Why the Focus on 3D-SiP
Although 3D- SiP have been the focus of attention for several years now, expectations of rapid growth in the 3D-SiP business have been mounting recently, accompanied by a surge in discussion of the topic among academics and the media. Those involved in semiconductor packaging technology, as are the authors, have consistently argued for the importance of the 3D-SiP. Many have now come to share this viewpoint, including not only those involved in process engineering and IC design and engineering within semiconductor manufacturers, but also those involved in product design who are the customers of semiconductor manufacturers. It is likely to be these changing trends that led to today's boom in SiP.

However, to understand the background, we must take a wide view of electronic equipment design and manufacturing, examining the steps in the sequence of development. For semiconductor manufacturers there are two key aspects: issues relating to silicon chip design, and those of process and packaging technology. For product design and the associated development of manufacturing technology, we must understand the great impact the 3D-SiP is having on these areas, and how it is this that is attracting the attention of people responsible for product development. These relationships are shown schematically in Figure 1. Put briefly, the situation is as follows: the 3D-SiP is strongly related to the both the System on Chip (SoC) and System on Board (SoB) sectors, and is expected to expand into them.

Although 3D-SiP development has been driven from the area of manufacturing technology, and it is possible today to stack chips in four or even five layers, development of the business model is lagging. This is largely due to the distinctive features of 3D-SiP. In short, because SiP are complete systems and are close to being the final product, the components that make up the system are so diverse that single companies cannot provide all the components needed. This makes the business side of things very complex, leading to such lagging. To simplify these complex business relationships, Sharp, together with Amkor Technology, Inc. (U.S.A.), put forward the world's first proposal for standardizing the outlines and terminal layout of 3D-SiP in March 2003.

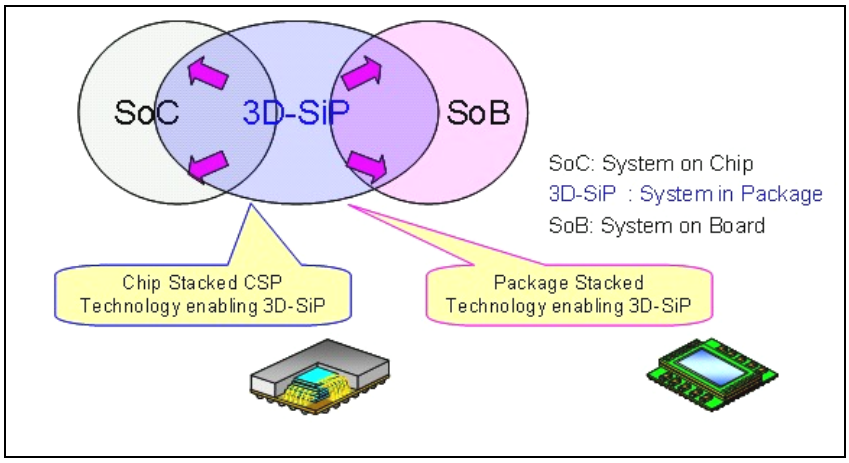


Figure 1- Correlations between SoC, SoB, 3D-SiP and Package Technology

Silicon Chip Process and IC Design[2]

Historically, since the creation of the semiconductor IC, progress in electronic devices has definitely been attributable to the design shrinkage of silicon chips. Originally proposed in 1965, Moore's Law states that the integration of semiconductor chips doubles every 18 months, and the fact that this Law still holds attests to the importance of shrinkage. It is predicted that this framework will not change for some time to come. However, as process design rules break through the 0.1-micron level, numerous problems have arisen in building all the required functions into a monolithic silicon chip (i.e., in realizing so-called system ICs). In other words, the limitations of or problems with SoC have begun to reveal themselves. Limitations are mainly as follows: It is fair to say that these problems with SoC have acted as an incentive for SiP development.

1. Exorbitantly high cost
   - Cost of a mask set for a 0.09 micron process is about $100 million
   - Custom chips have become predominant, and there are almost no models (other than game chips) whose lifetime production volume exceeds 1 to 3 million pieces
2. Much longer development period for product value
   - Development of a system IC takes 1 to 2 years, but product lifetime is only a few months (about 6 months for mobile phones)
3. A long adjustment time required to respond to specification changes
   - A change in the mask takes at least a few months
4. Difficulty in optimizing the mixture of logic, analog, and memory circuitry
   - Operating voltage disparity: Circuits that can operate at low voltage are mixed with those that cannot (Logic: near 1 to 2 V; analog: 2 to 4 V; DRAM: 2 to 4 V; Flash: 2 to 3 V, and over 10 V)
   - Design rule disparity: Shrinkage of analog circuitry is difficult
5. Transistor leakage
   - It has become impossible to ignore power consumption due to transistor leakage when the device is not operating
6. The trend toward software processing due to system hypertrophy, and the need for high-capacity memory
7. Memory diversification
   - DRAM, NOR Flash, NAND Flash, SRAM, PSRAM, etc.

Package Technology[3]

With regard to package technology, it is considered that chip-stacked CSP development created the opportunity for switching to the 3D-SiP and gave it impetus. As discussed above, in 1998, Sharp developed a technology for use in mobile phones in which two chips (Flash memory and SRAM) were stacked into a CSP the same size as a single chip. This technology was successfully applied to mass production. The author regards this as the beginning of the 3D-SiP. We have consistently led the world in stacked technology, mass-producing a 3-chip stacked CSP in 1999 and a 4-chip stacked CSP in 2001, and advocating the concept of stacking packages successfully realizing 3D-SiP in March 2002. Our early products were memory-memory combinations, which could hardly be called bona fide SiP; however, from the standpoint of package technology, they were real 3D-SiP. These devices triggered the growth in 3D-SiP centered around mobile phone applications. We are now producing a wide range of products, not only combinations of logic and memory but also combinations including image sensors and DSPs.

In contrast with the design shrinkage of silicon , the technology for stacking multiple chips in a CSP is a type of three-dimensional integration. Hence the ability of the 3D-SiP to raise the silicon functionality (per unit area) of a SoC by many

times is one reason it has gained priority. In summary, from the standpoint of package technology it is thought that the following two trends have encouraged the development of the SiP:

1. The advent and evolution of chip-stacked CSPs
2. Realization of functionality a few generations beyond that achievable through process shrinkage by means of three-dimensional integration

Furthermore, it is thought that the 3D-SiP will be boosted by its ability to realize a chip with different functions and processes that are difficult to combine using monolithic devices (such as logic, analog, and memory circuitry) essentially in a single device (1 package).

SiP and SoC

In comparisons of SiP and SoC, it is often said that the SiP technology is one that supplements SoC technology. However, the author feels that SiP and SoC are equivalent and have a complementary rather than supplementary relationship. The author would assert that the combined technologies meet needs that they cannot satisfy individually. Figure 2 illustrates this relationship.

There are also those who assert that SiP technology is merely a stopgap until SoC technology is fully realized, but the author would claim that this is not the case and that SiP is an important technology capable of solutions that cannot be addressed by SoC technology. For example, combination memory, which began in 1998 by combining flash memory and SRAM chips, shows no tendency to become monolithic even five years later, rather combinations of memory types have been supplemented by logic, analog and memory, etc., which would be extremely difficult to achieve using SoC technology. The table in Figure 3 shows the pros and cons of SiP as compared to SoC.

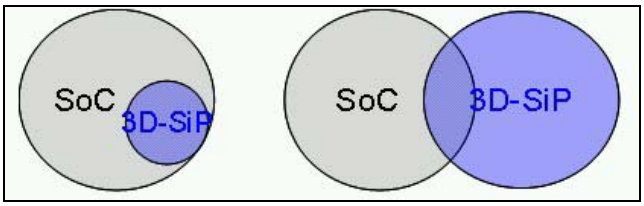


Figure 2- Relationship between SiP and SoC (left: supplementary; right: complementary)

(compare to SoC)

Pros	Cons
1. Lower NRE 2. Short TAT 3. Lower cost for many types of products 4. Possible to combine different types of functional devices (Memory, Logic, Analog) 5. Possible to use current ICs 6. Possible to combine different companies devices 7. Easy to make optimized system 8. Easy to make larger and more complex system 9. Higher Si efficiency (Smaller PCB area) 10. Reduce PCB cost (Less PCB layer) 11. Easy to make system change	1. Difficult to make higher system speed 2. Higher cost in large volume production

Figure 3- Pros and Cons of SiP as Compared to SoC

Effects on Product Design and Manufacturing

In conventional products, a technique called surface mount technology (SMT) has been in use since the 1980s and become the de facto standard throughout the world. The 3D-SiP has the potential of changing this basic framework. As more electronic devices are incorporated at high density into a 3D-SiP, it becomes possible to achieve larger systems in a single device (package), with the relative value of SMT being decreased. The effective use of SiP prior to other companies improves product differentiation and competitiveness. Simultaneously there may be a rush for added value between semiconductor manufacturers and product manufacturers. This is a business opportunity in an area in which Japan is strong.

Packaging in the Japanese Latest Mobile Phones

In this section, we will discuss the ways in which the now commonplace chip-stacked CSPs are used in mobile phones in Japan and how that usage is changing. Figure 4 shows the situation for the main packages used in mobile phones in Japan over a 3-year period from 2001 to 2003. Starting from the left of the table, the figures show the total numbers of packages used, the number of logic packages used, the number of memory packages used, the memory capacity, and the number of memory chips.

If we focus on the numbers of memory packages, the memory capacity and the number of memory chips, it becomes clear that the reason behind the need for chip-stacked CSP technology and the year-by-year increase in the number of layers used. In short, the increasingly strident demand from the market for greater functionality in mobile phones has led to the memory capacity doubling or tripling each year. However, according to Moore's Law, the integration of semiconductor chips only doubles every 18 months. So if memory capacity is to increase at a rate faster than that stipulated in Moore's Law, the only way is to increase the number of chips. However, the mounting area available in mobile phones cannot be increased. We inevitably come to the conclusion that the only solution is to stack chips in layers (3D-chips) more and more. The numbers in Figure 4 make it clear that this is what is actually happening now with the chips installed in mobile phones in Japan.

We also know that memory is becoming more diverse, as in the case of NAND flash memory. In addition, what is not shown in the table below is that stacked CSPs made up of logic chips and memory chips are also being used, indicating that 3D-SiP chips are now moving into a second stage.

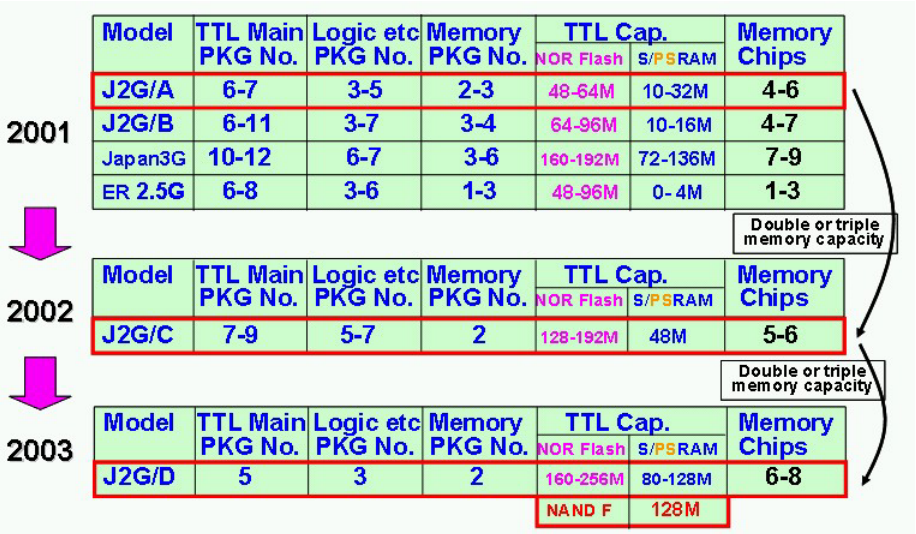


Figure 4- Main Packages used in the Latest Mobile Phones and the Progress in Si Chip Content

3D-SiP and Package Technology

Chip-stacked CSPs, presently the de facto standard for mobile phones, created the opportunity for the shift to 3D-SiP. The memory capacity required by mobile phones will continue to increase far into the future. Meanwhile, progress will be made in developing chip-stacked CSPs with more levels of stacking and thinner layers.

However, in shifting to the higher density systems of the future, we must consider not only chip stacking, but also package height (thin chips), interconnection between chips, yield, and combination limitations. For example, if we try to achieve a 10-chip stack with the current maximum height of 1.4 mm, chip thickness must be reduced to 20 to 25 μm. This will present a number of problems that cannot be easily resolved by extending current technology (i.e., pre-assembly technology, wafer handling technology, chip electrical characteristics, package reliability, and ensuring high yield). Furthermore, when a system solution is provided by chip stacking, it is difficult for the same company to supply all memory chips, such as Flash, SRAM and PSRAM, as well as the logic chips and analog chips. A number of problems must be solved, including:

1. Testing technology development (KGD: Known Good Die, testability)
2. Business model establishment (distribution of various LSI chips)
3. Reliability assurance
4. Provision of system follow-up for users.

When these problems are considered, there are many situations where it is easier to use package stacking rather than chip stacking. Package stacking has a number of advantages, such as:

1. There are fewer constraints on the applicable devices and stacking because it is possible to stack only good packages little affected by yield problems.
2. It is possible to flexibly respond to specification changes, such as changes in memory capacity because individual chips
3. are combined.
4. Combination with chips from other companies is easier, and the KGD problem can be solved.
5. It is possible to incorporate passive components.

These advantages make it easier to provide a system solution with package stacking.

Figure 5 shows the structure and appearance of a package stack developed by Sharp. In a memory type designed for high-capacity memory, a device hole is provided in the center of a 2-layer wiring board, and two chips are stacked in that hole. Connection between the boards is achieved via wire bonding, and after that the unit is resin molded. Mounting height is 0.55 mm with one package, and 1.5 mm with a 3-package stack (6-chip stack).

There are two types for logic chips. The first has the same structure as the memory type, and is thin-compatible having terminals laid out in four directions. With this version it is possible, for example, to stack multiple memory types on a single logic chip, and thereby realize a 5-chip stack (ASIC logic chip x 1 package, + memory type x 2 packages) with a thickness of 1.4 mm. The mounting area for the memory devices can thereby be reduced to virtually zero. The second version is for logic type ASIC higher pin-count ICs in the 300 to 400-pin class, such as the mobile phone base band chip and application processors. This version has a cavity structure that enables wiring even in the area directly below the chip.

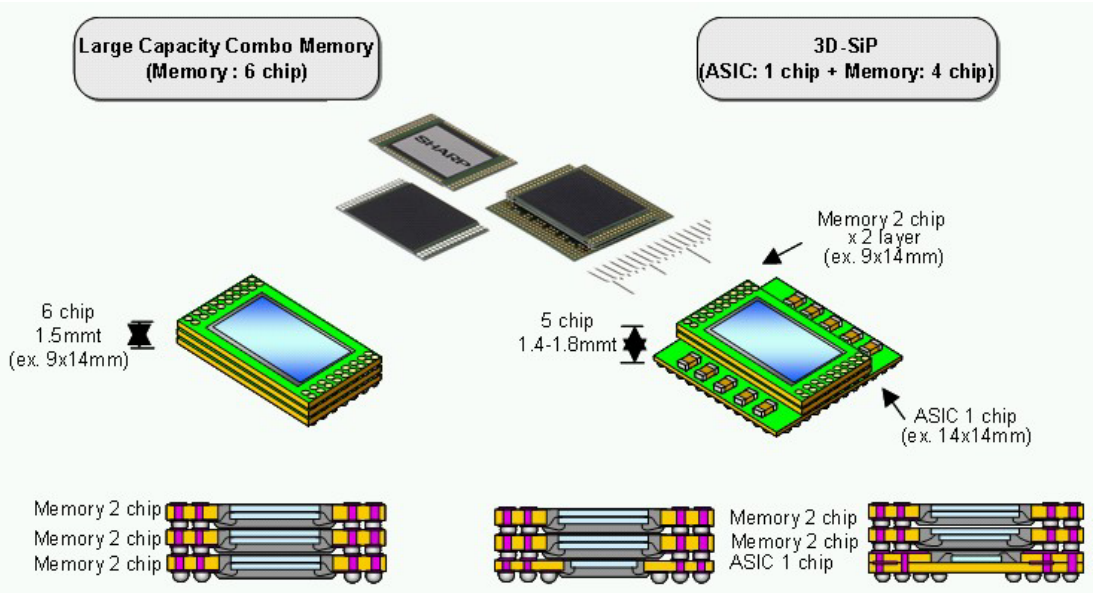


Figure 5- Example of the application of package stacking technology to create a 3D–SiP

At present there are many cases where the ASIC chip terminal layout is not designed to be stacked with memory, and complex wiring must be used across the package board. In cavity-structure higher pin-count ICs types, the degree of freedom for this wiring is greatly increased. Furthermore, the arrangement of via holes near the chip improves the heat characteristics of the package. Naturally the memory type can also be stacked on this package, thereby providing an ideal 3D-SiP.

Efforts to Standardize 3D-SiP

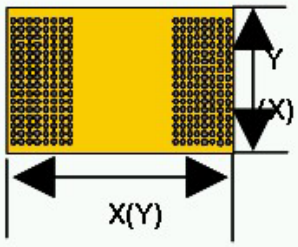
Package Outline Standardization

Having started with chip-stacked CSPs, Sharp has consistently proposed the package stack as a 3D-SiP. There are currently high expectations of the 3D-SiP as a key technology for the future, and various structures and specifications have been proposed by different companies. However, there is as yet no uniformity, and specifications must be standardized in order to achieve full-scale development and dissemination. Hence, we agreed with Amkor Technology Inc. to unify outline specifications for the 3D-SiP, and thereby enable systemization by stacking ultra-thin packages.

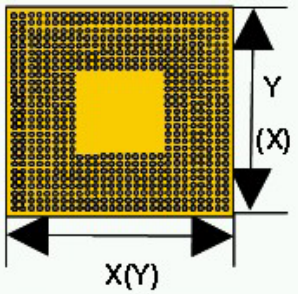
The specific proposal is shown in Figures 6 to 8. It is based on the current outline standards of the Japan Electronics and Information Technology Industries Association (JEITA) and the JEDEC Solid State Technology Association for fine-pitch ball grid arrays (FBGA), and proposes a standard outline size, terminal pitch, number of terminals and package height. For

package height in particular, we considered combination of the three types of FBGA height specifications (XFBGA, UFBGA and WFBGA), proposed stacking of up to four packages, and introduced the first standardized package stacking concept.

BODY SIZE		X,Y : Mmax+1 MATRIX		MAX PIN	X,Y : Mmax MATRIX		MAX PIN	X: Mmax+1, Y: Mmax MATRIX		MAX PIN
X	Y	X	Y		X	Y		X	Y	
9	9	18	18	324	17	17	289	18	17	306
	10		20	360		19	323		19	342
	11		22	396		21	357		21	378
	12		24	432		23	391		23	414
	13		26	468		25	425		25	450
	14		28	504		27	459		27	486
10		20			19			20	17	340
	10		20	400		19	361		19	380
	11		22	440		21	399		21	420
	12		24	480		23	437		23	460
	13		26	520		25	475		25	500
	14		28	560		27	513		27	540
11		22			21			22	17	374
									19	418
	11		22	484		21	441		21	462
	12		24	528		23	483		23	506
	13		26	572		25	525		25	550
	14		28	616		27	567		27	594
12		24			23			24	17	408
									19	456
									21	504
	12		24	576		23	529		23	552
	13		26	624		25	575		25	600
	14		28	672		27	621		27	648
13		26			25			26	17	442
									19	494
									21	546
									23	598
	13		26	676		25	625		25	650
	14		28	728		27	675		27	702
14		28			27			28	17	476
									19	532
									21	588
									23	644
									25	700
	14		28	784		27	729		27	756



2-sided terminal



4-sided terminal

Figure 6- Proposal for Standardizing the 0.5-mm Pitch Terminal Matrix

BODY SIZE		X,Y : Mmax+1 MATRIX		MAX PIN	X,Y : Mmax MATRIX		MAX PIN	X: Mmax+1, Y: Mmax MATRIX		MAX PIN
X	Y	X	Y		X	Y		X	Y	
9	9	14	14	196	13	13	169	14	13	182
	10		15	210		14	182		14	196
	11		17	238		16	208		16	224
	12		18	252		17	221		17	238
	13		20	280		19	247		19	266
	14		21	294		20	260		20	280
10	9	15	14	210	14	13	182	15	13	195
	10		15	225		14	196		14	210
	11		17	255		16	224		16	240
	12		18	270		17	238		17	255
	13		20	300		19	266		19	285
	14		21	315		20	280		20	300
11	9	17	14	238	16	13	208	17	13	221
	10		15	255		14	224		14	238
	11		17	289		16	256		16	272
	12		18	306		17	272		17	289
	13		20	340		19	304		19	323
	14		21	357		20	320		20	340
12	9	18	14	252	17	13	221	18	13	234
	10		15	270		14	238		14	252
	11		17	306		16	272		16	288
	12		18	324		17	289		17	306
	13		20	360		19	323		19	342
	14		21	378		20	340		20	360
13	9	20	14	280	19	13	247	20	13	260
	10		15	300		14	266		14	280
	11		17	340		16	304		16	320
	12		18	360		17	323		17	340
	13		20	400		19	361		19	380
	14		21	420		20	380		20	400
14	9	21	14	294	20	13	260	21	13	273
	10		15	315		14	280		14	294
	11		17	357		16	320		16	336
	12		18	378		17	340		17	357
	13		20	420		19	380		19	399
	14		21	441		20	400		20	420

Figure 7 - Proposal for Standardizing the 0.65-mm Pitch Terminal Matrix

The above specifications have so far been adopted by two companies (Sharp and Amkor), and in the future we plan to encourage their adoption by other companies. If various companies offer 3D-SiP conforming to these specifications,

compatibility and hence design convenience will be improved for users, and we believe this well help lead to the full-scale dissemination of the 3D-SiP.

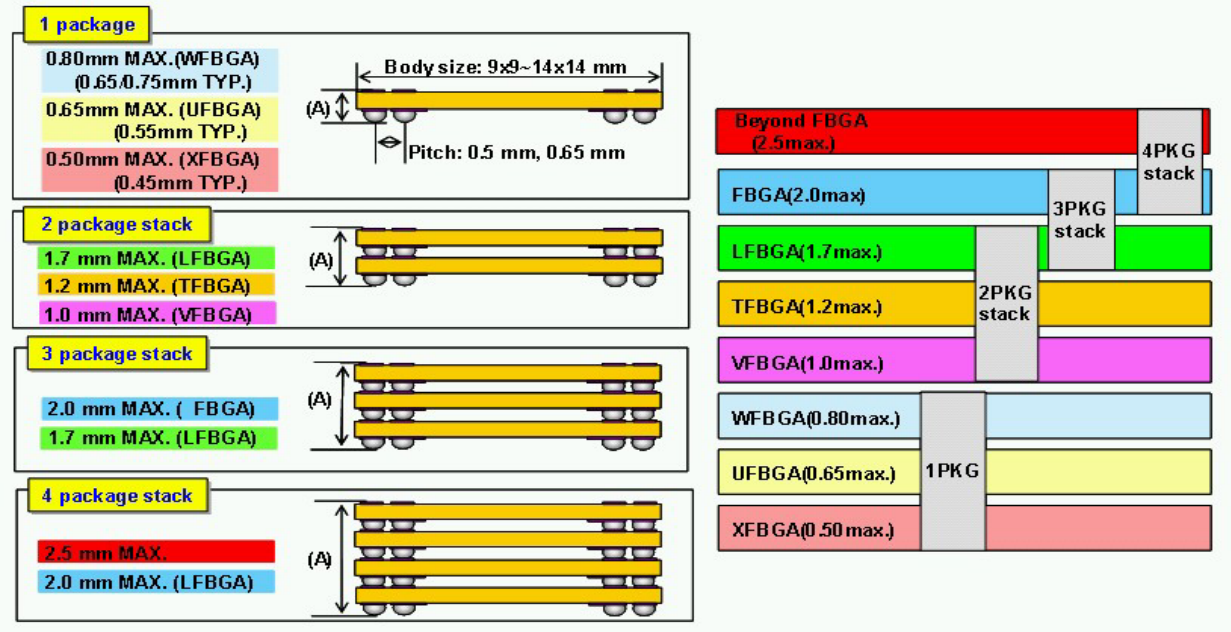


Figure 8- Proposal for Standardizing the Package Height

Memory Terminal Layout Standardization

JEDEC has made progress in the standardization of terminal layouts for chip-stacked CSP combination memory, and this has contributed to the rapid growth and spread of combination memory. For package stacked 3D-SiP too, we must standardize the terminal layout concept assuming a mix of memory and logic. Figure 9 shows our concept. Outline size is standardized relative to the terminal layout (package top and back) of the memory type (combination memory such as Flash memory, SRAM, PSRAM), and in the logic type, land terminals are laid out so that the memory device can be connected to the back of that package. This makes it possible to improve the general applicability of the memory device fitted, and expand shared aspects of board and circuit design for users. The package outline standardization described above takes into consideration this memory terminal standardization.

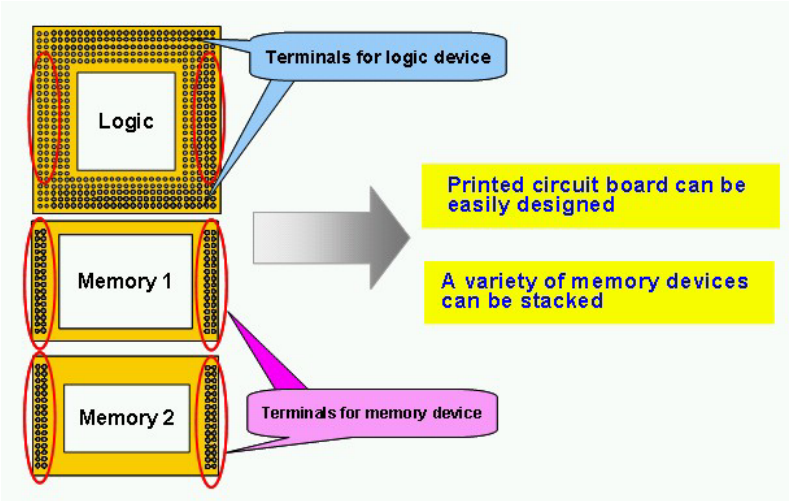


Figure 9- Proposal for Standardizing Memory Terminal Layout

Issues and Future Outlook for SiP

As the limitations of SoC become evident, it is the authors' belief that the 3D-SiP will take the place of SoC in meeting future system requirements for performance, cost and development time, and that the first 10 years of the 21st century will be the era of the 3D-SiP. However, we have gone beyond the germination period, and it is also clear that many problems, as described below, still remain. These must be resolved in both the business and technology domains.

Business

1. Applications must be extended (With usage limited to mobile phones the market will be unreliable. Applications must expand to include digital home appliances).
2. Distribution and business models must be developed for silicon chips and IC devices (One company cannot supply a diverse range of memory, logic and analog devices. Overall responsibility must be determined).
3. A profitable business model must be developed (1 + 1 = 2 + Premium price).

Technology

4. An optimal design for switching to 3D-SiP must be developed (Standardization of outline, pin out, I/O, etc).
5. The design environment must be established (Electrical, thermal and physical, for uniform handling of chips, packages and mounting boards.)
6. Package technology must be advanced (Multi-layer stacking of chips, cost reduction, refinement, multi-layer metal board technology)
7. Test technology must be developed (KGD, testability, burn-in)
8. Reliability assurance must be established
9. Necessity for built-in passive components must be determined (Must components such as high-value capacitors remain?)
10. How to accommodate RF circuits must be determined

Although there are constraints on the functions of SoC, they will definitely have to coexist with and complement 3D-SiP. It is said that the future of SiP and SoC will be determined not by the PC, but rather by consumer electronics, which is directed at a fickle consumer. Hence the future outcome depends on the degree to which we can find large-volume applications (products) such as mobile phones, which can drive the mass production of devices.

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Exotic Interconnections and Advanced Process Capability

Three-Dimensional System-in-Package (3D-SiP) in Japan: The Second Stage of Development

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SHARP

1. Introduction

Three-Dimensional System-in-Package (3D-SiP) in Japan: The Second Stage of Development

1. Expansion of application
: Mobile phones to digital consumer products

2. Not only combination memory but also ASIC + Memory and Camera module

3. Expansion of business alliance between companies

4. Increasing of involved companies and institutes

5. Focusing from packaging technology to circuitry design

3. Silicon Chip Process and IC Design

Silicon Chip Process and IC Design

1. Exorbitantly high cost
   - -Cost of a mask set for a 0.09 micron process is about $100 million
   - -Custom chips have become predominant, and there are almost no models (other than game chips) whose lifetime production volume exceeds 1 to 3 million pieces
2. Much longer development period for product value
   - - Development of a system IC takes 1 to 2 years, but product lifetime is only a few months (about 6 months for mobile phones)
3. A long adjustment time required to respond to specification changes
   - - A change in the mask takes at least a few months

3. Silicon Chip Process and IC Design

Silicon Chip Process and IC Design

4. Difficulty in optimizing the mixture of logic, analog, and memory circuitry
   - Operating voltage disparity: Circuits that can operate at low voltage are mixed with those that cannot (Logic: near 1 to 2 V; analog: 2 to 4 V; DRAM: 2 to 4 V; Flash: 2 to 3 V, and over 10 V)
   - Design rule disparity: Shrinkage of analog circuitry is difficult
5. Transistor leakage
   - It has become impossible to ignore power consumption due to transistor leakage when the device is not operating
6. The trend toward software processing due to system hypertrophy, and the need for high-capacity memory
7. Memory diversification
   - DRAM, NOR Flash, NAND Flash, SRAM, PSRAM, etc.

3. Silicon Chip Process and IC Design

Package Technology

1) The advent and evolution of chip-stacked CSPs

1998:2-chip stacked CSP

1999:3-chip stacked CSP

2001:4-chip stacked CSP

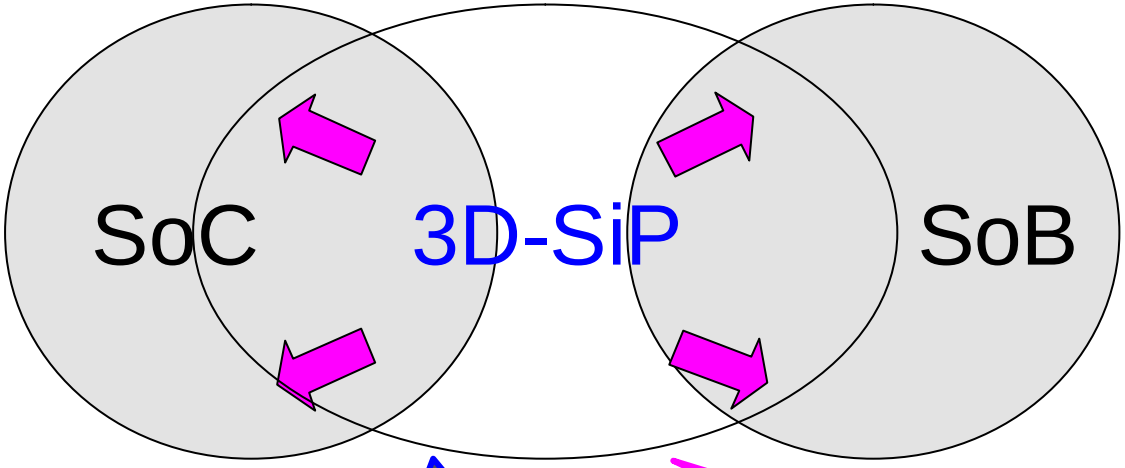
2002:Package stacked CSP

From

Memory+Memory to Logic+Memory or Logic+ Logic

2) Realization of functionality a few generations beyond that achievable through process shrinkage by means of three-dimensional integration

Correlations between SoC, SoB, 3D-SiP and package technology



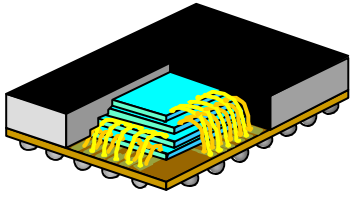
SoC: System on Chip

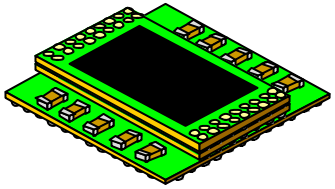
3D-SiP : System in Package

SoB: System on Board

Chip Stacked CSP
Technology enabling 3D-SiP

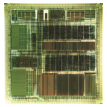
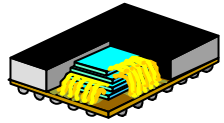
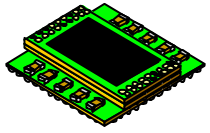
Package Stacked
Technology enabling 3D-SiP



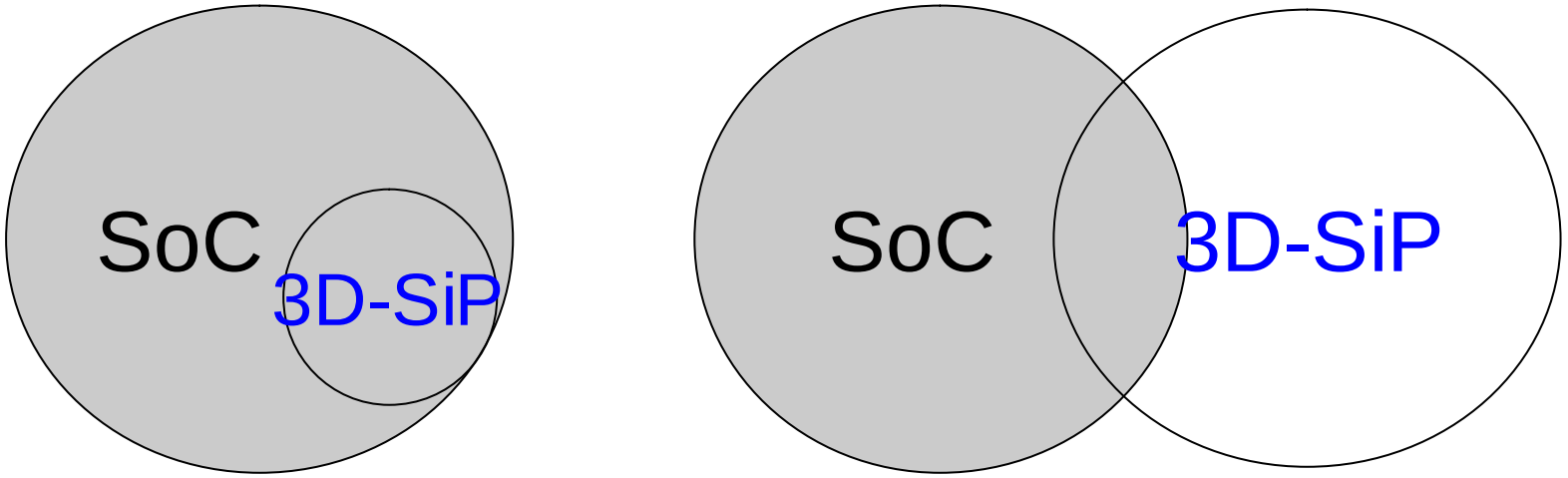


Pros and cons of SiP as compared to SoC

(compare to SoC)

Pros	Cons
1.Lower NRE 2.Short TAT 3.Lower cost for many types of products 4.Possible to combine different types of functional devices (Memory, Logic, Analog) 5.Possible to use current ICs 6.Possible to combine different companies devices 7.Easy to make optimized system 8.Easy to make larger and more complex system 9.Higher Si efficiency (Smaller PCB area) 10.Reduce PCB cost (Less PCB layer) 11.Easy to make system change	1.Difficult to make higher system speed 2.Higher cost in large volume production   

Relationship between SiP and SoC (left: supplementary; right: complementary)



Main Packages and ICs in Latest Mobile Phones(2001-2002-2003)

2001

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap.		Memory Chips
				NOR Flash	S/PSRAM	
J2G/A	6-7	3-5	2-3	48-64M	10-32M	4-6
J2G/B	6-11	3-7	3-4	64-96M	10-16M	4-7
Japan3G	10-12	6-7	3-6	160-192M	72-136M	7-9
ER 2.5G	6-8	3-6	1-3	48-96M	0- 4M	1-3

Double or triple memory capacity

2002

Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap.		Memory Chips
				NOR Flash	S/PSRAM	
J2G/C	7-9	5-7	2	128-192M	48M	5-6

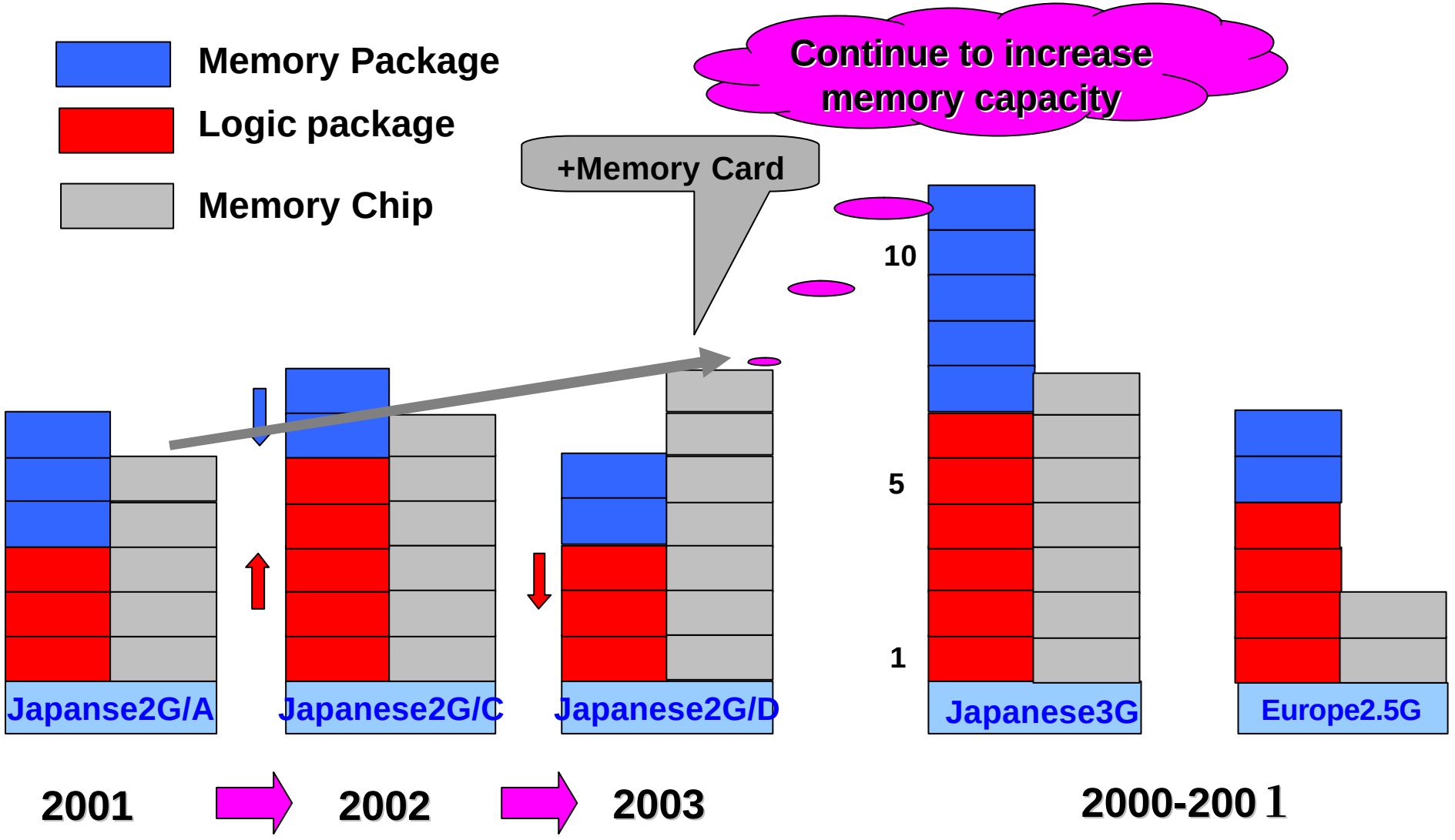
Double or triple memory capacity

2003

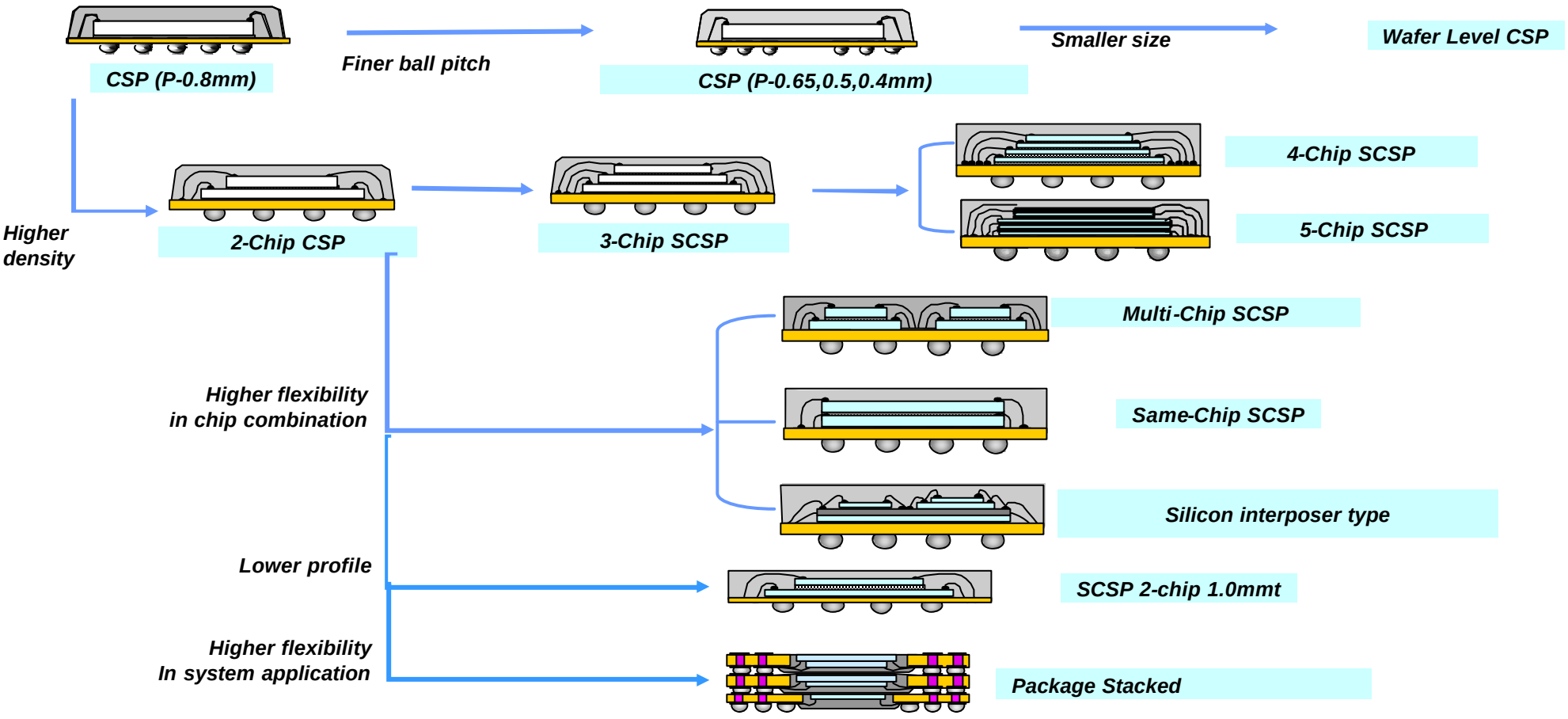
Model	TTL Main PKG No.	Logic etc PKG No.	Memory PKG No.	TTL Cap.		Memory Chips
				NOR Flash	S/PSRAM	
J2G/D	5	3	2	160-256M	80-128M	6-8
				NAND F	128M	

+Memory Card

Main Package Count and Memory Chip Count in Latest Mobile Phones (2001-2002,2003)

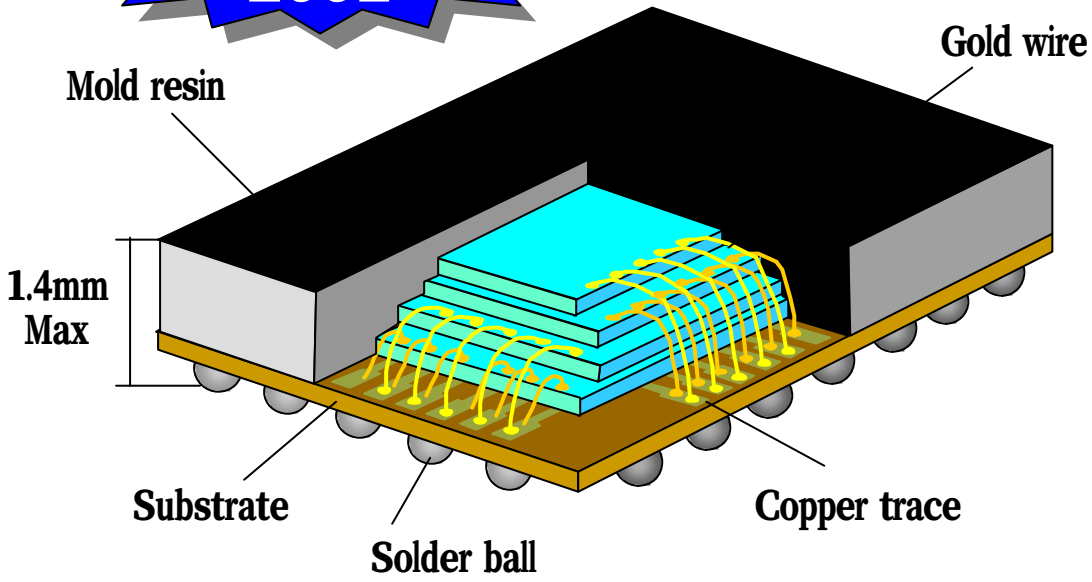


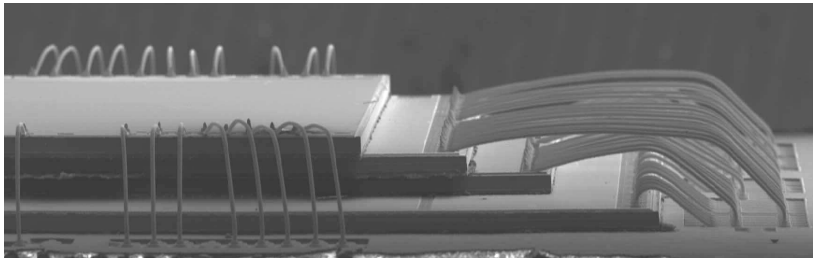
3D-SiP Map



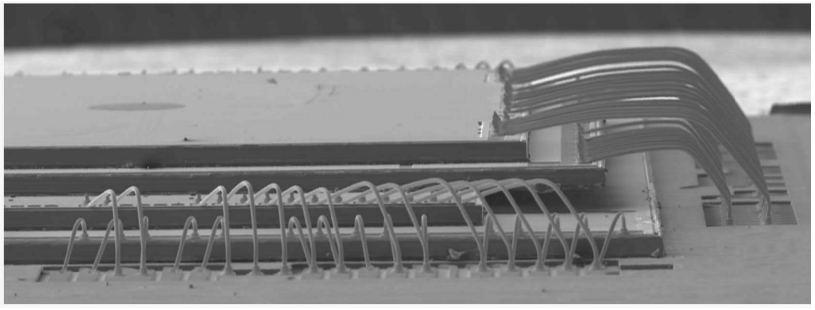
4-Chip Stacked CSP

World First
2001

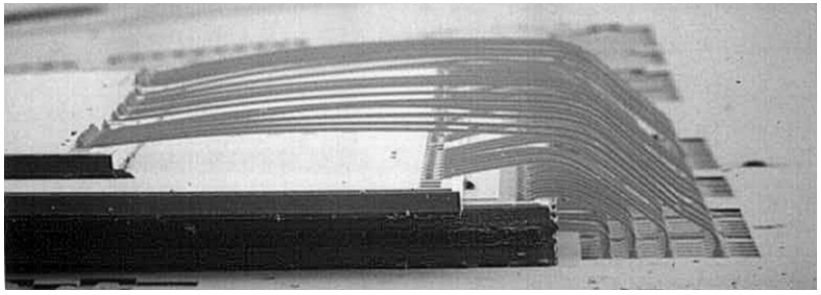




(a) Pyramid system



(b) Over hanging structure

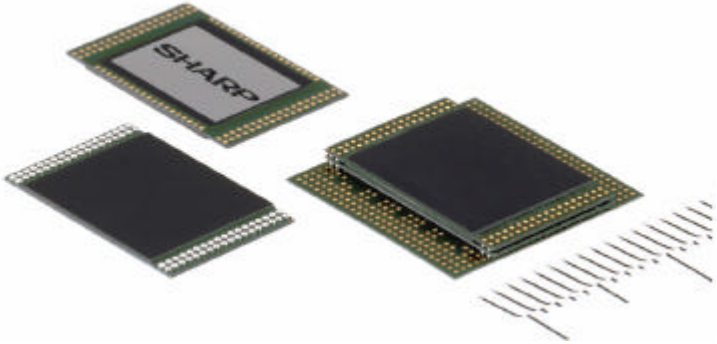


(c) Same chip structure

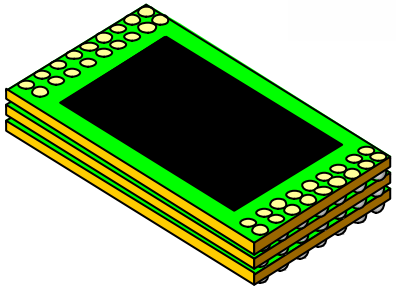
Package Stacked technology

Large Capacity Combo Memory
(Memory : 6 chip)

3D-SiP
(ASIC: 1 chip + Memory: 4 chip)

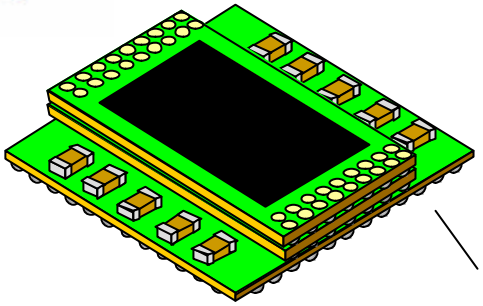


6 chip
1.5mmt
(ex. 9x14mm)



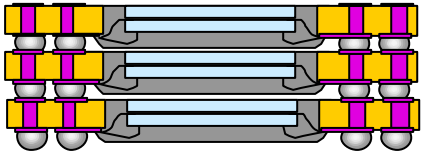
5 chip
1.4-1.8mmt

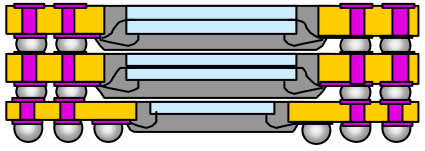
Memory 2 chip
x 2 layer
(ex. 9x14mm)



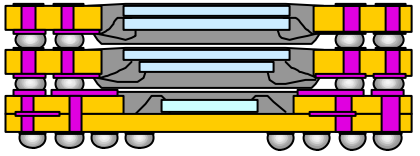
ASIC 1 chip
(ex. 14x14mm)

Memory 2 chip
Memory 2 chip
Memory 2 chip

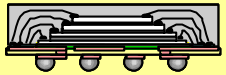
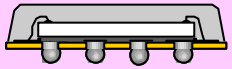
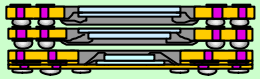
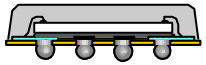




Memory 2 chip
Memory 2 chip
ASIC 1 chip

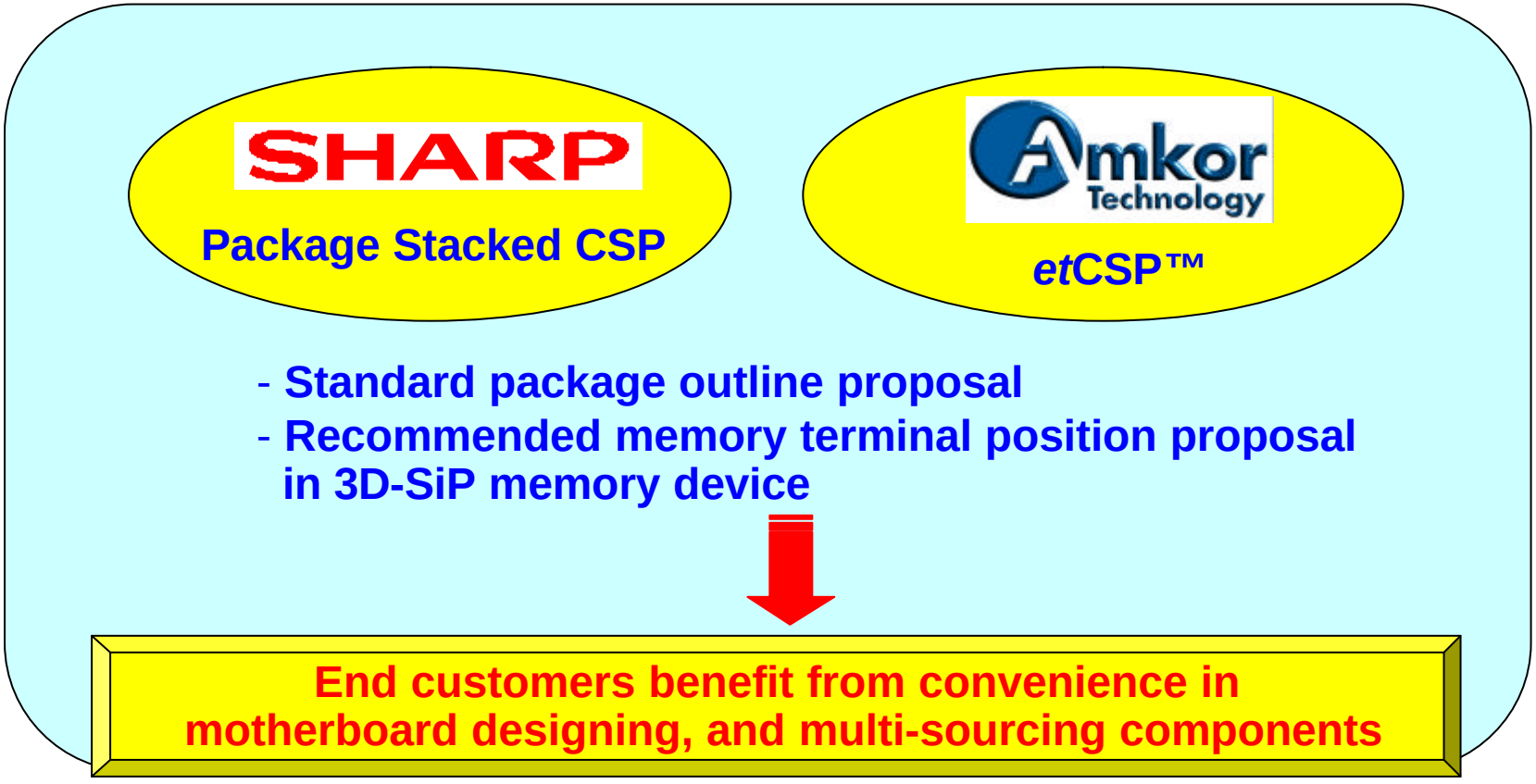


Comparison of Mounting Area for Current Packages and Package Stack on a Japanese Mobile Phone

Current	Package Stack
Memory (4-chip)  8×11=88mm²	No memory area!! on board
ASIC(B.B)  12×12=144mm²	 Memory (4-chip) ASIC(B.B) +Analog 14×14=196mm²
Analog  10×10=100mm²	
Mounting Area 332mm²	196mm² (-41%)

3D-SiP Design Unification by Sharp and Amkor

- **First 3D-SiP standard design proposal**
- **First standardized concept introduced as stacked package**



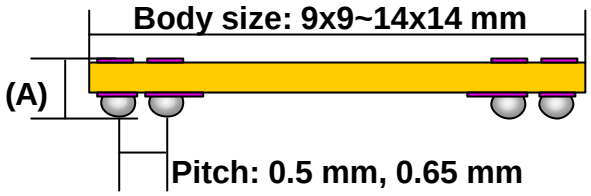
Proposed 3D-SiP Standard Outline

1 package

0.80mm MAX.(WFBGA)
(0.65/0.75mm TYP.)

0.65mm MAX. (UFBGA)
(0.55mm TYP.)

0.50mm MAX. (XFBGA)
(0.45mm TYP.)



2 package stack

1.7 mm MAX. (LFBGA)

1.2 mm MAX. (TFBGA)

1.0 mm MAX. (VFBGA)

3 package stack

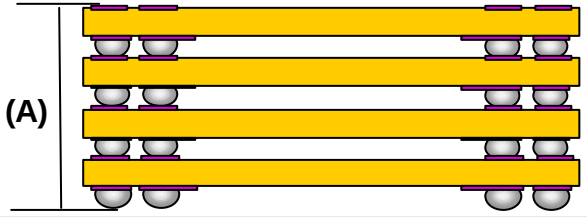
2.0 mm MAX. (FBGA)

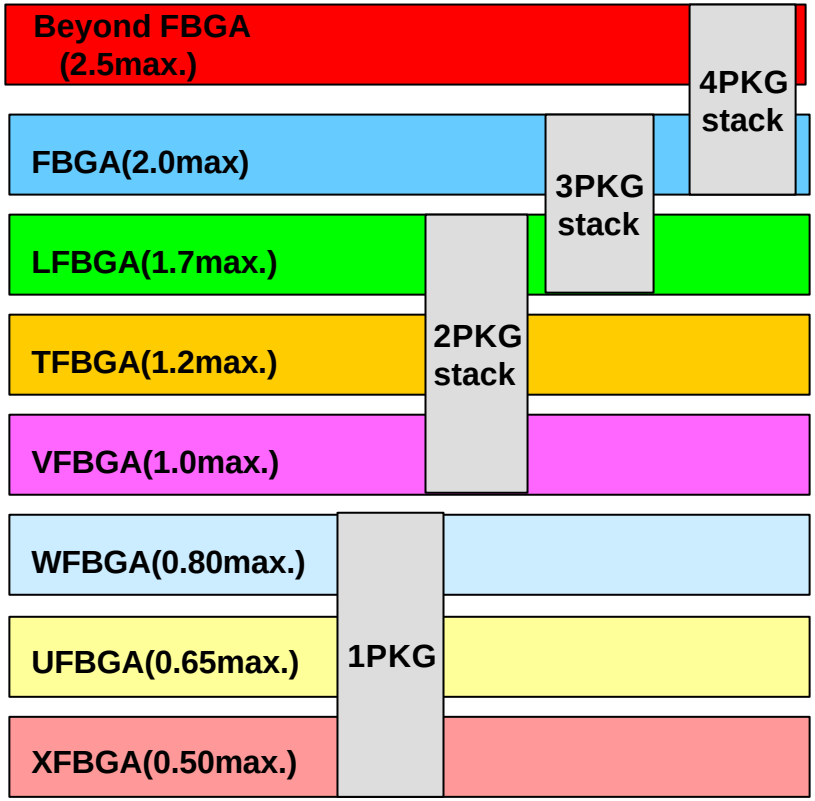
1.7 mm MAX. (LFBGA)

4 package stack

2.5 mm MAX.

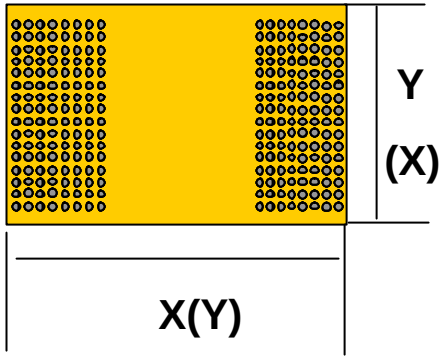
2.0 mm MAX. (LFBGA)



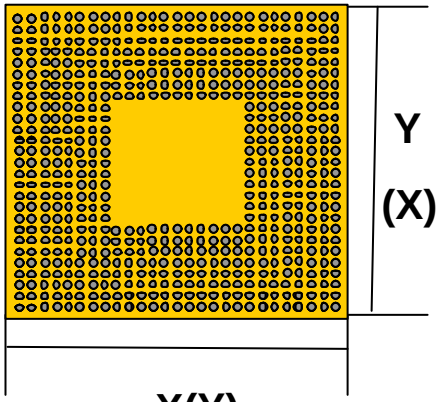


Proposed Terminal Count (0.5mm-P)

BODY SIZE		X,Y : Mmax+1			X,Y : Mmax			X: Mmax+1, Y: Mmax		
		MATRIX		MAX	MATRIX		MAX	MATRIX		MAX
X	Y	X	Y	PIN	X	Y	PIN	X	Y	PIN
9	9	18	18	324	17	17	289	18	17	306
	10		20	360		19	323		19	342
	11		22	396		21	357		21	378
	12		24	432		23	391		23	414
	13		26	468		25	425		25	450
	14		28	504		27	459		27	486
10		20			19			20	17	340
	10		20	400		19	361		19	380
	11		22	440		21	399		21	420
	12		24	480		23	437		23	460
	13		26	520		25	475		25	500
	14		28	560		27	513		27	540
11		22			21			22	17	374
									19	418
	11		22	484		21	441		21	462
	12		24	528		23	483		23	506
	13		26	572		25	525		25	550
	14		28	616		27	567		27	594
12		24			23			24	17	408
									19	456
									21	504
	12		24	576		23	529		23	552
	13		26	624		25	575		25	600
	14		28	672		27	621		27	648
13		26			25			26	17	442
									19	494
									21	546
									23	598
	13		26	676		25	625		25	650
	14		28	728		27	675		27	702
14		28			27			28	17	476
									19	532
									21	588
									23	644
									25	700
	14		28	784		27	729		27	756



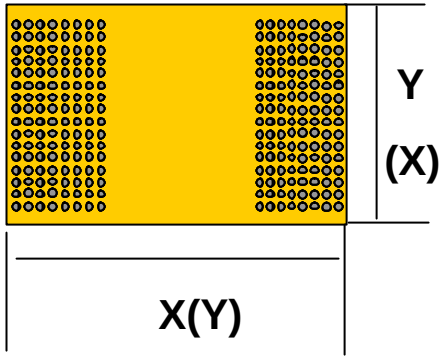
2-sided terminal



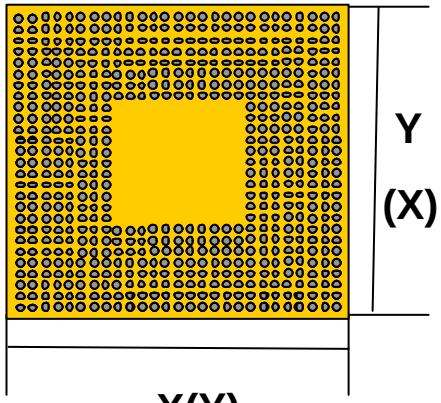
4-sided terminal

Proposed Terminal Count (0.65mm-P)

BODY SIZE		X,Y : Mmax+1			X,Y : Mmax			X: Mmax+1, Y: Mmax		
		MATRIX		MAX	MATRIX		MAX	MATRIX		MAX
X	Y	X	Y	PIN	X	Y	PIN	X	Y	PIN
9	9	14	14	196	13	13	169	14	13	182
	10		15	210		14	182		14	196
	11		17	238		16	208		16	224
	12		18	252		17	221		17	238
	13		20	280		19	247		19	266
	14		21	294		20	260		20	280
10		15			14			15	13	195
	10		15	225		14	196		14	210
	11		17	255		16	224		16	240
	12		18	270		17	238		17	255
	13		20	300		19	266		19	285
	14		21	315		20	280		20	300
11		17			16			17	13	221
									14	238
	11		17	289		16	256		16	272
	12		18	306		17	272		17	289
	13		20	340		19	304		19	323
	14		21	357		20	320		20	340
12		18			17			18	13	234
									14	252
									16	288
	12		18	324		17	289		17	306
	13		20	360		19	323		19	342
	14		21	378		20	340		20	360
13		20			19			20	13	260
									14	280
									16	320
									17	340
	13		20	400		19	361		19	380
	14		21	420		20	380		20	400
14		21			20			21	13	273
									14	294
									16	336
									17	357
									19	399
	14		21	441		20	400		20	420

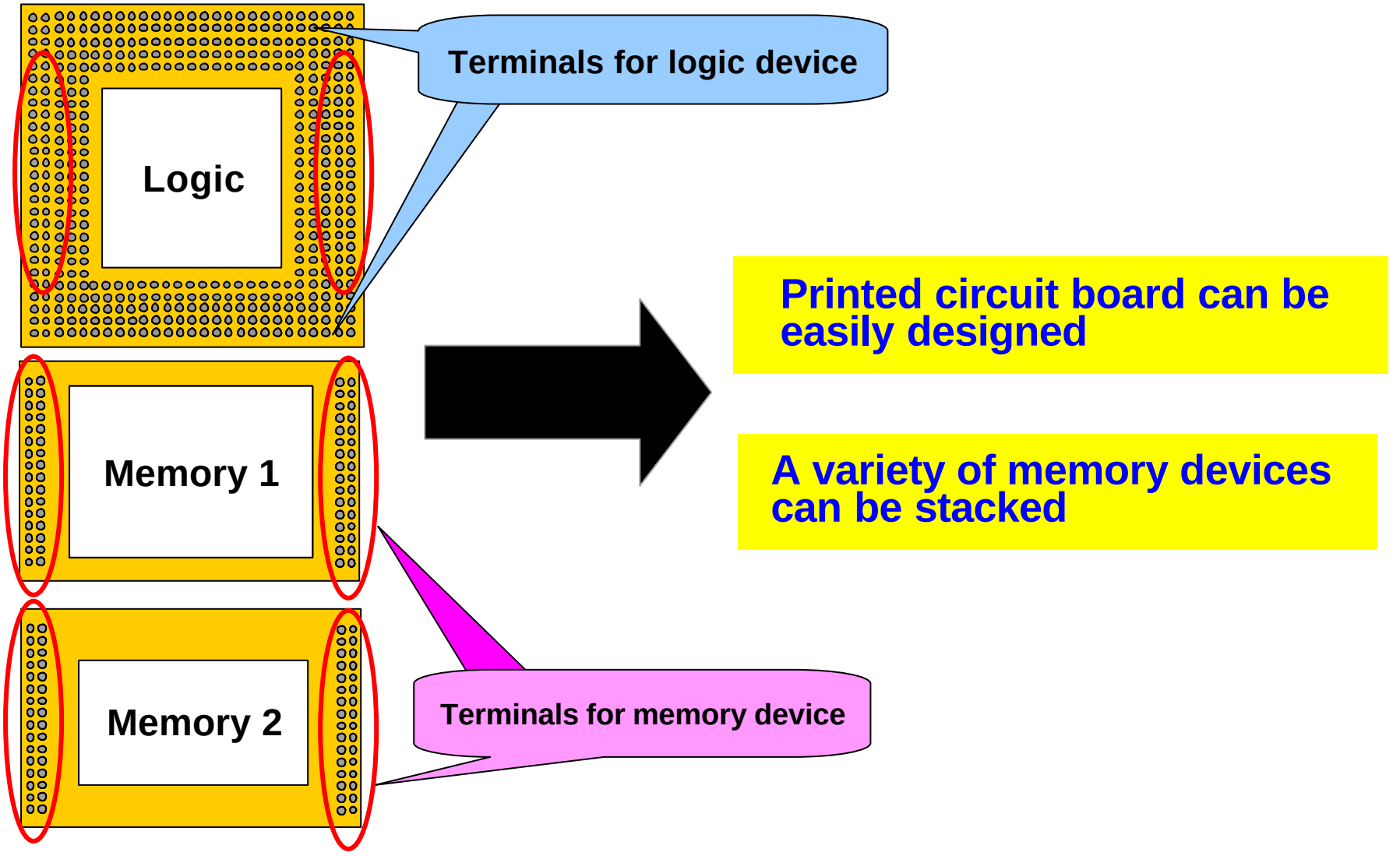


2-sided terminal



4-sided terminal

Recommended Memory Terminal Position for logic+memory 3D-SiP



Issues and Future Outlook for SiP

Business

1. *Applications must be extended (With usage limited to mobile phones the market will be unreliable. Applications must expand to include digital home appliances.)*
2. *Distribution and business models must be developed for silicon chips and IC devices (One company cannot supply a diverse range of memory, logic and analog devices. Overall responsibility must be determined.)*
3. *A profitable business model must be developed (1 + 1 = 2 + Premium price)*

Issues and Future Outlook for SiP

Technology

4. An optimal design for switching to 3D-SiP must be developed (Standardization of outline, pin out, I/O, etc.)

5. The design environment must be established (Electrical, thermal and physical, for uniform handling of chips, packages and mounting boards.)

6. Package technology must be advanced (Multi-layer stacking of chips, cost reduction, refinement, multi-layer metal board technology)

7. Test technology must be developed (KGD, testability, burn-in) 8. Reliability assurance must be established 9. Necessity for built-in passive components must be determined (Must components such as high-value capacitors remain?)

10. How to accommodate RF circuits must be determined