3-D Packaging:
Innovative Solutions for Multiple Die Applications

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Abstract
A vertically configured package technology developed by Tessera is proving to be a practical multi-die solution for any number of single and multiple functional combinations. The enabling technology for this stacking approach allows different sub-structures individually assembled, tested and joined together electrically and mechanically in a secondary process while still maintaining a small, single die footprint. This combining of several die sizes with varying functions within a single fine-pitch, low profile BGA package outline is achieved using thin flexible polyimide substrate as a base and adapting a unique combination of folding and package stacking methodology. In addition to the folded and stacked combinations, individual die can be configured for vertical stacking. In the case of memory for example, the single die can be packaged, tested, and marketed as unique sub-structures, allowing each die type to be sourced separately from multiple silicon vendors. This "layered" approach to packaging is designed to improve yield, resolve test concerns and overcome the business issues hindering the wide-scale adoption of multi-die solutions. The paper examines several alternative 3D multiple-die package solutions that solve many of the multiple die source problems while delivering the expected performance and cost benefits.

Introduction
With the advent of FBGA and die-size array package technology, the single die device package outline (often only slightly larger than the die) has played a major role in reducing product size. Newer generations of wireless hand-held portable electronics are furnishing a great deal more functionality than the preceding generations by combining two or more die functions within a single package outline. The multi-die packages initially adopted for these applications simply stacked one die on top of the other with adhesive in a pyramid fashion, using conventional wire-bond methodology for in-package electrical interface. When using multiples of the same size die in a stack, however, spacers must be added between each die to clear the bond loop. In either case, package yield can degrade to unacceptable levels because of the variation in die quality from multiple suppliers. To minimize risk, the idea of building up the multiple-die package sequentially becomes highly attractive. With the ultimate goal of combining several functions in a single package footprint still achievable, assembling and testing individual devices prior to final integration appears ideal.

Die Sourcing Concerns for Multiple-Die Packaging
Memory die, such as Flash and SRAM, have relatively high fabrication yields and some companies waive die level testing altogether, but even these devices are not immune to physical damage during assembly processing and handling. Combining memory and logic within the same package outline is appealing for a number of applications but, processors and ASIC yields are not always predictable and difficult to gauge. Combining these very different yielding products into the same finished package without thorough die-level pre-testing can subject the multiple die package to an unacceptable level of risk. Combining two or three mature die within a single package may provide a reasonable assembly process yield but as the die count increases, the ratio of failure probability increases as well.

Package Stacking Advantage
The primary issues associated with compound yield and test can be easily addressed by isolating specific functions into unique but joinable packages. For example, one package can contain the logic function; and the other, a memory device or other less complex function. By separating the devices into their own stand-alone package sections, testing can be more efficient and functional configuration control more flexible.

The package technology detailed in the following text is a package stacking concept that relies on a flexible polyimide film substrate base material with one and two metal circuit layers for intra-package termination. The package assembly process employs both folding and stacking methodology that allows the addition of various sub-structures to be mounted onto the base package while retaining a package footprint that is only slightly greater than the largest die in the set. The individual die or die sets can be packaged separately, electrically tested before joining, ensuring higher yield of the finished multiple die configuration. In addition, separating the package functions maximizes sourcing flexibility, allowing users to procure combinations of pre-tested product from multiple silicon vendors.

μZ™ Fold-Over Stacked Package Methodology

Through a process of folding and joining of two or more packaged and pre-tested parts, the final stacked package configuration becomes a single, high yielding multiple-function component. If the decision is to join package sections at the board-level assembly, the base fold-over package can be placed onto the board and the memory or other packaged die can be placed sequentially onto the mating contact matrix of the base for simultaneous reflow soldering. This alternative has two benefits. It allows the user configuration flexibility, for example, in selecting different memory functions, data rate and so on, as well as accommodating secondary sources of supply. Furthermore, by providing the compatible interface on the topside of the logic package, commercially available memory or other products can be soldered directly to base package. That is, the fold-over extension of the package can be configured to accept any number of fine-pitch array package types.

Several scenarios can be considered for the upper section of the μZ package, maximizing product configuration options. The two sections can be supplied as separate units and joined together at the board level assembly stage or furnished as a single package level product, tested and ready for PCB mounting as illustrated in Figure 1.

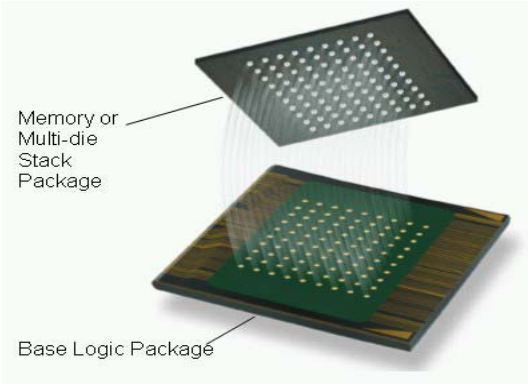


Figure 1 - μZ Fold-Over and Stacked Package Enables Board Level Sequential Assembly of Components Supplied from Multiple Sources

Whether or not to join one package to the other before or during the board level assembly process is a decision that may be influenced by the requirement for in-process configuration flexibility. For example, the base fold-over package maybe furnished by vendor 'A' while the memory sections of the stack supplied by vendor 'B', 'C' or 'D'. After all, memory functions are available from a greater number of sources and the testing for memory is somewhat specialized. The handling and testing of the base or logic portion of the package may require more dedicated fixturing, software and system support. Furthermore, the concern of ownership of total quality and reliability can be alleviated. The logic device supplier is responsible for the logic, the memory manufacturers are responsible for the respective memory, and the board assembler is responsible for only the surface mount attachment of the two.

Fold-Over Package Substrate Development

The substrate developed for the μZ folded-over base package uses a high-grade polyimide film as its dielectric foundation. For electrical interconnect it relies on a pattern of narrow gold plated copper-core conductors for the interface (through gold wire) between the aluminum bond site on the die, the interconnection between die and ultimately, the contact (solder ball) array needed for the circuit board attachment. The actual interface between die sets will typically require two circuit layers to provide for higher wiring density. The two metal layer fabrication process adopted for the μZ package substrate enables very narrow circuit routing features and provides optimized in-package interconnect.

The Tessera design engineering team (working closely with an independent substrate supplier and the company's in-house assembly process development specialists) has designed a substrate that can be fabricated in either a panel format or tape-and-reel. The substrate material for the fold-over base 'test vehicle' package adapts a 50μm thick, adhesivless copper clad high-grade polyimide film and a non-functional die to physically replicate a typical proprietary logic die.

During the substrate design process the in-package circuit routing is refined and modeled to verify that the package, when fabricated, will meet the performance and reliability expectations required for complex applications (see sectional view in Figure 2).

Because each device area is often relatively small, multiple unit arrays can be closely clustered on the flex-tape material. The substrate design is configured for ease of handling and to be compatible with existing package assembly systems.

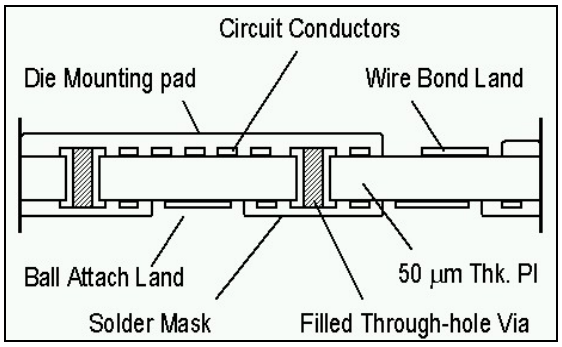


Figure 2 - The Substrate is Supplied with Copper Circuits on Both Surfaces of the Polyimide Film and Inter-connected with Plated and Filled Micro-vias

Micro-via Ablation and Plating

Because of the minimal surface area of the substrate, the inter-package circuit design requires adapting very small via pads, holes and narrow circuit conductor features. The via holes, for example, are only 125μm in diameter and 25μm to 35μm wide conductors are the rule for most applications. Although both sides of the substrate are utilized for interconnect, the circuit path between die and the array patterns are routed on the inside surface of the flex material. With the exception of the 'fold zone' on the substrate, the circuit pattern remaining on the outer surface is coated with a photo-imaged dielectric mask material specially formulated for flexible applications.

μZ Fold-Over Base Package Assembly

The substrate design typically accommodates several die arranged in a side-by-side or array format. Device sets can then be simultaneously processed using conventional assembly systems for die-attach, wire-bond and a series of sequential process steps. The following (illustrated in Figure 3) describes the package assembly process for a single die fold-over logic package that when completed, provides a mounting site for an additional package on its top surface.

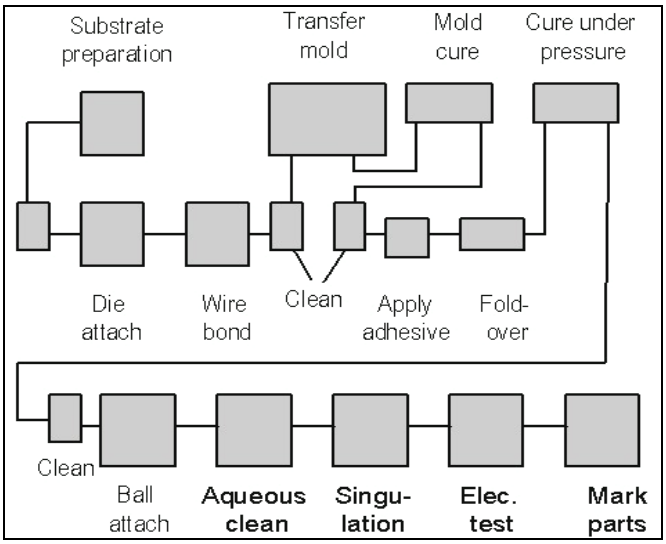


Figure 3 - Assembly Process Sequence for the μZ Fold-Over Base Package

In preparation for package assembly, the 48mm x 100mm flex-tape panel substrate is mounted to a universal rigid carrier-frame. The carrier-frame format allows the efficient in-line machine-to-machine transfer as well as enabling batch processing for cleaning and curing operations. The carrier-frame developed for the μZ fold-over assembly process is also compatible with commercial magazine systems and provides a secure and efficient method of transfer between subsequent stages in the process.

Die Attach, Wire Bond and Encapsulation

Prior to die attachment and wire-bonding operations, an adhesive pattern is applied to the substrate surface. This adhesive can be dispensed as a liquid, pattern printed or, pre-applied to the substrate as a die cut dry film composite. The silicon die is aligned and placed onto the prepared site followed by a short cure cycle. After curing the die-attach material the substrate

carrier is transferred to the wire-bond system to complete the electrical interface between die and substrate. A combination of wedge and ball bonding methods are employed to complete this process (Wire bonding remains the industry's preferred method for die-to-substrate interconnect, accounting for over 90% of bonds worldwide).

Limiting the wire loop height is vital to maintaining a lower package profile. The gold wires are sequentially bonded from the gold plated copper pad on the substrate to the aluminum bond pads on the die. The relatively low (7.5µm) loop height must be maintained in order to provide the thin encapsulated package height requirement established (see Figure 4).

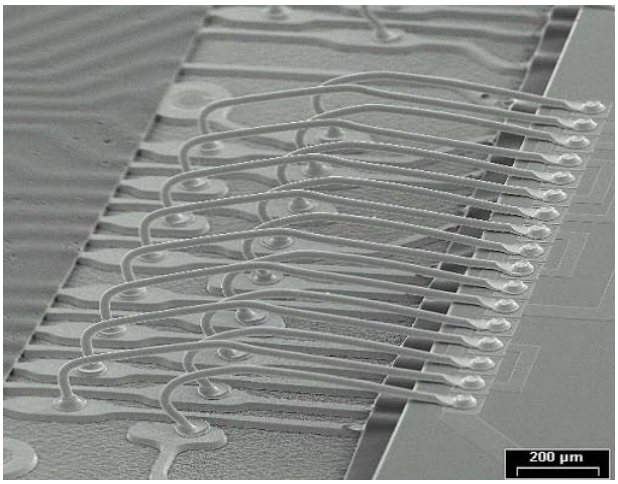


Figure 4 - A Lower Loop Height was Successfully Achieved by Adapting a Reverse-wire-bond Process

The attachment and wire-bond sequence completed, the assembled carrier-frame is inspected and transferred to the encapsulation stage. The substrate for the fold-over base package positions six die in two parallel rows allowing the encapsulation of two die per mold cavity. The encapsulation for the base assembly utilizes a preformed epoxy composition pellet that, when heated to a liquid, is transferred under pressure through gate channels into each of three, two die mold cavities.

Fold-Over Process

The final configuration of the base section is accomplished through a sequence that applies an adhesive composition to the top surface of the molding compound and precise mechanical folding. Figure 5 illustrates the folding sequence for the base package section.

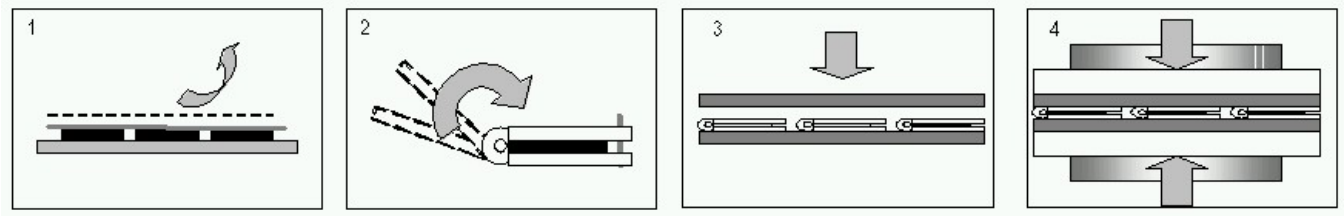


Figure 5 - The Fold-over Process Includes an Adhesive Application, Folding and a Simultaneous Temperature and Pressure Cure Cycle

When the bonding material completes its curing cycle, the finished base package is ready for ball contact attachment, singulation and electrical testing using test sockets developed for accessing two sides of the base package.

Ball Attachment, Singulation

Although several alloy compositions can be considered for the solder ball contacts, the standard package is furnished with either a eutectic (Sn/Pb) alloy or lead-free Sn/Ag/Cu alloy (which is typically preferred for consumer applications). In preparation for solder ball attachment on the base section of the package, flux is applied to each solder ball contact site on the package substrate with a pattern printing process. Using a precise template fixture, discrete solder balls are deposited in mass onto the flux and transferred to a surface conduction heating process to complete the ball-to-package joining process. Following cleaning and physical inspection of the solder ball process the packaged units are ready for singulation.

Singulation of the six packaged devices from the strip is very precise. For this application a precision saw proved efficient for cutting through the substrate and mold material. Both sawing and laser ablation are viable methods for package singulation, requiring minimal dedicated tooling and each can be programmed to accommodate several package outline variations.

Conclusion

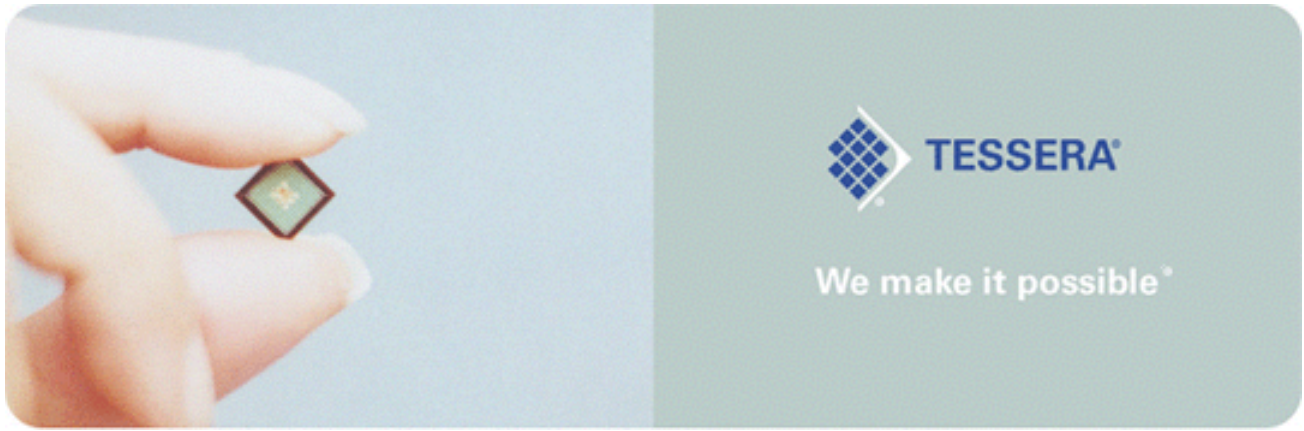
The μZ multi-chip package is proving to a cost-effective 3D package solution for a number of real and practical applications allowing optimization of individual die function, greater design flexibility, reducing risk and time-to-market.

Unlike some of the earlier over-molded multiple die, wire-bond packaging techniques, no new assembly lines are required for adapting the methodology and the assembly process yield is excellent. With minimal investment by the OEM or the user, the established μBGA® assembly infrastructure can quickly initiate the μZ multi-chip package technology.

References

1. Francis, David, "Thinning Wafers for Flip Chip Applications", High Density Interconnect, vol. 2 No. 5, pp 18-21.
2. Kim, Young-Gon et al., "μBGA Design and Reliability", SEMICON Singapore 1999, Technical Symposium, International Packaging Symposium (IPSS), pp. 57–75, May 4, 1999.
3. Jim Rates, Overcoming Technical and Business Issues Associated with System in Package Adoption, Proceedings of the IPC Annual Meeting 2002.
4. Nachon, Beni, "Basics of Ball Bonding", an application note available from Kulicke & Soffa.

IPC Annual Meeting, SO6 Exotic Interconnections Session
Minneapolis Convention Center - October 1, 2003, Minneapolis, Minnesota



3-D Packaging: Innovative Solutions for Multiple Die Applications

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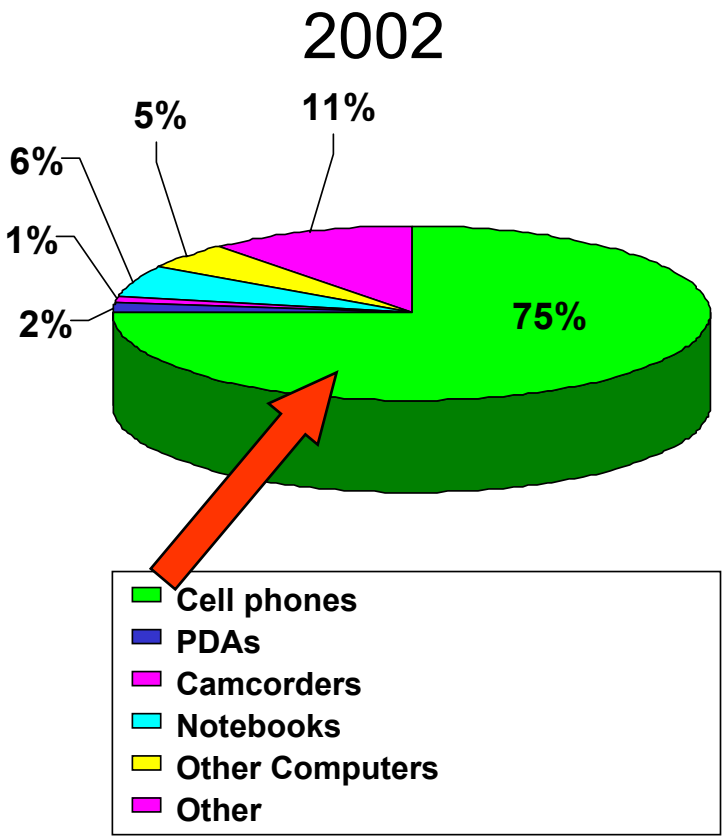
Topics of Discussion

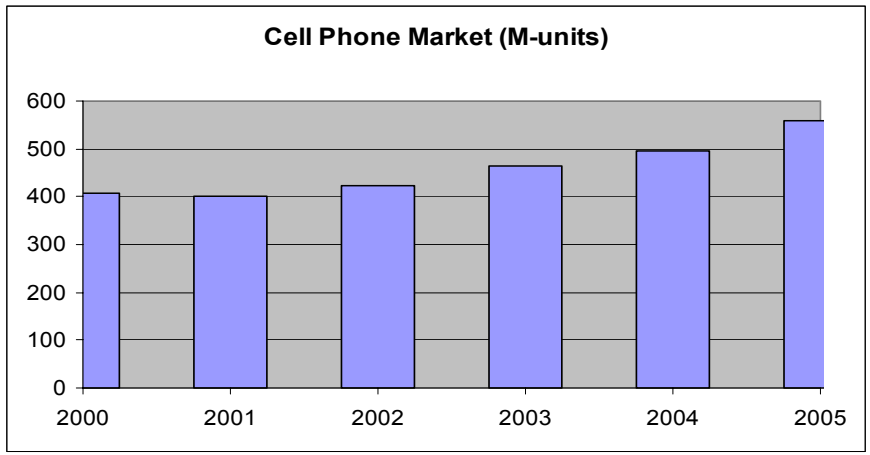
- Market for Stacked Multiple Die Packaging
- Multiple Die Package Innovations
- Test Vehicle Design and Development
- Two Metal Layer Flex Substrate Fabrication
- µZ™ Fold-Over Package Assembly

Consumer Product Trends…

- Smaller
- Lighter
- Greater Reliability
- Feature Rich
  - PDA
  - MP3
  - GPS
  - Multimedia Messaging
  - Digital Still and Video Camera
  - Video Streaming

Application for Multi-Chip Packages





Cell phone continues to be key driver of advanced packaging

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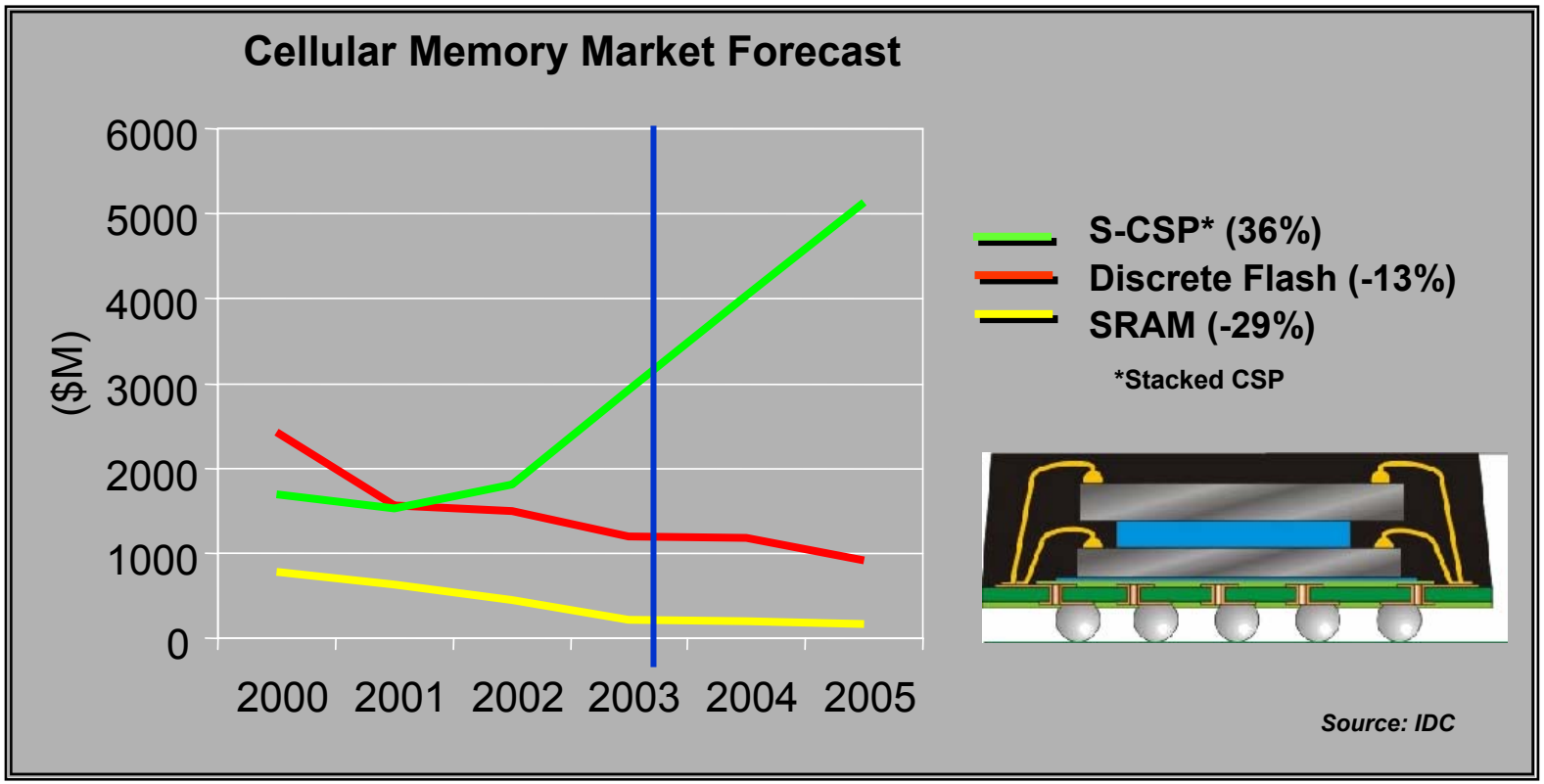
Multi-Chip Package Momentum



- Stacked CSP expected to account for 83% of entire handset memory market by 2005
- Next area of integration is Logic + Memory

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3D Packaging Issues

- Managing multiple IC vendors
- Known good die, test and burn-in
- Die and wafer availability
- Compound yield
- Overall product quality and reliability
- Accommodating incompatible die shrinks

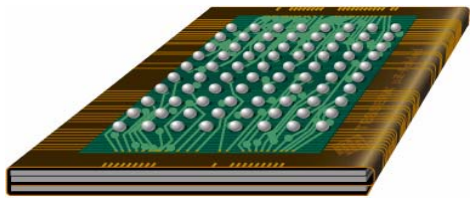
These issues must be resolved to move beyond Flash + SRAM stack!

Benefits of 3D Multiple Die Packaging

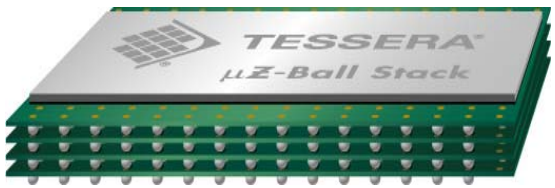
- **Increased Density**
  - Miniaturization of electronic products (size and weight)
- **Increased Functionality**
  - More functionality within same footprint
  - Integration of various device types

Tessera's µZ™ Multi-Chip Package Solutions

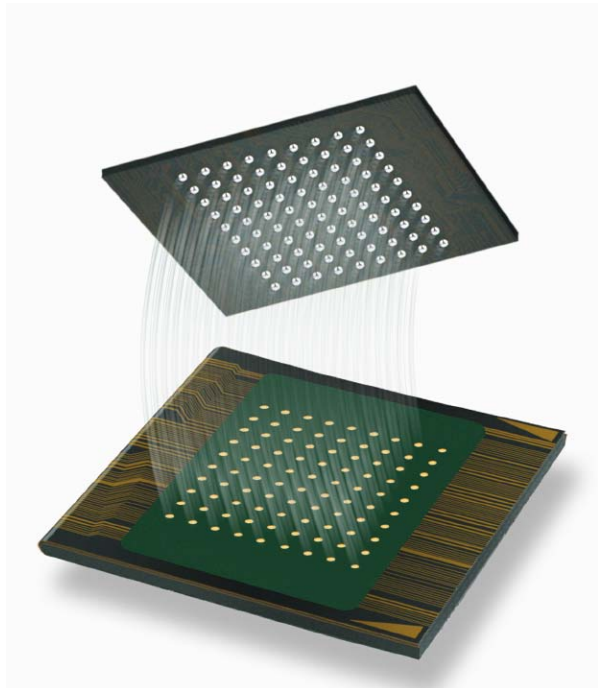
Multi-chip solutions developed specifically to address current business and logistics issues



Folded Package

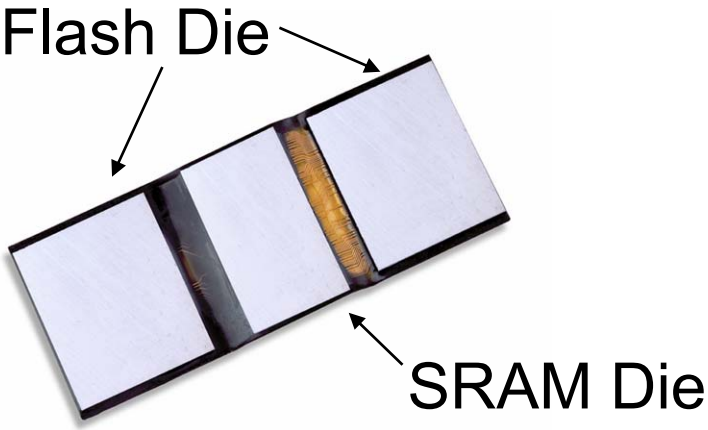


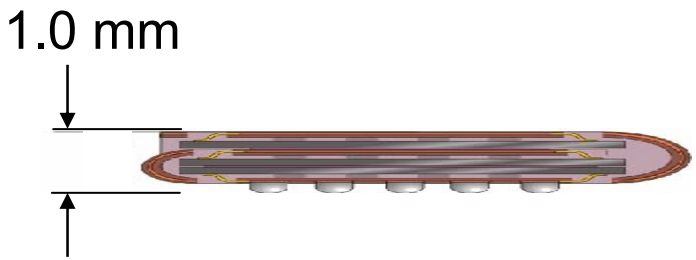
Ball Stack Package

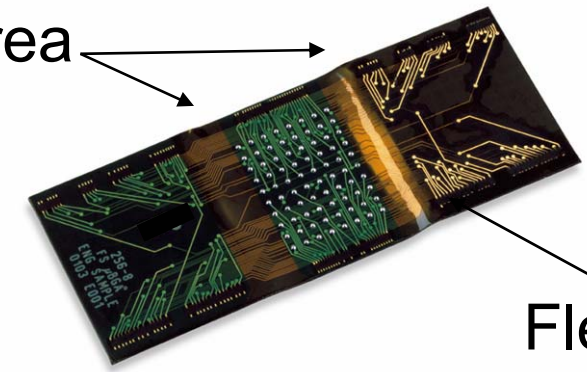


Fold-Over and Stack Package

3 Die µZ™ Folded Package







300 µm solder balls
on 0.75 mm pitch

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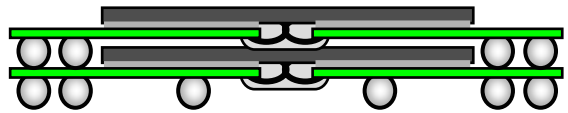
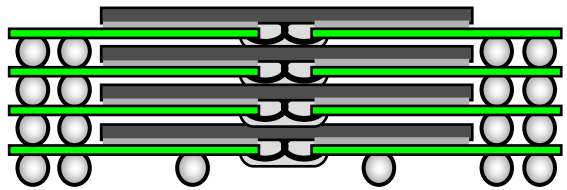
2 and 4 Die µZ™ Ball Stack Package

2 Die DRAM Ball Stack

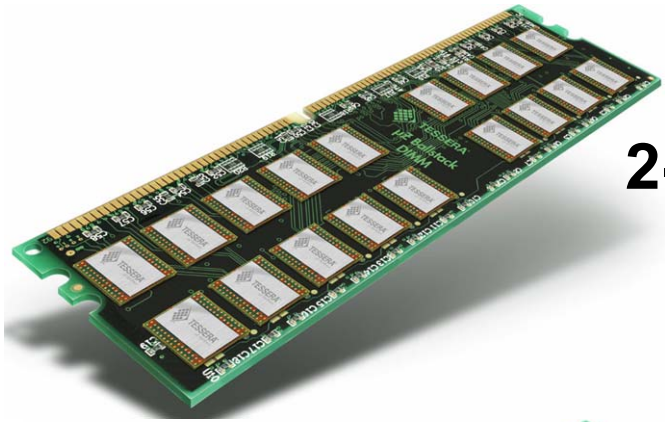


4 Die DRAM Ball Stack



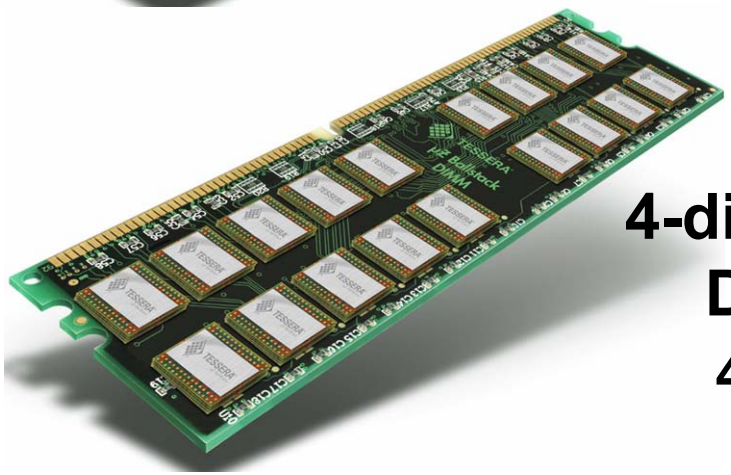
Enables the stacking pre - tested packages

µZ™-Ball Stack on DIMM and SO-DIMM



2-die stack DIMM
2GB *

2-die stack SO-DIMM
1GB *

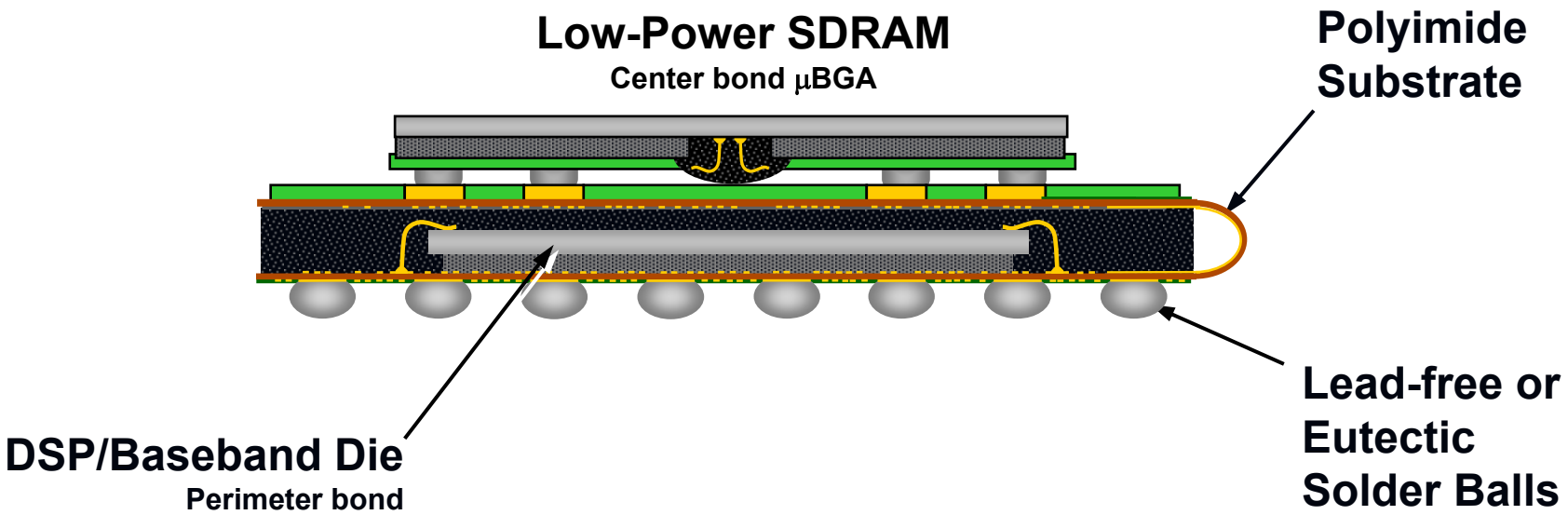


4-die stack DIMM
4GB *

4-die stack SO-DIMM
2GB *

*** Based on using 256M DDR SDRAMS**

µZ™ Fold-Over Package Logic + Memory



Single-die Fold-Over on bottom (DSP/baseband)
Single SDRAM on top

1.2mm max. height

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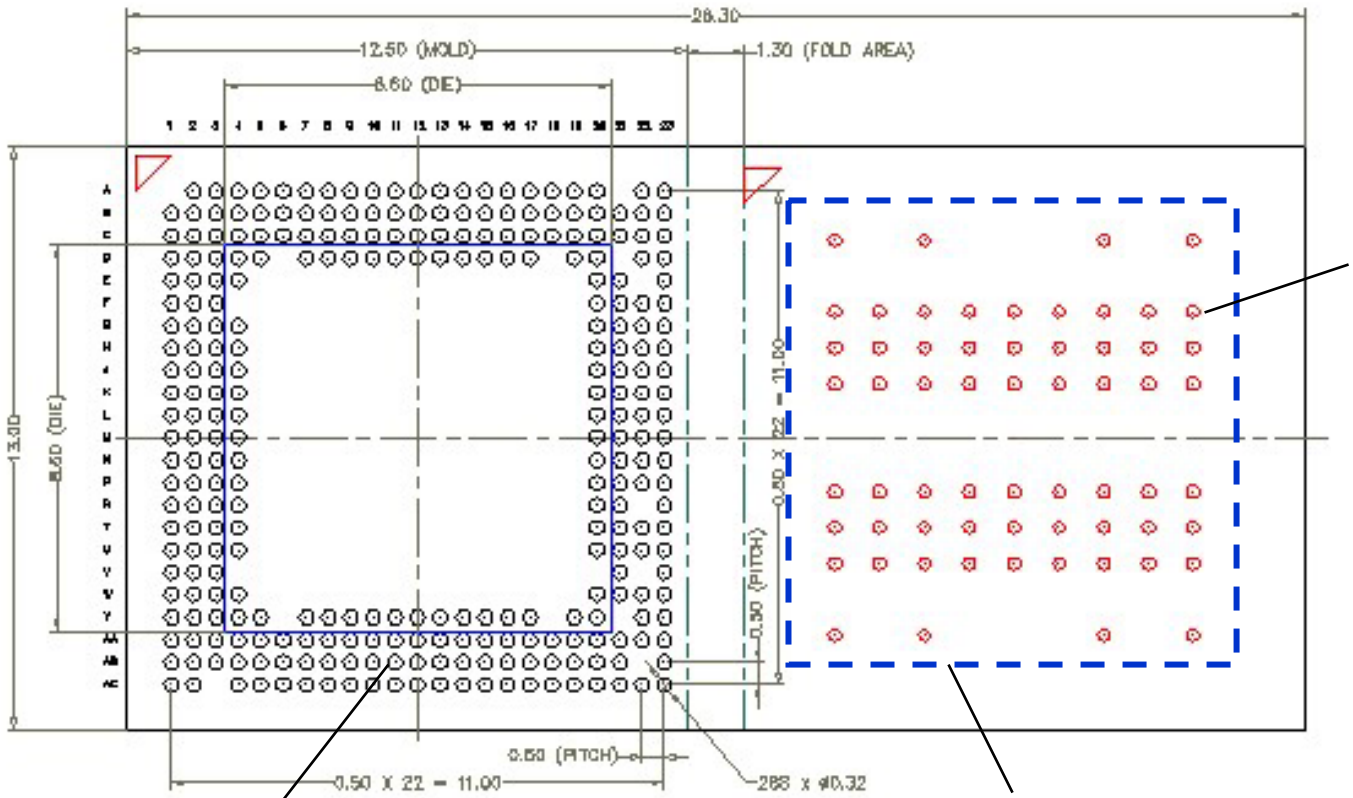
Package Stacking Addresses Key Issues

- ✓ Accommodates incompatible die shrinks
- ✓ Simplifies management of multiple IC vendors
- ✓ Enables package level test and burn-in
- ✓ Allows the combining of high and low yield devices
- ✓ Contributes to product quality and reliability
- ✓ Maximizes configuration flexibility

Tessera's TVM-288F Test Vehicle



0.80 x 1.0 mm
ball pitch
(on top surface)

0.50 mm ball pitch
(bottom surface)

This test vehicle is designed to support DRAM, RDRAM, SDRAM, DDR, Flash and SRAM devices.

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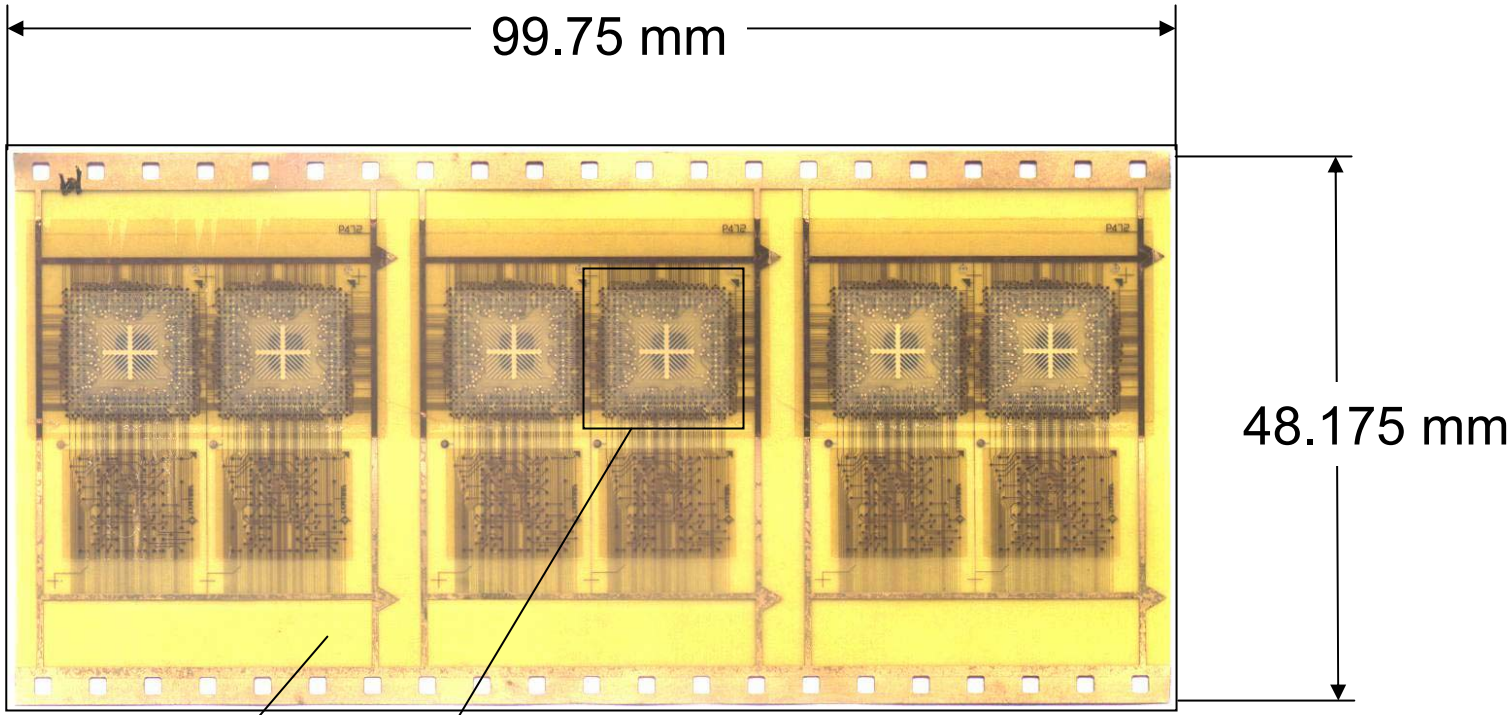
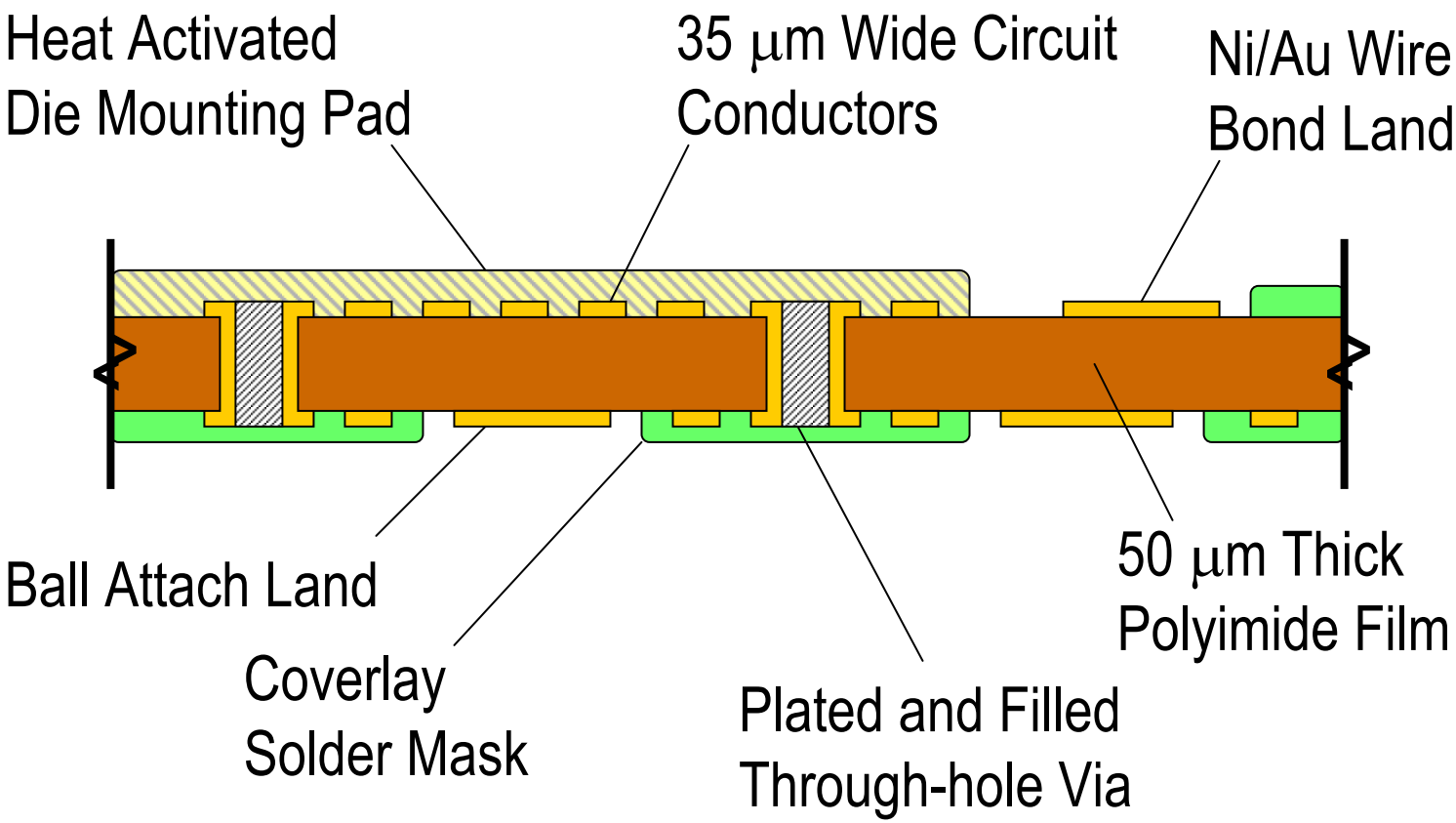
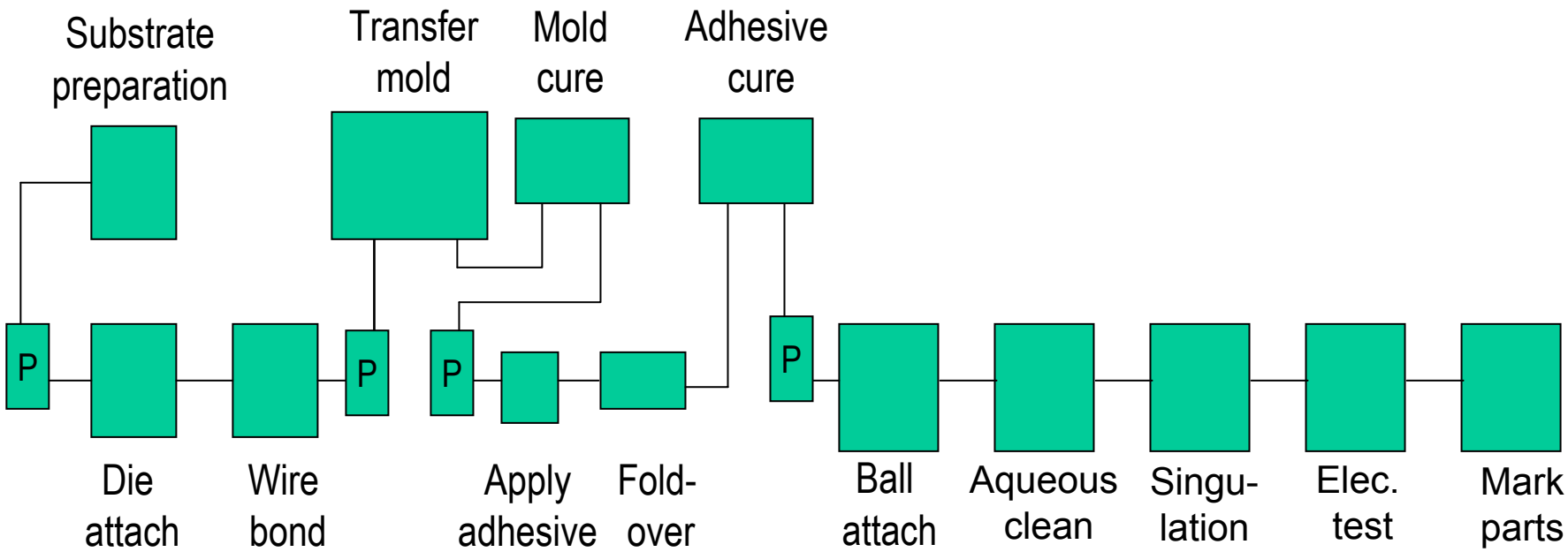
Two Metal Layer Flex Substrate



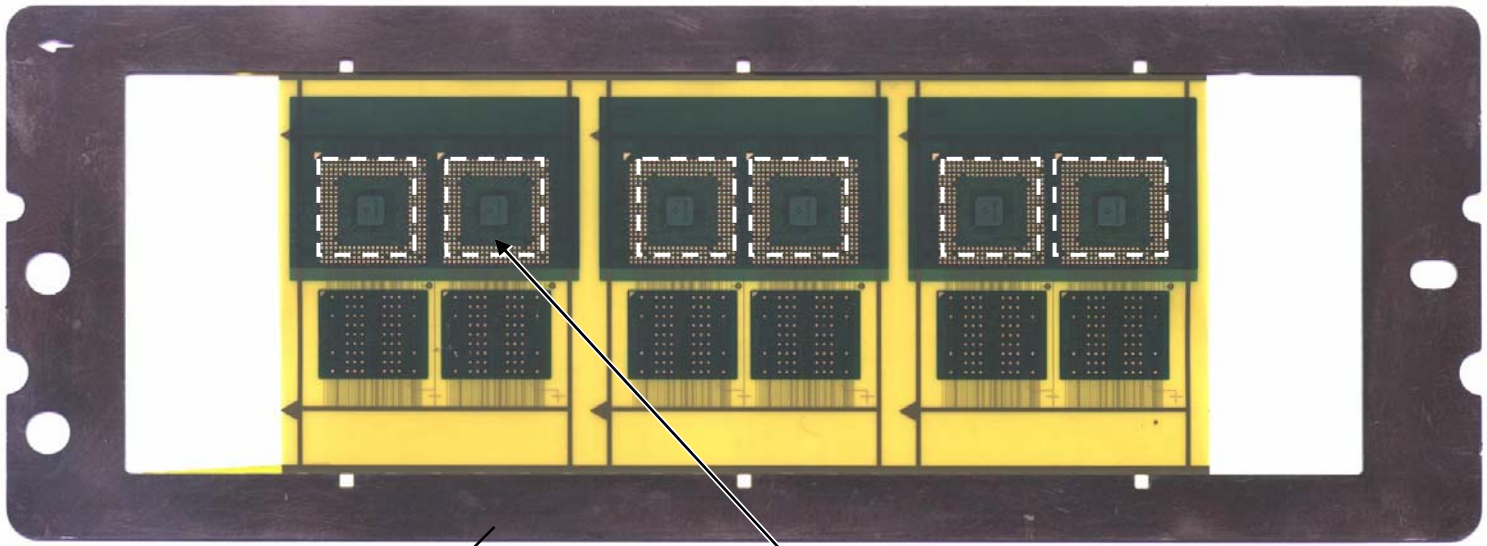
Substrate X-Section Detail



μZ™ Fold-Over Package Assembly Sequence



Package Substrate Mounting



Universal Carrier Frame

Heat Activated Die Attach Pad

Substrate Detail for Wire-Bond

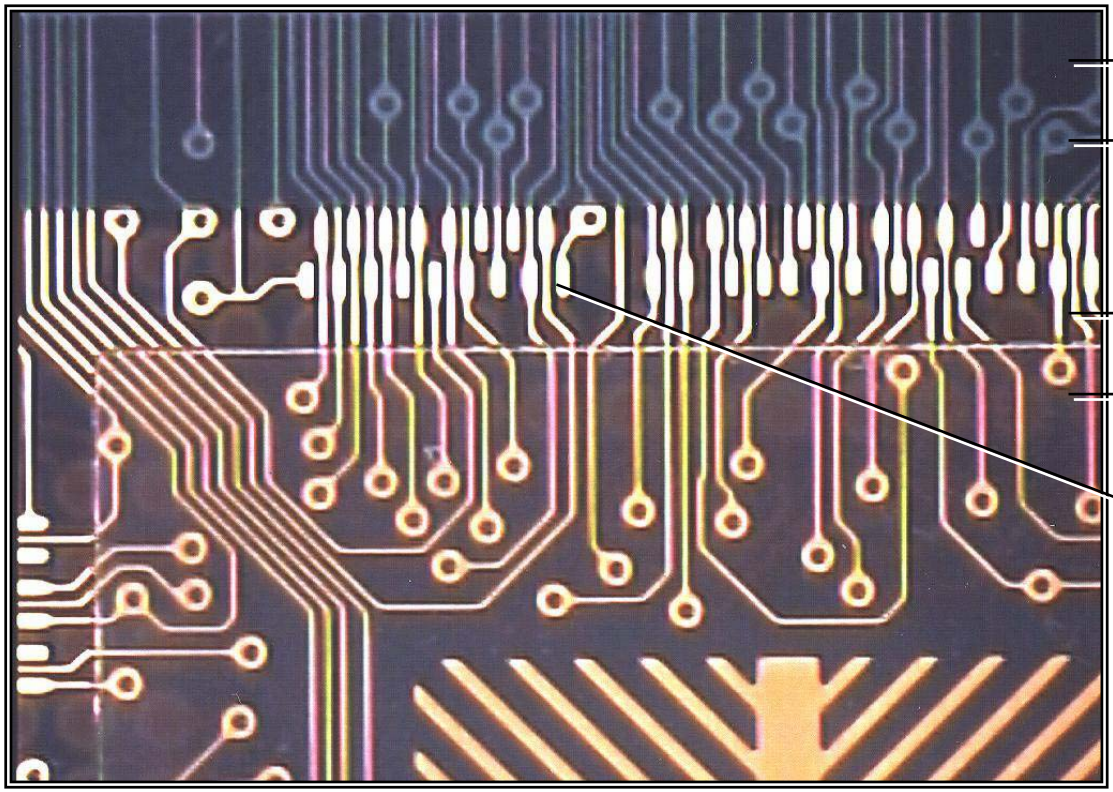
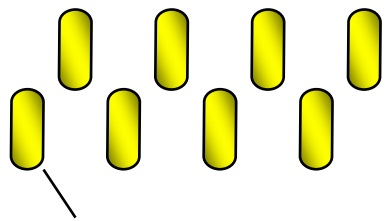


Photo-imaged cover lay

Plated and plugged via

35 μm wide circuit trace

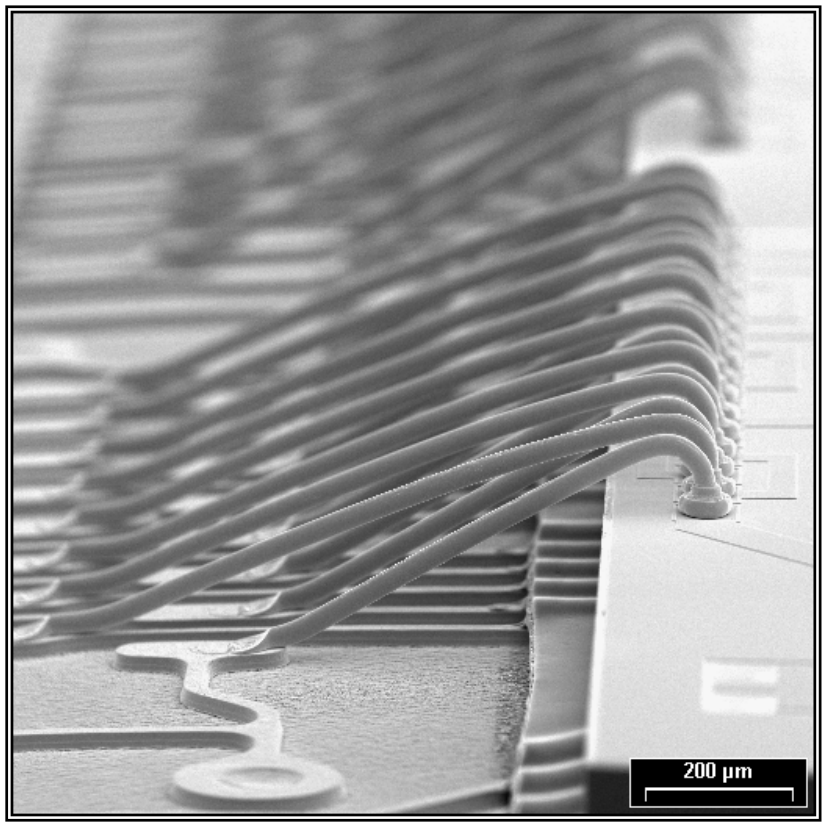
Die Attach Adhesive

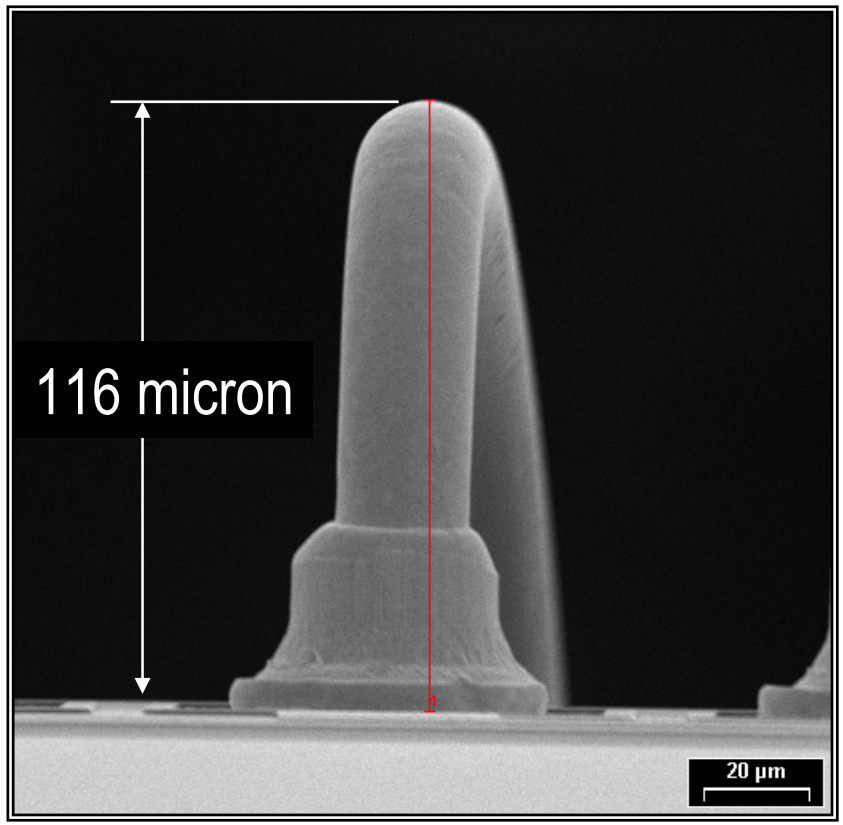


0.10 mm x 0.25 mm

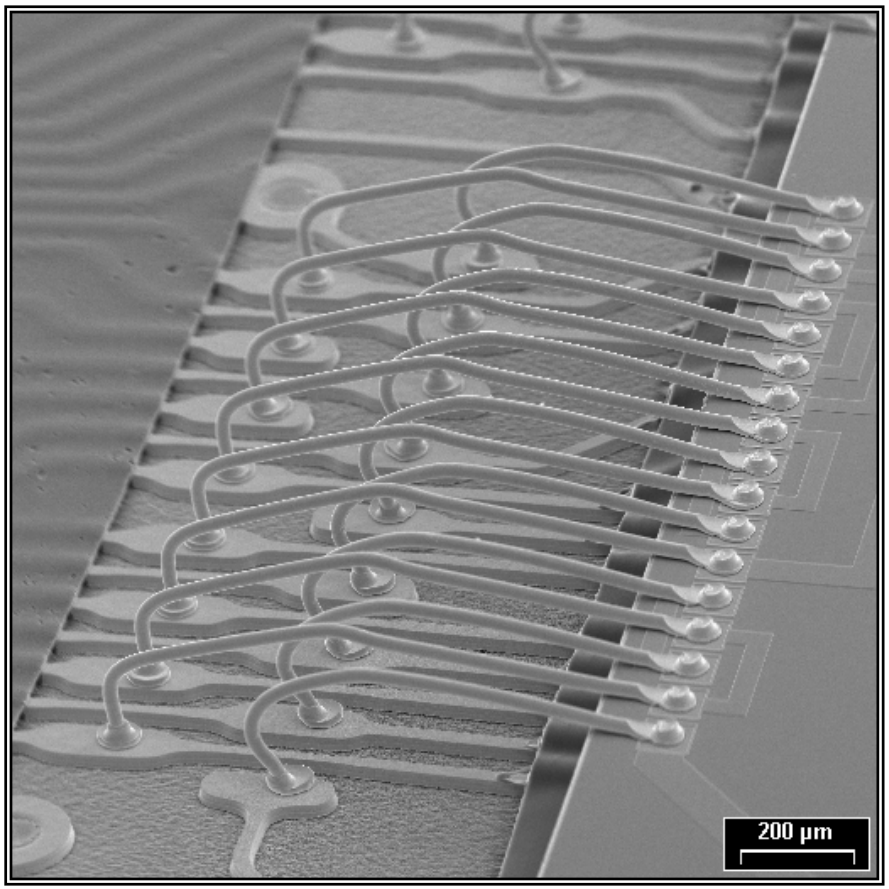
Staggered wire-bond pad

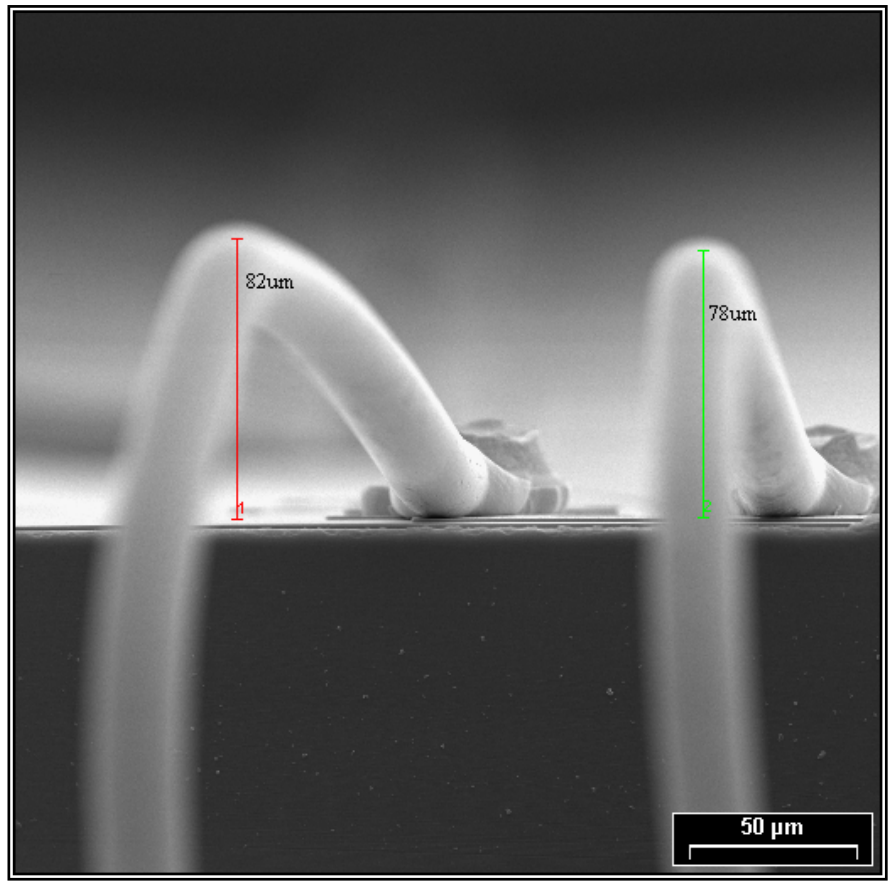
Standard Die-to-Board Wire-Bond





Low Profile Reverse Wire-Bond





Reduced loop height to 75 - 80 micron

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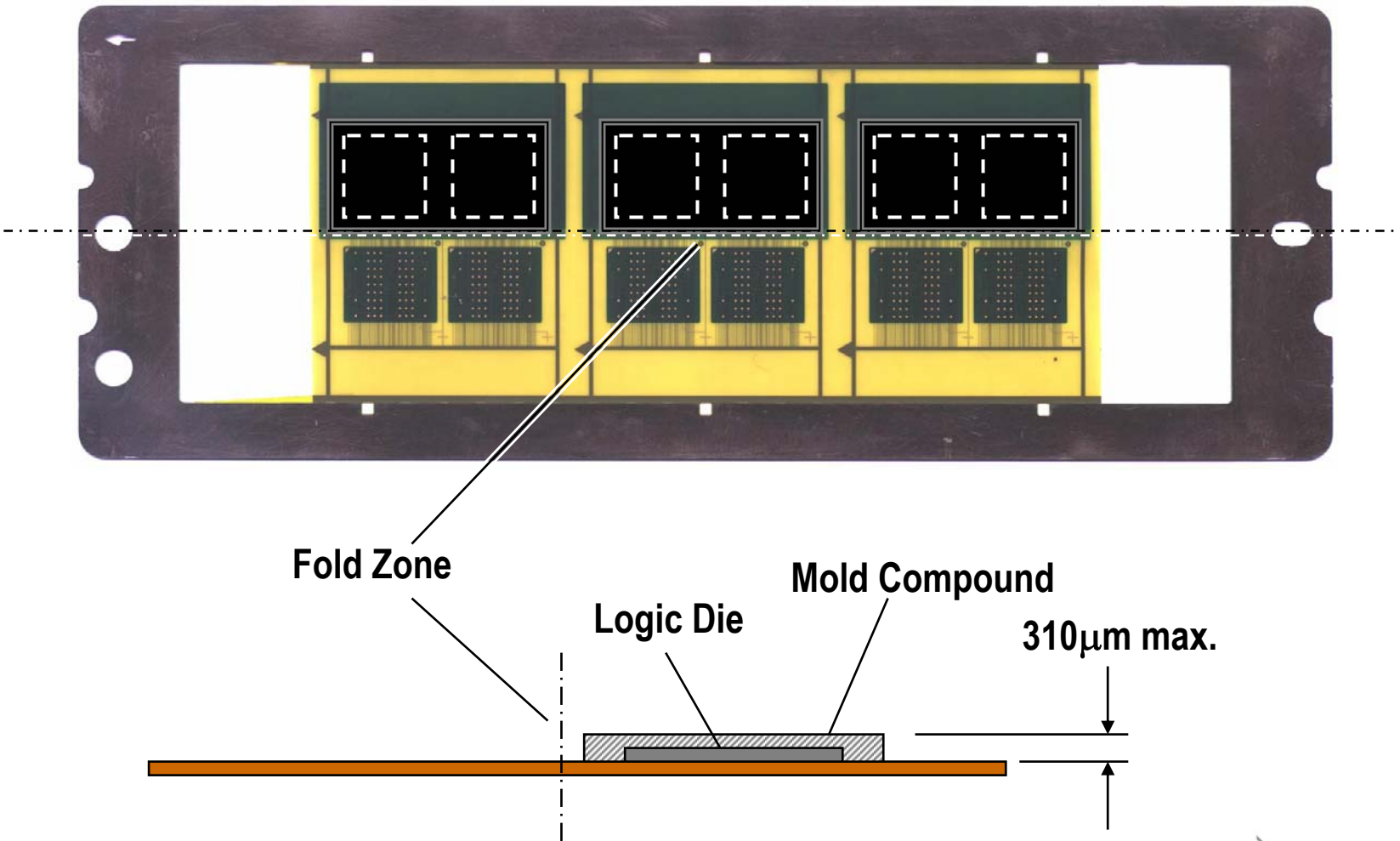
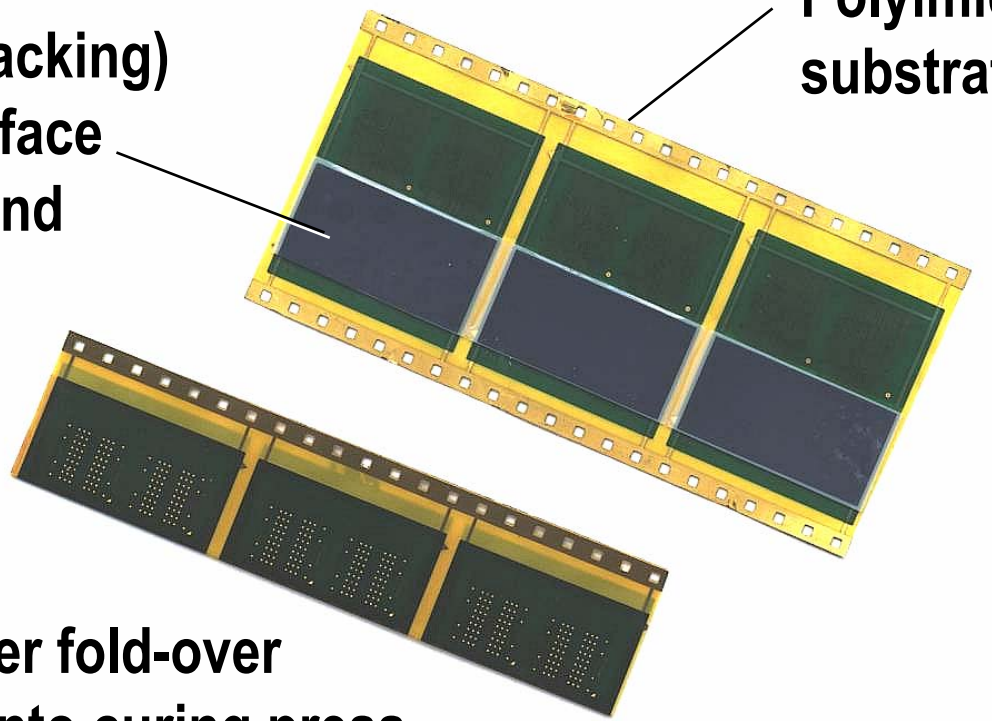
Transfer Mold Die Encapsulation



μZ™ Substrate
Before and After Fold Process

Adhesive film
(with low-tack backing)
applied over surface
of mold compound

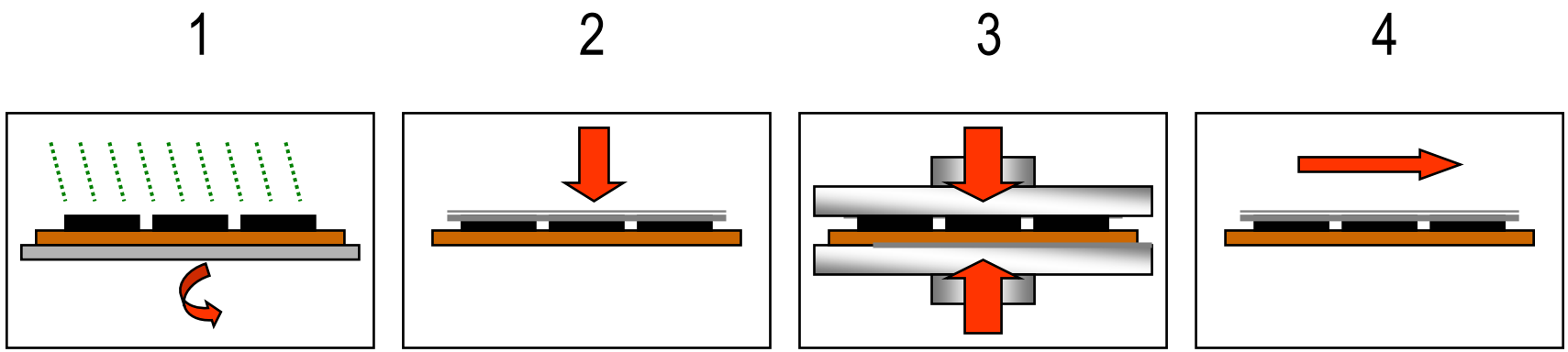
Polyimide based
substrate



Substrate after fold-over
For transfer into curing press

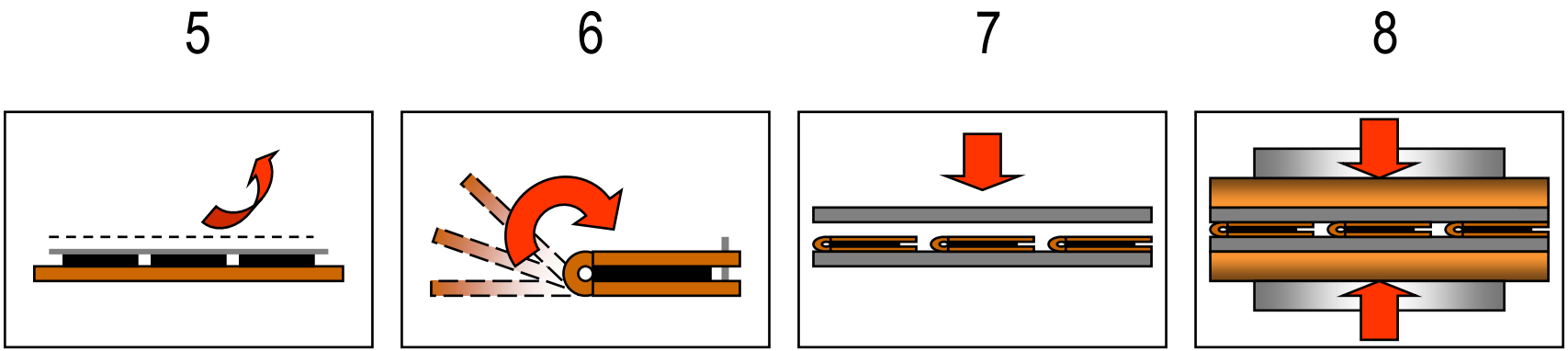
TESSERA®

Adhesive Film Application Detail



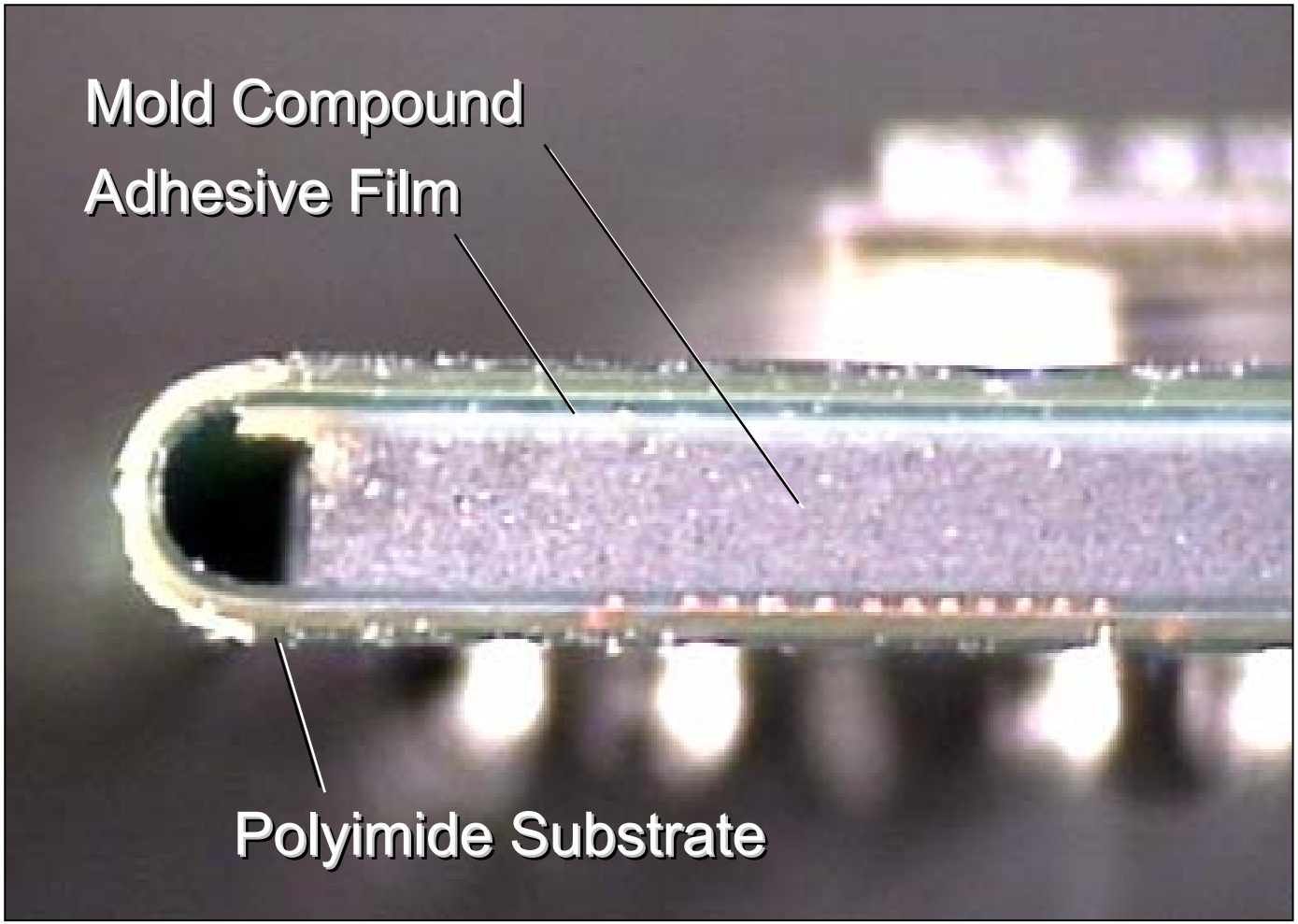
1. Plasma clean top surface
2. Position substrate, apply dry film adhesive
3. Transfer to heated press fixture and cure
4. Transfer to fold fixture

Fold and Bond Process Detail



5. Remove low-tack backing from adhesive.
6. Fold flex-tape extension over mold area.
7. Transfer folded units to heated press fixture.
8. Hold in press fixture under pressure to cure.

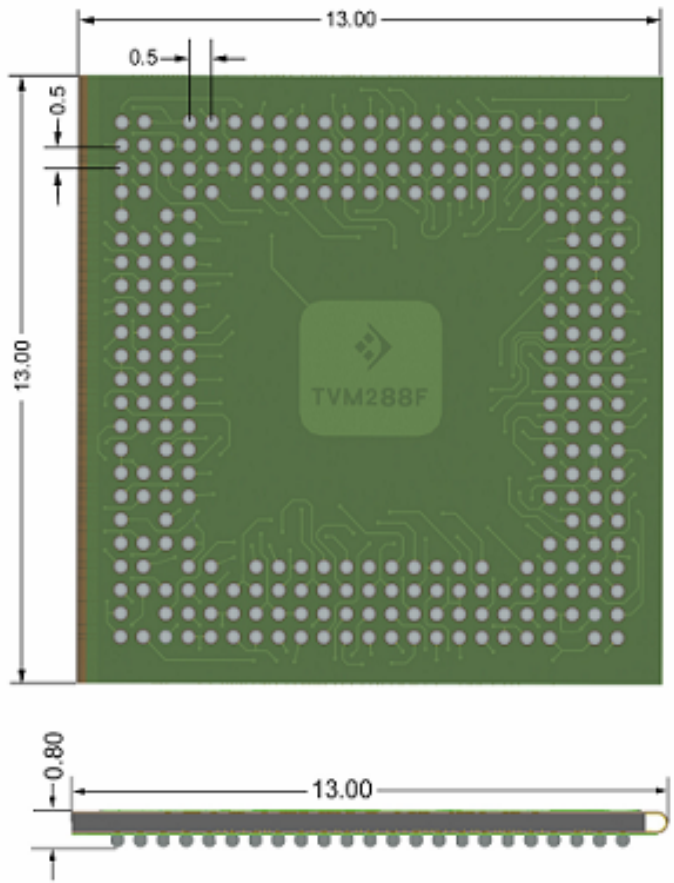
Post Cure View of Fold

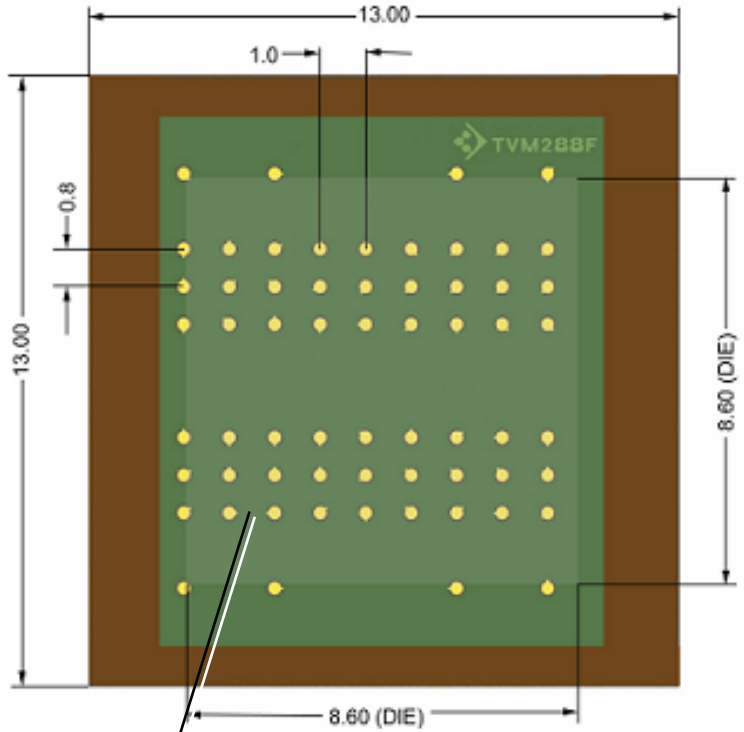


Ball Attach Process Detail

6. Print flux on ball attach sites
7. Place solder balls, reflow and clean

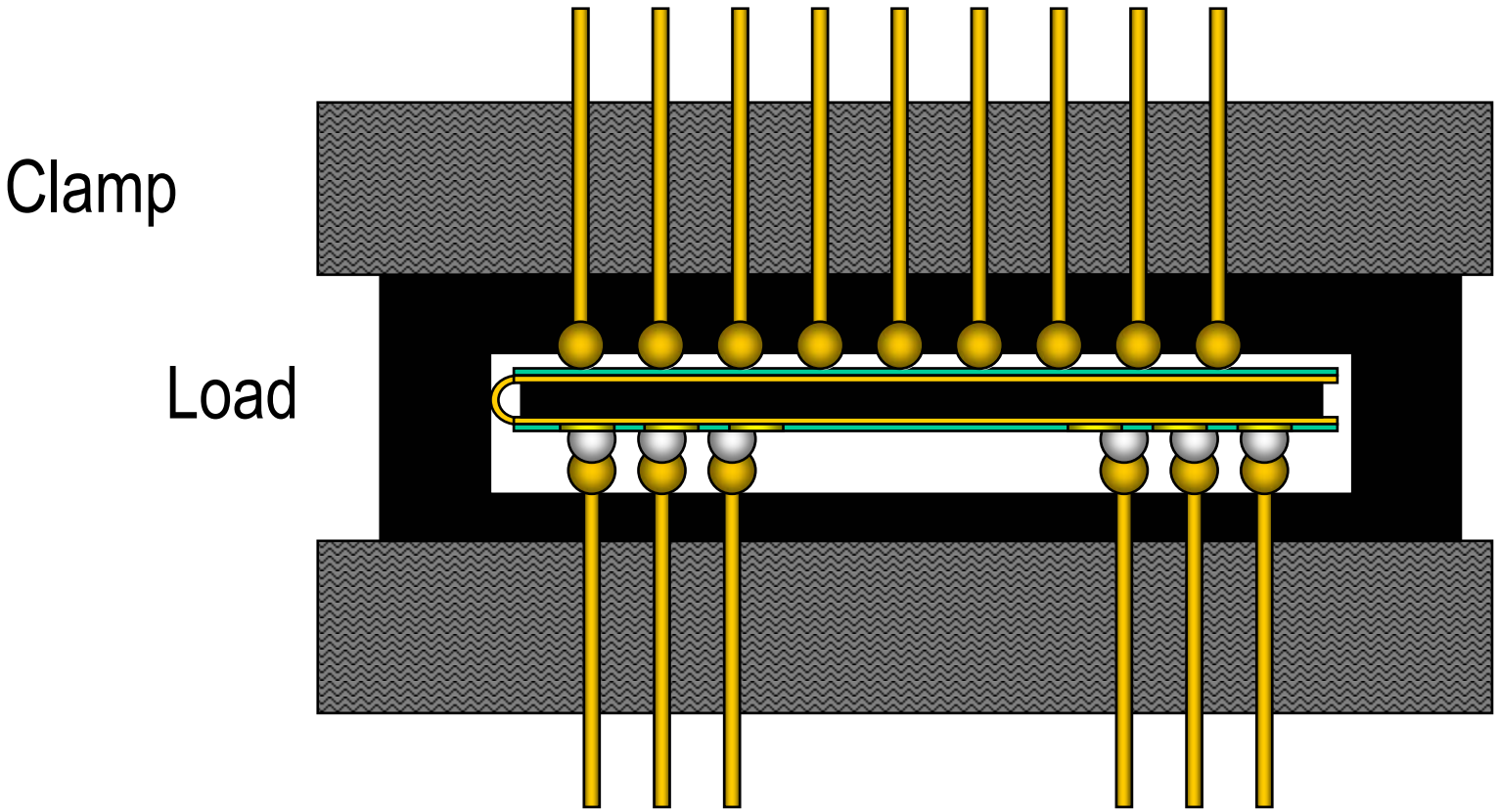
Finished Fold-Over Package Dimensions





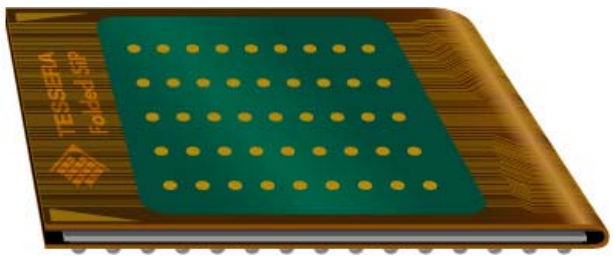
Land pattern site for standard DRAM memory package attachment

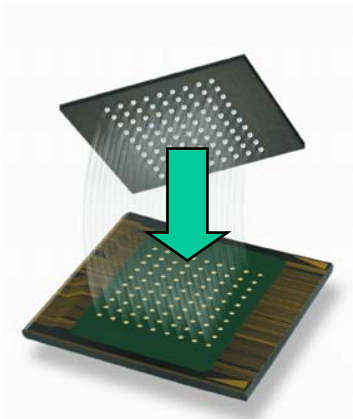
Electrical Test



Transfer individual package to electrical test

Final Configuration Flexibility





Universal interface enables…

- Multiple silicon sources for the top package.
- Efficient mix-and-match of commodity components.
- Utilization of existing SMT infrastructure to ensure supply.
- Final integration can be provided by either package or board assembler …

allowing potential for cost reduction and logistics simplification!

Conclusion

- µZ Multi-Chip Package Technology is proving to be an excellent, cost-effective 3D package solution for a number of practical applications.
- The fold-over and stack package allows optimization of individual die function and greater design flexibility, reducing both risk and time-to-market.

Risk is further reduced because the individually packaged sections are pre-tested by the supplier, assuring maximum yield at assembly.

Current suppliers of µBGA® Package Technology

Semiconductor Mfrs.

Intel Corporation
Samsung Electronics
Sharp Corporation
LG Micron
Advanced Micro Devices
Hitachi, Ltd.
Hynix Semiconductor
ROHM Corporation
Siemens AG
Sony Corporation
ST Microelectronics
Toshiba
Texas Instruments

Package Assembly

Amkor/Anam
Advanced Semiconductor Engineering
ChipMOS
ChipPAC
EEMS
Hitachi Cable
IPAC
Meicer
Mitsui Hightec
OSE
Plexus
Payton Technology
Shinko Electric
Siliconware Precision (SPIL)
United Test Center (UTC)
Walton Advanced Electronics, Ltd