# The Effect of Via-in-Pad Via-Fill on Solder Joint Void Formation

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**Abstract**
Fabricators, and the copper plating process they choose, can have considerable influence on their customers' solder joint reliability. In the case of high density assemblies, via-in-pad designs often cause solder joint void formation due to the trapping of air and/or other contaminants. If large enough, these voids can compromise reliability in the end systems they inhabit. This paper helps the board fabricator and the contract assembler understand how the copper plating process affects voiding levels in solder joints, for via-in-pad Printed Circuit Boards (PCBs). We compare three different plating methods for filling microvias, and then study the impact of these methods on the occurrence frequency and size of these voids. Three types of plating processes were analyzed: conformal plate (no via-fill), a one-step via-fill, and a two-step via-fill. Voiding frequency and size were determined from sample cross-sections and X-ray inspection. It is observed that even "low success" in filling the vias can significantly reduce the void size and occurrence in the solder joints.

**Introduction**
There is a constant struggle to maintain high I/O while decreasing the size of area array packages. One limiting factor has been the use of vias/dog bone pattern for interconnection of these devices to the Printed Wiring Board (PWB) surface. An alternative, via-in-pad, places blind microvias in the Surface Mount Technology (SMT) pads. The interconnection is then through subsequent inner layers, providing space for finer pitch chip scale devices. The use of via-in-pad while not new to electronic devices is now being considered for high volume PWB design. However, while via-in-pad helps design engineers, it creates problems for both fabrication and assembly of PWBs.

With a microvia ablated to a 100 micron diameter, conformal plating under best conditions will reduce the aperture by at least 50% in diameter. Thus, the finished size of a 100-micron microvia is an opening of less than 50 microns. Using current PWB fabrication equipment, a via size of 50 micron presents issues with wetting that result in:

- Entrapped corrosive process chemistry[1] from poor rinsing
- Incomplete coverage of the final surface finish
- Voiding due to etch out of the electroplated copper from incomplete or porous electrolytic tin coverage

By at least partially filling the microvias and achieving a fill angle of > 45°, wetting, rinsing, and coverage are less of an issue. The final result is overall improvement in long-term reliability. On the assembly side a via-in-pad will be “tented” with solder paste during the printing process unless solder paste is intentionally printed at an offset. This causes a gas pocket to form in the microvia that expands into the solder joint during the reflow process (Figure 1).

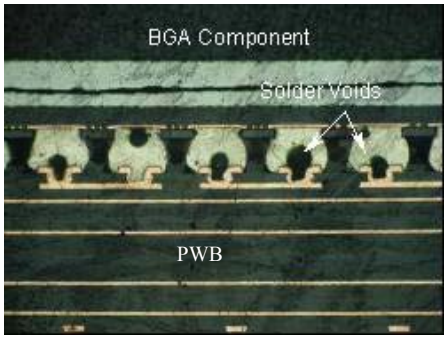



**Figure 1 - Solder Voids From Via-in-pad Designs**

The result is a high percentage of voids in the solder joint. Based on X-ray imaging, the IPC-7095 standard[2] specifies three categories for void size for BGA solder joints. These categories are based on the percentage of joint cross-sectional area occupied by the voided area.

Class III (Small): Void area is < 9%
Class II (Medium): Void area > 9% but < 20.25%
Class I (Large): Void area > 20.25% but < 36%

This standard does not specify a category for voids > 36% and assumes that is beyond acceptable limits of most products. Class III product would be for highest reliability with the smallest allowable void area.

Various methods of preventing void formation have been reported, including via-fill with a solder "capping" step,[3,4] via-fill with plated copper,[5] applying conductive inks,[6] creating via diameters wide enough to avoid trapping air,[7] and by applying a vacuum during reflow.[8]

In the first phase of this project alternative solder pastes were compared with no preventative measures to reduce voids in that phase. This test showed that optimization of the assembly process conditions and material formulations can reduce voids. However, void size and occurrence was extremely high with conformal plated via-in-pads. The second phase, reported here, investigates the impact of filling the micro-via with plated copper (two separate technologies in development, "Red" and "Blue") as a preventative measure for reducing or eliminating microvia-induced voids. This study was undertaken to quantify the frequency as well as the location and size of voids with and without copper filled vias.

**Experimental Procedure**

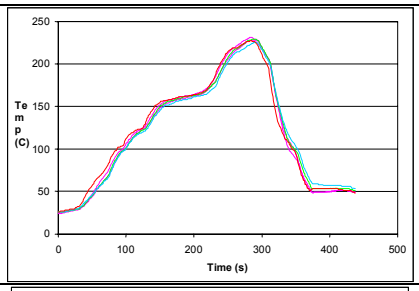
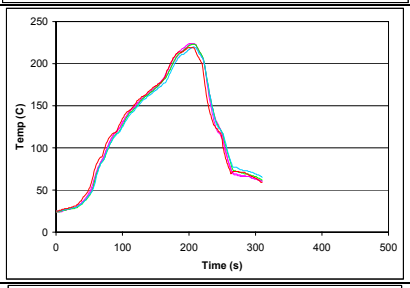
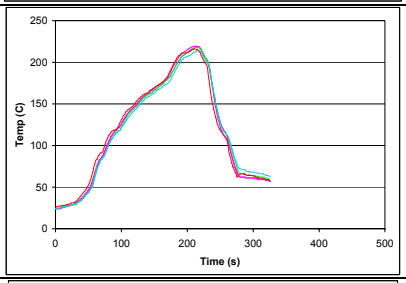
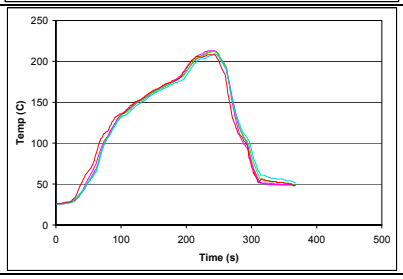
A test vehicle (TV) with microvia-in-pad designs was plated with three different acid copper systems. The TV had 1mm pitch ball grid arrays (BGA) pads with up to 300 I/O. The control copper plating process provided conformal plating of the microvia. It is a standard type acid copper formulation with high sulfuric acid and low copper sulfate. Two via-fill formulations were used. The one designated as "Red" is a two step system utilizing a pre-dip to suppress the surface plating followed by a separate grain refiner system in the plating bath. The "Blue" formulation is a newer development where the suppressor and grain refinement is all done in the plating process. The final finish on all test vehicles was OSP.

Table 1 summarizes the key reflow profile parameters for this experiment. The four no clean eutectic paste-related scenarios outlined in Table 2 were utilized with each copper plating process. Specific paste chemistries were chosen to provide minimal to maximum amounts of volatile materials. Reflow parameters were set to allow maximum and minimum time for volatiles to escape. In this manner a range of solder voiding was created to measure the true effect of different via-fill techniques.

**Table 1 - Key Thermal Profile Parameters**

| Case | Peak Temperature (deg C) | Time Above Liquidus (seconds) |
|---|---|---|
| **Control** | 231 | 90 |
| **Case 1** | 224 | 70 |
| **Case 2** | 220 | 71 |
| **Case 3** | 213 | 77 |

**Table 2 - Paste and Reflow Scenarios Used in Phase 1 & 2**

| | Paste Formulation | Reflow Profile |
|---|---|---|
| **Control Paste** | • 90% metal content<br>• 846 KCPS viscosity |  |
| **Case 1** | • 90% metal content<br>• M13 viscosity |  |
| **Case 2** | • 89.5% metal content<br>• M14 viscosity |  |
| **Case 3** | Same as Case 2 |  |

All conditions are compared in terms of the frequency of void occurrence, the size of the average void, and whether or not the void is still touching the microvia pad (void height). Cross-sections were utilized to show void location (Figure 2), occurrence of voids and via filling success.


**Figure 2 - Void Height**

X-ray data was collected using a Teradyne/Genrad GR-X-160L with Nicolet AIP 3 software. X-ray analysis was used to measure void size and occurrence. An example of X-ray images (before void detection and after) is provided in Figure 3.

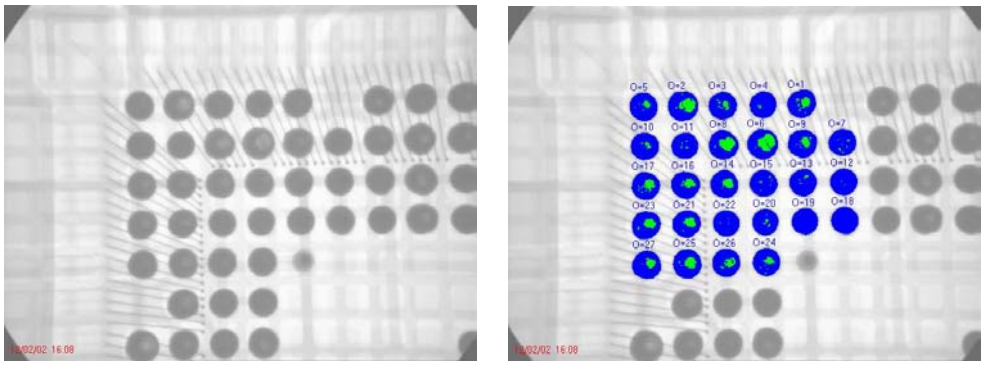


**Figure 3 - Typical X-ray Results**

**Results and Discussion: Cross-Section Results for Via-Fill, Void Occurrence, & Location**

In this test, as listed in Table 3, the Blue process filled only 59% of the vias, whereas the Red two-step process filled 96% of the vias. The variation in via filling (Figure 4) is due to differences in equipment used for each process in combination with rough microvia side walls.


**Figure 4 - Three Types of Copper Processes and Variation in Via Fill**

The high density interconnect (HDI) layer in this TV was made using 1080 prepreg with copper foil. The resultant via structure had severe glass exposure (Figure 5) on the microvia wall.

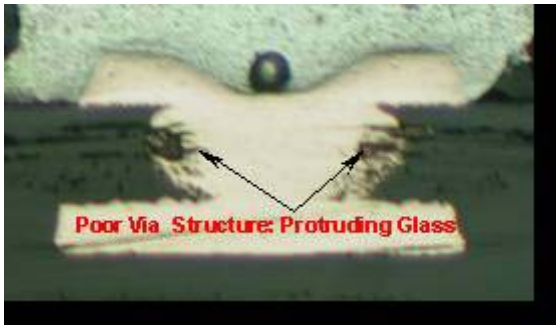



**Figure 5 - Rough Microvia**

The roughness of the via wall makes wetting of the microvia difficult resulting in poor copper plating. This problem can be eliminated by - using flat glass designed for laser ablation, optimizing the desmear process to ensure glass removal or by using resin coated copper. Under more optimum via geometries (i.e. no glass bundles protruding into the via, cone shaped etc.) via filling of the Blue process was superior. The result with this TV was three different levels of via-fill, conformal plating with the control, and partial filling with the Blue process and full fill with the Red process.

The cross-section data (listed in Table 3) provides a summary of the percentage of solder joints containing voids, the percentage of voids classified as "low," and the percentage of solder joints that were successfully filled with each via-fill technology. The detailed data is presented graphically in Figures 6 and 7.

**Table 3 - Void Summary (Data From Cross-Sections Only)**

| | No Fill | Blue Fill | Red Fill |
|---|---|---|---|
| # of Joints | 214 | 210 | 196 |
| # of Joints w/Voids | 162 | 81 | 46 |
| % w/Voids | 76% | 39% | 23% |
| % Low Voids | 81% | 85% | 20% |
| % Filled Via | 0% | 59% | 96% |

Table 3 data reveals significantly fewer voids for both via-fill technologies (@ 95% CI). Table 3 also shows mixed results in terms of the % of voids that are touching the microvia pad ("low" voids). Blue via-fill void heights are not significantly different than the No Fill case (@ 95% CI). However, the Red via-fill shows that far fewer of the voids are touching the pad.

Comparing the percentage of solder joints with voids versus the percentage of joints with successful via-fill (Figure 6), there is an apparent inverse correlation. The coefficient of determination ($R^2$) for a linear regression based on the data computes as 0.75, meaning that the via-fill success rate accounts for 75% of the variation in void occurrence. Each via-fill method clearly has a role in reducing voids. Statistical analysis (with a 95% confidence interval [CI]) indicates that both Blue and Red via-fill methods reduce the level of voiding significantly.

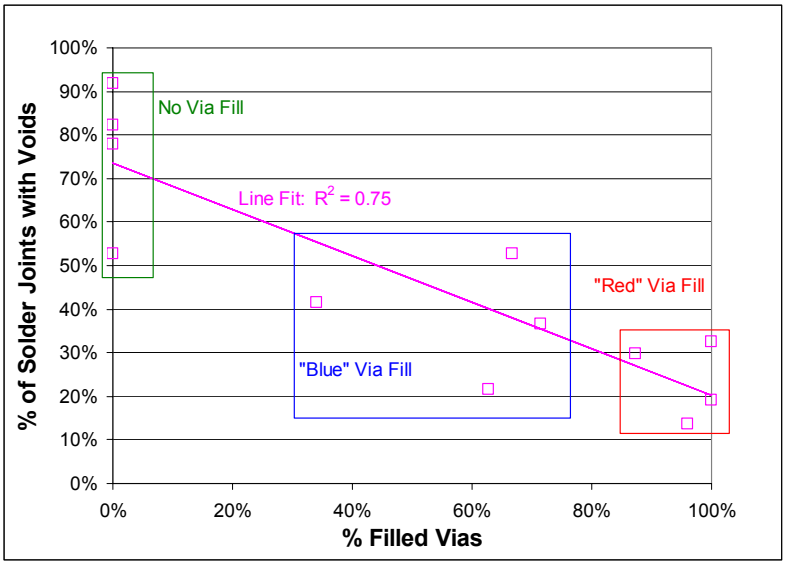



**Figure 6 - Cross-section Data: Comparing Void Occurrence with Via-Fill Success**

Also, via-fill success and void occurrence appear to be different in the Blue versus Red via-fill technologies. Statistical analysis (@ 95% CI) reveals that Red has a significantly higher percentage of via-fill and a significantly lower occurrence of voids than Blue via-fill.

Comparing the percentage of voids that are "low" versus the percentage of solder joints with successful via-fill (Figure 7), there is no valid correlation ($R^2$=0.45). Statistical analysis (@ 95% CI) shows that the Blue case is not significantly different than the Non-via-fill case. However, there are significant differences in "low voids" between Red and All via-fill (grouping Red and Blue together) versus the Non-via-fill case (@ 95% CI): voids for these two situations tend to be up, or off of the pad.

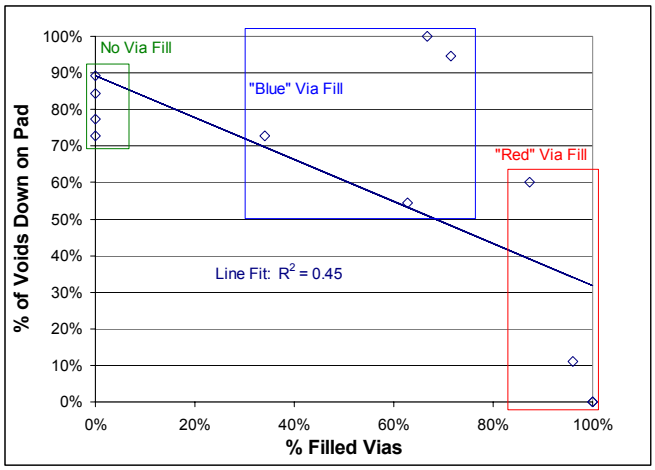



**Figure 7 - Cross-section Data: Comparing Void Height with Via Fill Success**

The reason for high void height when vias are successfully filled (Red Process), is the flatness of the pad after it has been filled. Without a via cavity, there is no mechanism for trapping air. Therefore, voids that occur in these solder joints are formed for other reasons (i.e., due to flux gases or paste deposit shape) and are formed randomly within the solder ball, leading to a low likelihood of the void touching the pad.

**Results and Discussion: X-Ray Results Void Size**

Table 4 shows the general results of all cases, revealing the effects of Blue and Red via-fill on void size. The row "Average Void Area %" calculates the average void size as a percent of the solder joint cross-sectional area (only considering those solder joints with voids present).

**Table 4 - Impact of Via-Fill on Void Size**

| | All Data | | |
|---|---|---|---|
| | No Fill | Blue | Red |
| Sample Size (# Joints) | 1940 | 1940 | 1940 |
| Average Void Area % | 7.6% | 2.8% | 2.0% |
| | | | |
| Voids @ Class I | 3% | 0% | 0% |
| Voids @ Class II | 32% | 5% | 1% |
| Voids @ Class III | 65% | 95% | 99% |

The average void size for voids in Blue via-fill solder joints is 64% smaller than voids found in the No Fill data. The Red via-fill voids are 74% smaller. Also, while 32% of the No Fill voids fall into the Class II (medium size) void size category, only 5% of Blue via-fill and 1% of Red via-fill voids fall into this category. For Red and Blue via-fill, the remainder of voids are Class III (smallest size).

Figure 8 graphs the average void size for each condition. The following results are statistically significant (@ 95% CI):

- Void sizes drop significantly for all of the via-fill technologies, compared to the No Fill condition for each case.
- All via-fill cases show lower void size than the Control Paste with no fill, with the exception of the Blue via-fill for Case 3.
- Lumped as a group, Red via-fill results in lower void sizes than Blue via-fill.

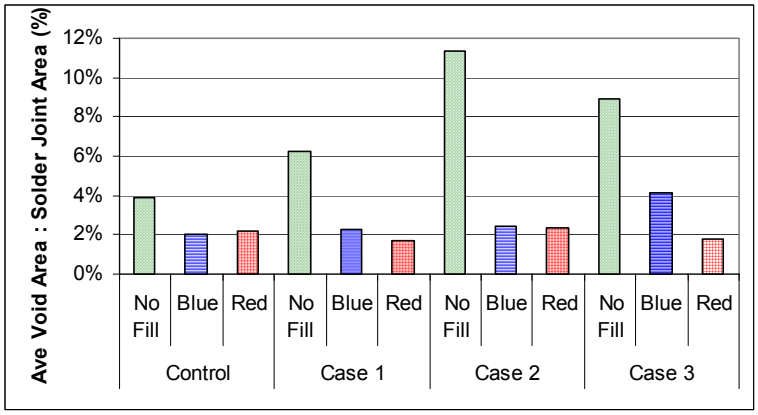



**Figure 8 - Void Size as a Percentage of Solder Joint Cross-sectional Area**

**Results and Discussion: X-Ray Results Void Occurrence**

X-ray analysis gave a much higher frequency of voids (Figure 9) versus the data from cross-sections (Figure 6). The likely reasons for this difference are the following:

- The cross-section voids are detected by eye, while the X-ray voids are detected using image analysis software capable of resolving hundreds of shades of gray as well as extremely small voids (down to the 2-3 micron feature size).
- The cross-section analysis only counts those voids that intersect the middle of the solder joint (where the cut has been made). Many small voids are not visible when considering just this plane of the solder joint.

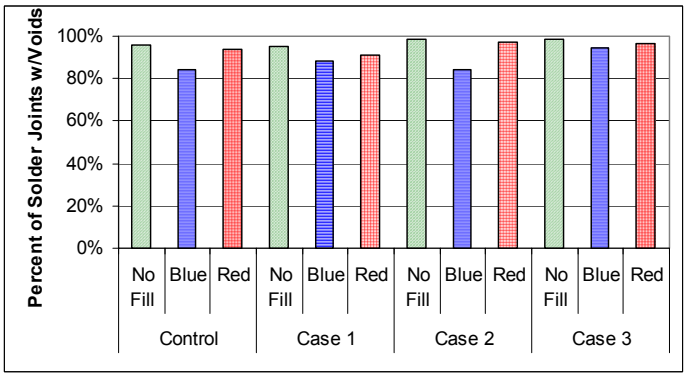



**Figure 9 - Percentage of Solder Joints with Voids (X-ray data)**

Comparing the percentage frequency of voids for each of the cases, the data shows high readings for all cases, in the range of 84% to 99%. The consistently high void prevalence is mainly due to the high sensitivity of the X-ray system: just about every solder joint has a void 2-3 microns in size or larger (or an artifact of similar size, such as a solder surface dimple or copper plating void). Due to the X-ray system sensitivity, X-ray analysis on void occurrence frequency should be used with caution.

The high level of X-ray sensitivity warrants a closer look at void size in calculating void occurrence frequency. With sensitive X-ray equipment, the question arises as to whether voids on the order of a few microns in size are actually present. False detection of extremely small voids can occur due to several reasons such as; solder bump surface irregularities or copper patterns in the circuit board that are aligned with the X-ray source and detector. However, there is no known standard below which a void would be considered "insignificant."

To try and quantify smallest significant void size, Figure 10 plots void occurrence frequency as a function of minimum void size. For this analysis, solder joint voids are disregarded if they are below a limit chosen on the x-axis in Figure 10. For example, at a minimum significant void size of 10% of the solder joint area, there are far fewer voids than when the minimum size is 1%.

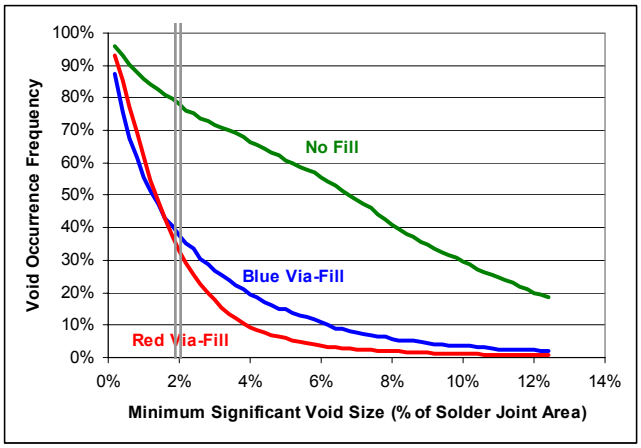



**Figure 10 - "What-if" Analysis for Minimum Void Size**

At 2% of the solder joint area, the slope of both the Red & Blue via-fill curves drop significantly in Figure 10 indicating that void size less than 2% may be noise from the X-ray or assembly process. Further, with a minimum significant void size of about 2%, it appears that the X-ray data agrees well with the cross-section data. Table 5 compares the data for a minimum void size of 2.2% and data from the cross-sections.

**Table 5 - Void Occurrence Frequencies for X-ray Versus Cross-section Data**

| | All Data | | |
|---|---|---|---|
| | No Fill | Blue | Red |
| X-ray data - 2.2% min size | 76% | 35% | 29% |
| Cross-section data | 76% | 39% | 23% |

**Effect of Solder Paste Parameters on Voiding**

Figures 11 through 13 show the distribution of absolute void size as detected by the X-ray system. The void size categories in "Blue" partial filling (Figure 12) and "Red" full fill (Figure 13) copper processes are less since voids are much smaller with vias filled with copper.

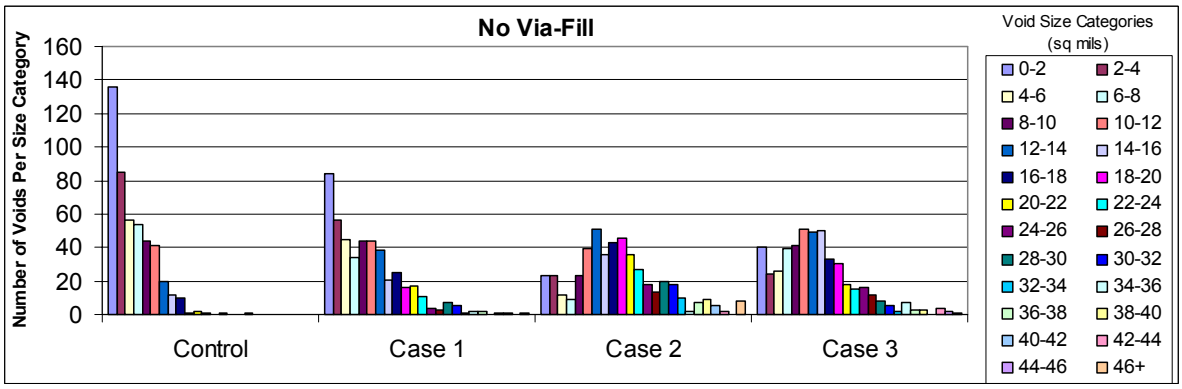



**Figure 11 - Void Frequency Distribution – No Via-fill- Control Copper**

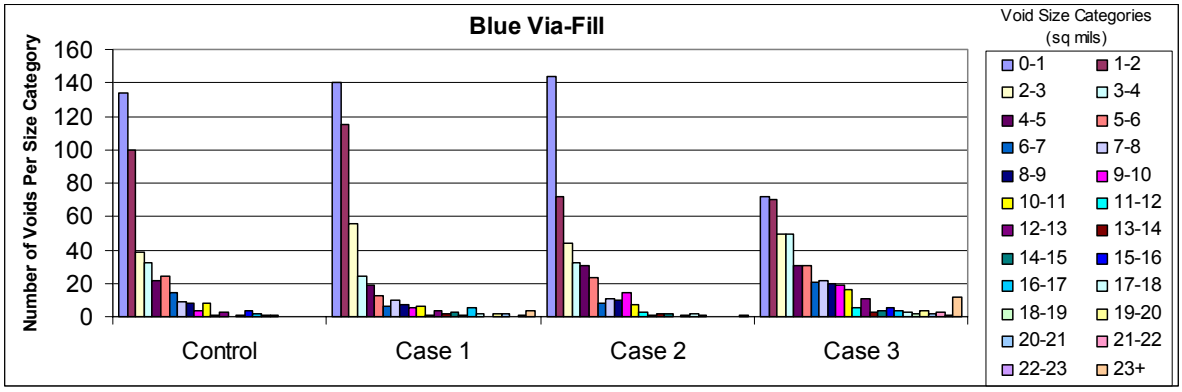



**Figure 12 - Void Frequency Distribution – "Blue" (Partial) Via-fill**

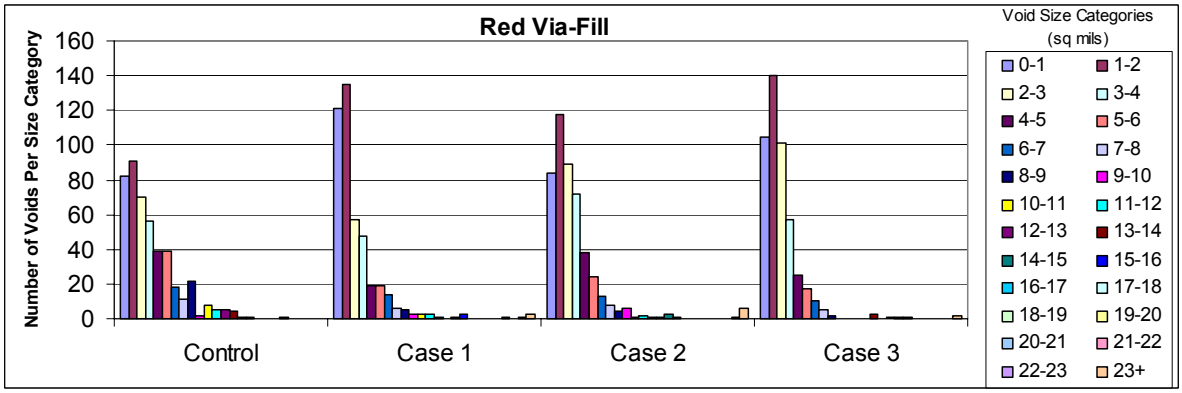



**Figure 13 - Void Frequency Distribution – "Red" (Full) Via-ill**

Plotting the average void area for each of the different paste and reflow conditions in Figure 14 illustrates that both paste selection and reflow profile have an influence on solder void size. Reflow profiles with longer time above liquidus (control paste & Case 3) allow more time for volatiles to escape. In addition, specific paste chemistry will also contribute to void size especially with non-filled vias.

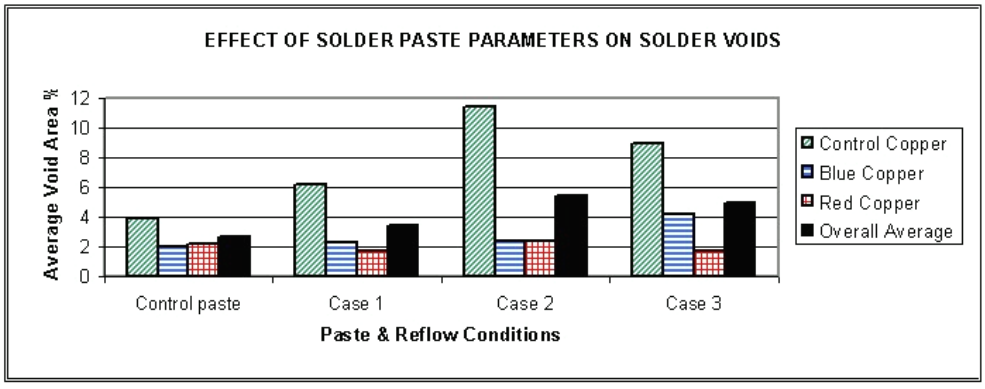
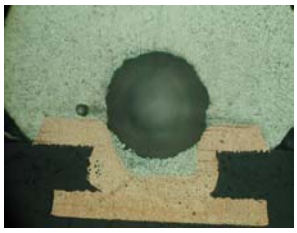
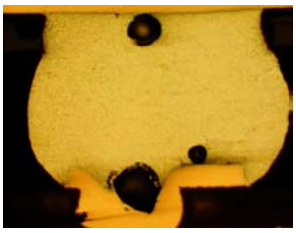
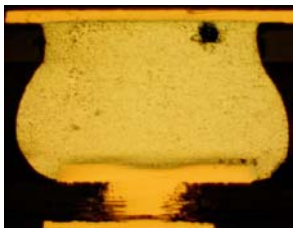
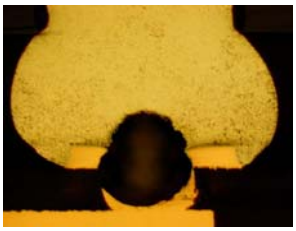
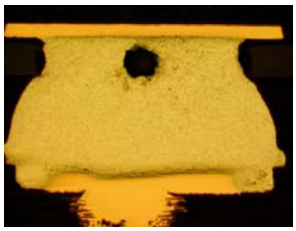
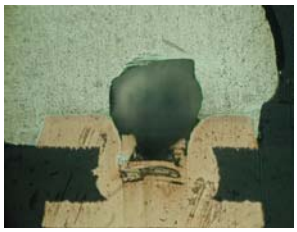
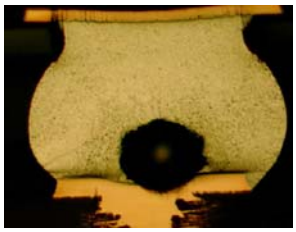
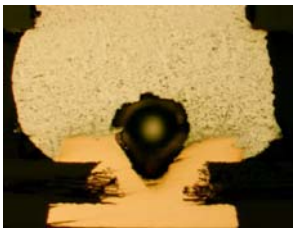
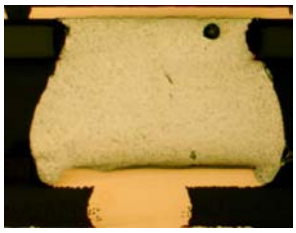



**Figure 14 - Average Void Size Copper Process Versus Paste & Reflow Conditions**

However both paste chemistry and reflow profile have much less of an effect when the microvias have at least partial filling. Cross-section data in Table 6 illustrates the same conclusion, paste and reflow profile yield a bigger impact on void size with conformal plated copper.

**Table 6 - Comparison of Solder Voids Copper Plating vs. Solder Paste Parameters**

| | Conformal Copper | "Blue" Via-Fill Copper | "Red" Via-Fill Copper |
|---|---|---|---|
| **Control**<br>**Optimized Reflow** |  |  |  |
| CASE 1<br>Alt Paste 1, Std Reflow |  |  |  |
| CASE 2<br>Alt Paste 2, Straight Ramp Reflow |  |  |  |
| CASE 3<br>Alt Paste 2, Low Voiding Reflow |  |  |  |

Even partial filling allows a wider selection of paste and reflow profile so that other criteria such as solder balls can be compensated for without a dramatic increase in void size. As the microvias fill with copper, not only does the potential gas volume decrease, but the angle of the microvia wall becomes $< 45^{o}$ allowing easier removal of trapped volatiles.

**Summary and Conclusion**

After analyzing void areas using X-ray imaging, void height using cross-sections and void frequency using both methods, the following conclusions can be drawn:

- Void Size (percentage of solder joint area, based on X-ray data): Full via-filling with the "Red" process reduced void size by 74% versus vias with the control copper process or conformal plated. Even partial filling with the "Blue" process reduced voids size by 64% versus conformal plating.
- Frequency of Void Occurrence (based on X-ray and cross-section data): According to cross-section data, via-fill results in fewer voids than for the No Fill solder joints (76% occurrence for No Fill overall versus 39% for Blue via-fill and 23% for Red via-fill). The X-ray results confirm a reduction in void frequency with via-fill but the improvement indicated by the raw data is much less. X-ray data can come close to cross-section data if the definition of minimum significant void size is greater than ~2%.
- Void Location (touching the microvia pad or not, based on cross-sections): The Blue "partial" via-fill process results in a similar percentage of "low" void heights as the No Fill case (81% low for No Fill versus 85% low for Blue via-fill). However, the Red full via-fill process results in only 20% of the voids still attached to the PWB surface. This effect is due to the degree of copper via-filling. A pad with full via-fill has a mostly flat surface, while a pad with no or partial via-fill still has a microvia cavity that can serve as an "attachment point" for a void.
- Solder Paste Selection and Reflow Profile: Paste and reflow selection has a much larger impact on solder void size and frequency with a conformal copper process. Paste parameters have little effect on solder voids with either full or partial filling of the microvias. Filling of the microvias with copper provides a wider process window for selection of paste parameters.

Unique copper plating chemistries are being developed to fill microvias void free with copper. These systems, when utilized for microvia-in-pad designs reduce solder void size and occurrence of voiding. Additional work is planned to look at solder voids and reliability of finer pitch chip scale devices with the use of Pb-free paste and final finishes.

**References**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