Design of Optimized High Speed Circuits

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Abstract
Designing a signal path to provide a particular impedance is thought to be a well understood science. The first issue which is often overlooked is to analytically establish the need for specifying a controlled impedance signal path. After determining this to be the case, the designer normally selects a combination of line width and dielectric thickness to satisfy the stated requirement. There are usually, however, an infinity of selections that will satisfy any stated impedance requirement. Obviously, one would prefer to select the combination that will minimize variations in the impedance caused by the fabrication process. This becomes extremely important in designs using low impedance paths such as Rambus.

This paper discusses an analytical procedure addressing these issues. Once the optimal selection is made, it is then possible as further described in this paper, to define the statistical variation of the impedance to be expected for the optimal construction.

Introduction
Few printed circuit board parameters are as well known as impedance or as misunderstood. Controlled impedance designs have been around for sometime. Motorola produced what some believe to be one of the best primers on understanding impedance and its application to printed circuit boards in its MECL System Design Handbook (Reference 1).

The initial consideration in high-speed circuit design is to determine if the impedance needs to be controlled. As discussed below there are several accepted procedures for making this judgment. Two of the more popular methods are discussed below. Following this discussion, the issue of fabrication optimization to achieve the desired impedance is discussed.

Criteria for Stipulating Controlled Impedance
A good rule of thumb is when length of the structure is greater than one tenth of the wavelength for fundamental frequencies and harmonics an impedance requirement is in order, or:

$$\lambda = c / f (e_r)^{1/2} \quad (1)$$

i.e., wavelength = speed of light / frequency * √(dielectric constant)

As an example, a 100 MHz signal in FR-4

$$\lambda = 3 \times 10^8 / 100 \times 10^6 (4.3)^{1/2}$$

$$\lambda = 1.4 \text{ m}$$

$$\lambda/10 = 0.14\text{m} \sim 6"$$

Therefore, if the structure is longer than 6" there will be a need to control the impedance. Once the need is identified the next step is to develop the structure which will provide the impedance and in particular the optimum structure. This is the "famous" six inch rule of thumb that has been used by designers for years.

This same issue is discussed by Johnson and Graham (Reference 2) who approached the issue from the standpoint of rise time; in particular when the length of the electrical path is greater than the length of the rising edge (l) it is necessary to control the impedance. The length of the rising edge is:

$$l = T_r/D \quad (2)$$

where:

T_r is the rise time

D is the delay time (180 ps/in for FR4)

A rise time of one nanosecond then corresponds to length of 5.5 inches. To be conservative, most designers become concerned if the length of the structure is within 50% of this value.

While opinions vary, it is generally accepted that if the electrical structures exceed 6 inches, impedance will be an issue. As bandwidths become larger, the sensitivity to structure length becomes more acute.

Analytical Modeling Considerations

Early on in the evolution of high-speed circuits, closed form algebraic approximations such as presented in (References1 and 2) produced acceptable results for impedance modeling. These approximations along with many others used in the industry (including IPC) are helpful for simple PCB designs and first order calculations. Typically, they can be used to establish the framework of the PCB environment: layer count, maximum line length, and parallelism rules.

As pointed out in Reference 3, it is first of all important to realize that the governing equations for high speed current flow (Maxwell's Equations) are highly nonlinear and have never been reduced to an exact closed form equivalent. Normally, the assumptions associated with a particular closed form approximation are stated. Often, however, the impact of these assumptions have been ignored, overlooked or misunderstood. Consequently, designers have been trapped in a time consuming and expensive iterative loop requiring numerous prototype test vehicles before finally arriving at an appropriate dielectric spacing and trace width. In other cases, designers have blindly used empirical tables correlating the impedance to the construction of the PCB. When the finished product does not meet the design intent, the tables are modified to include the most recent observations.

This problem has become magnified as the sophistication of the PCB designs continue to increase. Algebraic or empirical approximations to the governing partial differential equations are more often than not poor predictors of the electrical characteristics of many leading edge, high-speed circuit designs. These include such designs as asymmetrical differential broad side signal paths, coplanar ground and signal layers, narrow signal paths coupled with a thin dielectric thickness, embedded microstrip and non-adjacent signal to reference ground planes. To further complicate the situation designers are resorting to multiple material packages each with significantly different electrical properties.

All of these concepts and others are becoming commonplace in the high layer count boards used in servers, routers and high-speed memory storage units. To deal with this issue, a new generation of modeling tools has evolved which numerically integrate the exact governing differential equations using a stated board construction geometry as the boundary conditions for the solution to the governing equations. By varying the construction geometry, the designer can quickly and accurately converge upon a suitable construction for the design requirements. These are the so-called finite element models. An enlighten application of these analytical tools, removes the mystery of predicting impedance.

With these sophisticated tools, complicated designs, both from the standpoint of design feasibility and fabrication, can be analyzed. We are also able to optimize the design to minimize the effect of process fluctuations upon the electrical performance of the board. This is of paramount importance in high layer count boards with impedance requirements on many layers; if the impedance is out of tolerance on any layer then the board is defective. By optimizing the construction of the board, large yield improvements can be obtained. This technique is discussed below.

Still another example, which demonstrates the importance of accurate impedance modeling, is the Rambus application. In this case the target impedance is 28 Ohms with a tolerance of ten percent. A finite element simulation yielded values of .018" for circuit width and .0045" for dielectric spacing. A similar simulation using a closed form algebraic approximation with a dielectric thickness of .0045" and a line width of .018"produces an impedance of 18.70 Ohms. A full 33 percent lower than the 28 Ohms that would actually have been obtain if you were to manufacture the microstrip construction per Figure 1. On the other hand, if you were to use the closed form formula to derive the proper values for a 28-Ohm line, the results when manufactured would be a 34-Ohm impedance line. Clearly, the closed form approximations are simply inadequate for Rambus and many other applications.

Design Optimization

Sophisticated software packages such as a finite element analyzer now provide the circuit board designer the capability to quickly perform accurate impedance calculations for various PCB geometrical constructions. This capability opens the door to optimization techniques that here to for were impractical. A particularly important example is the optimization of the board impedance parameters, circuit width and dielectric thickness, with respect to the manufacturing processes. Techniques such as this are especially useful in constructing Rambus designs, which have an inherently small absolute impedance tolerance, typically less than three Ohms. The mechanics of this process is discussed below.

The impedance of a path is to first order controlled by three parameters, the width of the circuit path and both the permeability and thickness of the dielectric media separating the trace and the reference ground plane. Fortuitously, as will be explained, defining the impedance does not uniquely define the construction of the board.

The designer can take advantage of this situation and uniquely select the design
parameters, which will optimize the manufacturing reproducibility of the PCB. That is, maximize the C_{pk} associated with the likelihood of satisfying the impedance requirements. This parameter can be both predetermined and optimized.

Procedure

A procedure for attacking this issue was first discussed in Reference (3). An example of this process is shown in the enclosed figures that treat a Rambus microstrip design. Typically, as mentioned, Rambus designs have an impedance requirement of 28 Ohms and a tolerance of $\pm$10%.

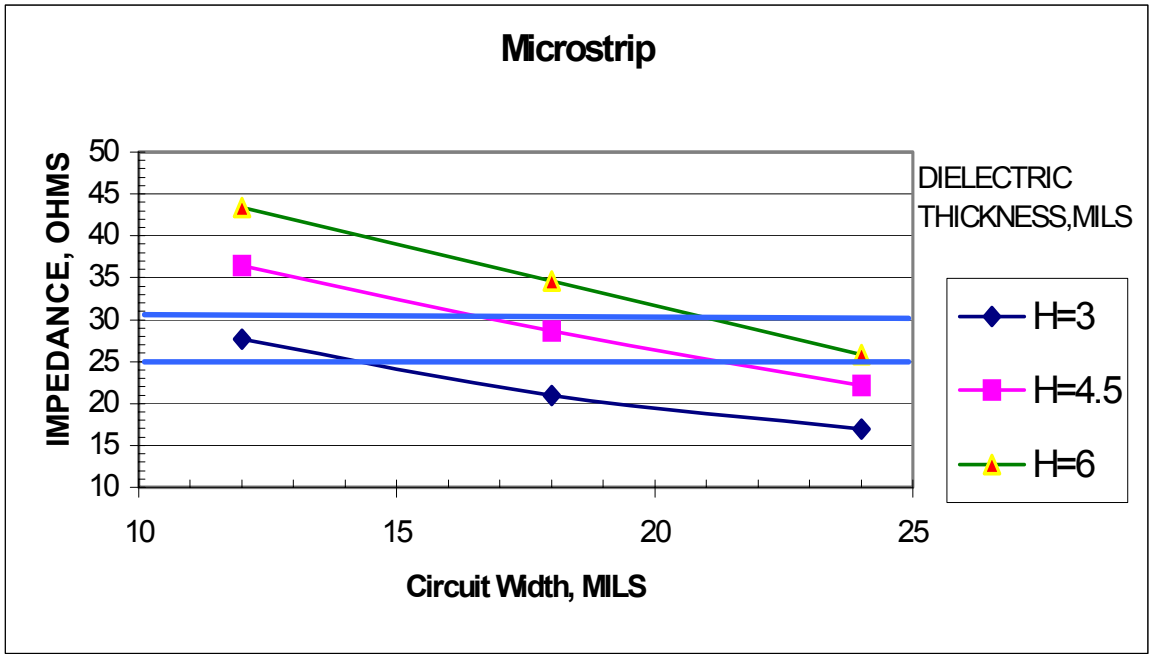

Figure 1 - Microstrip

Figure 1 shows the impedance of a microstrip circuit path as a function of circuit width and dielectric thickness in the neighborhood of 28 Ohms. The horizontal window drawn about the 28-Ohm axis defines the various combinations of circuit widths and dielectric thickness that will satisfy the design requirement. The objective is to select the combination that will minimize the sensitivity of the design to manufacturing fluctuations.

After defining the impedance as a function of the independent variables in the neighborhood of the desired value, the next step is to calculate the partial derivatives of the impedance with respect to these variables, i.e. $\partial Z/\partial T_D)_{LW}$ and $\partial Z/\partial L_W)_{TD}$. We refer to these derivatives as the sensitivity coefficients. These variables can be empirically measured from the data shown in Figure 1. The values at the desired 28 Ohms are presented in Figures 2 and 3.

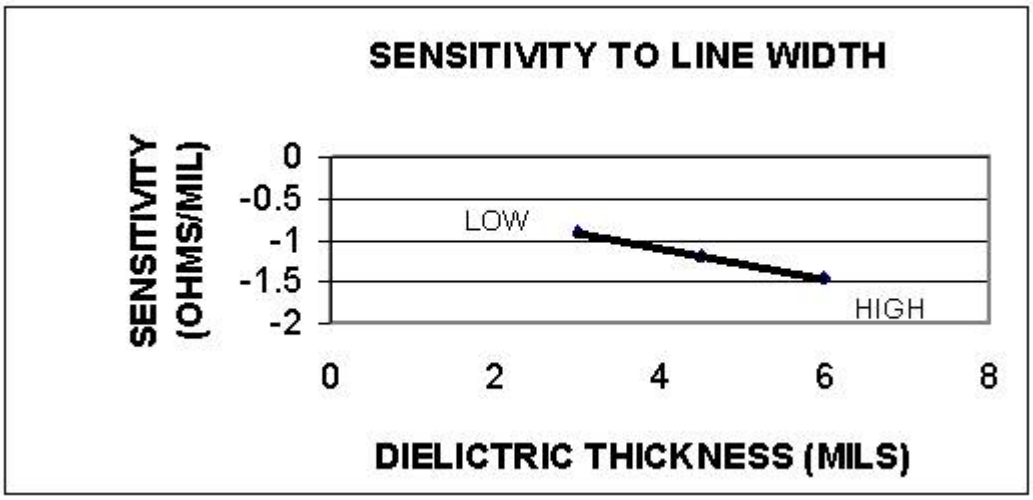

Figure 2 – Sensitivity of Line Width

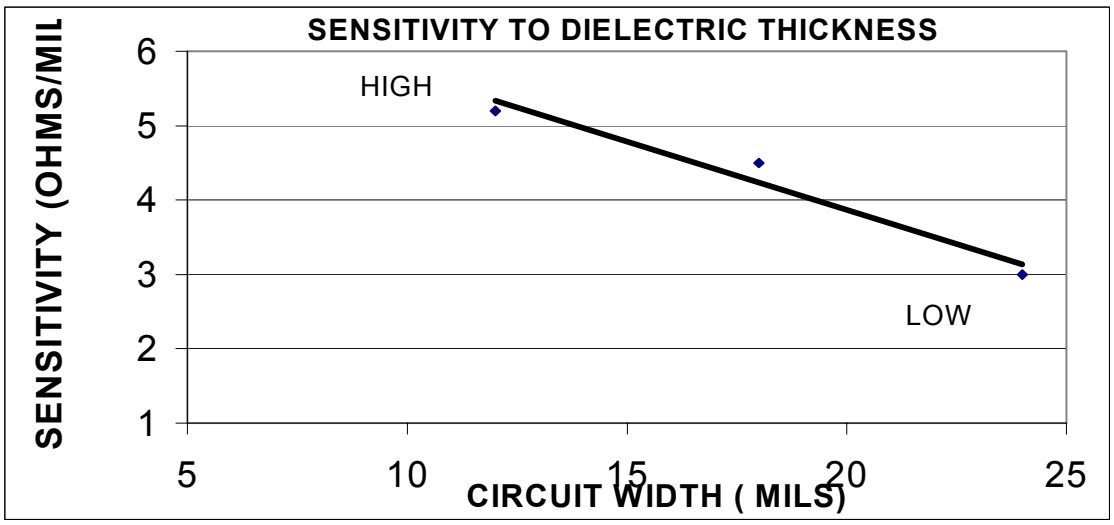

Figure 3 – Sensitivity to Dielectric Thickness

The range of the anticipated fluctuation of the impedance can now be determined by coupling the data in Figures 2 and 3 with the Statistical Process Control (SPC) information for the etching and laminating processes which is commonplace in all progressive manufacturing facilities. For the C_{pk} calculation, we need the three-sigma values of the operating variation for circuit width variation (ΔL_W) and the dielectric thickness (ΔT_D).

At this point, we assume that the two variables are independent, i.e. the two statistical distributions defining the process variation of both the circuit width and dielectric thickness are not related. In that case (see Reference 4), the expected variation in the impedance to the same statistical confidence level (x) is:

$$(\Delta Z)_x^2 = (1/2)\ \{[\ \partial Z/\partial T_D)_{LW}(\Delta T_D)_x]^2 + [\ \partial Z/\partial L_W\ )_{TD}\ (\Delta L_W)_x]^2\} \qquad (3)$$

If the three-sigma values are selected for both ΔT_D and ΔL_W, the C_{pk} for the impedance variation is:

$$C_{pk} = (\Delta Z)_{TOL}/(\Delta Z)_{3\sigma} \qquad (4)$$

Where $(\Delta Z)_{TOL}$ is the specified tolerance for the impedance.

Going back to Figures 2 and 3, the C_{pk} can then be determined for a practical range of both circuit widths and dielectric thickness. The construction variables can then be selected to maximize C_{pk}.

Summary

The necessity of controlled impedance designs has been discussed and techniques proposed to define where controlled impedance is appropriate. Analytical methods for designing such structures are discussed. Finally, these techniques are used to develop to optimize controlled impedance designs and determine the expected statistical variation in the impedance caused by manufacturing fluctuations.

References

1. Blood, W. R., MECL System Design Handbook, Motorola, Inc, 1980
2. Johnson, H. W. and Graham, M., High-Speed Digital Design, Prentice Hall PTR, 1993.
3. Mackillop, J. W. and Parker, J. L., Sensitivity Analysis of High Speed Circuits, Future Circuits, Issue 7, 2001
4. Dixon, W. J. and Massey, F. J., Introduction to Statistical Analysis, McGraw-Hill, 1969.