Cray X1: Extreme Performance Requires Extreme Reliability

Terry Fischer
Hitachi Chemical Co. America, Ltd.
Cupertino, CA

Gary Purvis
Cray, Inc.
Chippewa Falls, WI

Yoichi Daiko
Hitachi Printed Wiring Board Solutions Co., Ltd.
Kanagawa, Japan

Abstract
The Cray X1™ system dramatically extends the capability of supercomputers with High efficiency and extreme performance. Specifically designed to meet the needs of the high-end user, the Cray X1 provides exceptional memory bandwidth, low-latency interconnects and vector-processing capabilities.

While development of the Cray X1 received substantial support from several U.S. government agencies, including the National Security Agency (NSA), Cray decided to develop its own specifications for printed wiring boards, materials and reliability.

This paper will discuss the introduction of the Newest Cray X1 Supercomputer, and the requirements of the printed wiring boards used in the systems. It will also focus on the Unique Challenges of the fabrication of the PWB, the different materials explored, their properties, and their setbacks. Also addressed will be the stringent electrical test requirements and the many quality and reliability controls for PCB acceptance from its suppliers.

Introduction
The Cray X1 product is a major milestone en route to Cray's goal of delivering, by 2010, the world's first supercomputer able to sustain petaflop speeds (10^E15 calculations/second) on a variety of challenging applications. Problems needing this extreme performance include drug discovery, energy and transportation modeling, nanotechnology, weather forecasting and climate modeling, planning for natural pandemics and bio-terrorism, and more HIGH- EFFICIENCY / EXTREME PERFORMANCE.

The Cray X1 system, designed to be the world's most powerful supercomputer product, features ultra-fast (12.8 gigaflops) individual processors, up to 819 gigaflops of peak computing power in a single chassis, and a high-bandwidth, low-latency interconnect for substantially more efficient scaling than on clustered SMP systems. The Cray X1 system is available with up to 52.4 teraflops of peak computing power. The Cray X1 supercomputer is the successor to Cray MPP's and vector products.

PCB Requirements for Cray X1
The design of the Node PWB called for a 34-layer board, having eight signal plane pairs, with sixteen layers of power and ground. Both sides of the finished PCB would require metalization. An overall bare copper board with an Organic Solderability Preservative (OSP) that would allow a shelf life of at least 12 months, two different types of plating; bondable gold in the MCM areas, and a very closely controlled thickness of Pb/Sn for the edge connectors attach along the periphery of the finished board.

The size of the PCB is 22" x 17" (560 x 432 mm) and with the coupon requirements the panel size would be increased to 24" x 20"(610 x 508 mm), minimum. The thickness overall is 0.135",(3.5 mm +/- 5%), with PTH diameters down to 0.010"(0.25 mm) and very critical clearances of 0.028"(0.7 mm) through power and ground planes. This would make registration of all of the inner layers and drill locations a must to control at fabrication. Characteristic Impedance measurements would be required on all signal layers having specifications of: single line impedance of 45 Ω and differential lines of 100 Ω all with tolerances of +/- 5%. The layout of the surface called for SMT, BGA/MCM pitch of 0.040" (1mm). The total buried via layer count would be 34,685 and the total Plated Through Holes would be 66,000.

SV2 Node Module (bottom)

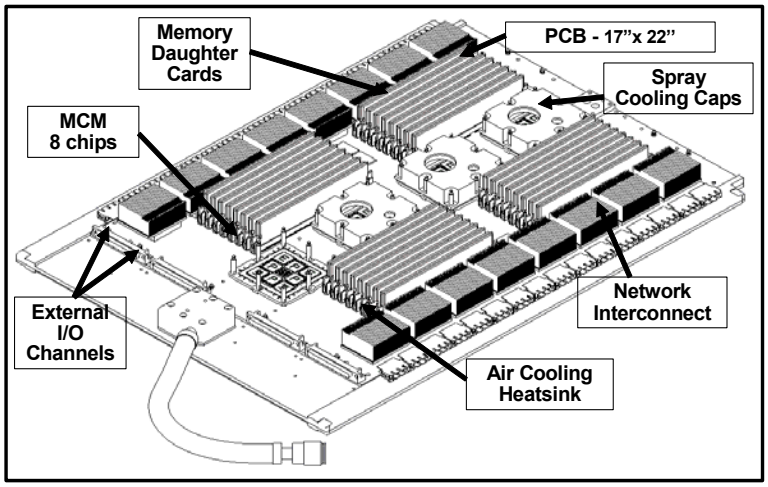


Figure 1 - Node Assembly

Material designation was not called out, but rather the dielectric constant and loss were specified along with the glass transitional temperature, Tg, in order to survive thermal test requirements and meet the final reliability. The Dk specified should be 3.5-4.0, Df of 0.0150-0.005 @ 3 Ghz. The Tg minimum should be 185°C and must be able to pass six solder shock tests @ 288°C without any delamination or blistering. Further the finished board must have four coupons from each panel fabricated tested for IST[1] using the Cray Protocol of 10 cycles minimum from 25°C to 220°C. There would be no allowable defects or deviations from the specifications.

Material Choices

The original choices for materials were BT blends (Bismalimide-Triazine) meeting the original requirements, yet having slightly higher Dk and Df. Two suppliers were using modified BT's and Hitachi proposed using a new laminate developed of a Cyanate ester/thermal plastic blend called MCL-LX67Y. Having a Dk of 3.5 and loss of 0.005, LX-67Y would allow for a balanced construction of 0.004" (0.1 mm) cores and dielectric spacings of 0.002" (0.050 mm). This would allow for line widths and spaces of 0.003" (0.075 mm) and 0.004"(0.10 mm) making the fabrication easier to meet the final impedance criteria, with higher yields.

Testing of Inner layers and Final PCB

Testing for both inner layers and the final PCB requires the use of several different techniques. Automatic Optical Inspection (AOI) is critical for inner layers and also the finished board. However AOI is only one method that is employed and two different types of AOI must be used to capture any defects. First opens and shorts must be found to either remove these inner layers from the stack for final lay-up or repaired. For copper surfaces reflection type is usually used and can detect down to 15-micron size anomalies. The finished board however has several different types of metallization and fluorescence type of AOI must be used. This can detect defects on copper, tin/lead and gold all used on this PCB.

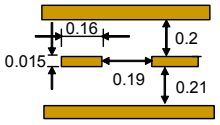
Moreover this will only capture gross opens and shorts. Any types of defects that are not a clear open or short, reducing line dimensions or spacing, another type of test must be used. LAtest is used to find these types of defects and it is used in conjunction with a flying probe electrical design. This will capture any "mouse bites" or even dish downs where the cross sectional area is reduced. LAtest[2] or Latent Defect Test measures the Resistance of the lines (Rdc) reporting differences from known calculated values.

Further the flying probes can also be used to test electrical continuity of the traces and insulation resistance between layers. Yet another test employed is finding high DC resistance vias. All of the Plated through holes are measured to ensure that only known good boards are used in the SMT assembly and, again increase the final board yields through process improvements.

Material Options

Manufacture			Hitachi	Company B	Company C	Hitachi
Material			MCL-LX-67Y	Low Dk / Low Df		MCL-E-65
Material	Dielectric constant (DK)*	at 1MHz	-	3.4-3.8	3.50	3.8-4.0
		at 1GHz	3.48	-	3.40	3.7-3.8
	Dissipation Factor (DF)*	at 1MHz	-	0.0020-0.0024	0.003	0.006-0.008
		at 1GHz	0.0056	-	0.004	0.010-0.011
	Glass transition temperature(Tg)*	TMA	175-195℃	-	-	150-160℃
		DMA	225-245℃	-	210℃	170-180℃
Model	Structure model		#1	#1	#1	#1
	Line width(mm)		0.160	0.160	0.160	0.160
	Line to Line space (mm)		0.190	0.190	0.190	0.190
	Cu surface roughness (lamination)	Rz(μm)	3.0-4.0	0.7-1.2	5.0	0.7-1.2
	Cu surface roughness(mat)	Ra(μm)	0.300	0.300	1.200	1.200
		Rz(μm)	2.400	2.400	8.000	8.000
Electrical performance	Characteristic Impedance(ohm)		58ohm			55ohm
	S parameter(@1GHz)	S11	0.070			0.060
		S21	0.625			0.513
		S31	0.080			0.052
		S41	0.019			0.050
	Tpd(ps/mm) *1	Single	6.69			6.91
		Odd mode	6.69			6.90
		Common mo	6.69			6.92
	Dielectric constant (DK) ((ESD) Calculated by Tpd)	Single	4.03			4.30
		Odd mode	4.03			4.28
		Common mo	4.03			4.32
	Crosstalk	Vb(%)	6.3			5.0
		Vf(ps/mm)	0.012			-0.043

* Values are based on manufacture's catalogue.



Structure model #1

*1: $Tpd=(\varepsilon_o\varepsilon_r\mu_o)^{1/2}$ ·$C=1/(\varepsilon_o\mu_o)^{1/2}$
$\varepsilon_r=C^2/V^2$

1.Test Modeling was performed on SerDes LSI evaluation Board, to characterize RF performance of available materials

Figure 2 - Material Options

Automated Optical Inspection

High resolution AOI

Type	Camtek	Orbotech
	QA station 604-HR	Blaser
Defects	Short/Open	Short/Open
Applicable surface finish	Copper	Copper/Gold/Tin lead
Detecting system	Reflection	Fluorescence
Detection limit (μm)	Min.:15.24μm	Min.:30.48μm
Pixel(μm)	5.08μm	10.16μm
Inspection Method	Design rule and full reference comparison	Design rule and full reference comparison
	Morphology algorithms	Morphology algorithms
Panel dimensions	550x710mm	1016x787mm
Inspection area	535x690mm	610x762mm

Figure 3 - AOI Comparisons

Electrical Testing Options

Applied test parameter

		Test parameters	Equipment	
			Open/Short test	
			Flying probe type	Universal type
OPEN	Open test	Applied voltage	10V	
		Applied current	3mA-30mA	
		NG judgement	> 30 ohms	
	Latent test	---	Applied	
SHORT	Short test	Method	Field measurement	
		Applied voltage	10V	
		Applied current	3mA-30mA	
		NG judgement	< 10M ohms	
	High Voltage test	Applied layers	Between Gnd/S, V/S	Between S/S
		Applied voltage	350V	200V
		NG judgement	< 10M ohms	< 10M ohms

Flying probe type tester

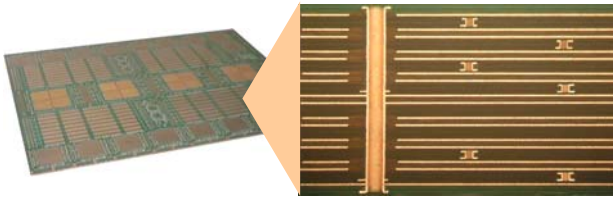


Figure 4 - Electrical Test Options

Automated Test for Rpth

Low resistance TH measurement

Automatic Testing Equipment

Advantage

(1)Resistance measurement with IVHs (Interstitial Via Holes) or PTHs (Plated Through Holes)

(2)High Resolution of 5 aF for Capacitance Measurement (1aF=10-6pF)

(3)Detection of High Resistance Short Circuits with Capacitance Measurement

(4)Four-Terminal Resistance Measurement Function

Probe work area	600 (W) ×500 (H) mm
Thickness	0.6 to 10 mm
Number of steps	40,000 steps (300,000 for continuous testing)

Figure 5 - Rpth Testing

Reliability Requirements of the Finished Product

6x Solder Shock

Many board specifications have specific quality requirements that are taken for granted and are not tested as new part numbers are built. Cray's previous product was a 22-layer board constructed with another material, and had 18-42 mm BGA components on a 1mm grid. This product has been in service for many years. During its production there were solder shocks performed on various regions of the board without any notable issues.

As Cray moved into the current product, there was little urgency to conduct this test in the early stages of development. Because of issues with the bus block attach shear strengths, Cray was required to increase the SMT reflow temperature from 210°C to 240°C and experimented with various solder pastes. At this point it made sense to conduct the IPC solder shock test of 6X shocks at 288°C. Unfortunately, these boards had via to via delamination in the BGA, bus block and MCM areas.

The root cause has not been found to date, although many attempts to eliminate this defect have been tried. Some of the processes tried were additional bakes of 24 hrs and 5 days prior to solder shocking, additional baking during various processes, elimination of thermal reliefs, and maximizing drill size in the relief pads. One of the supplier tried different materials types without any success.

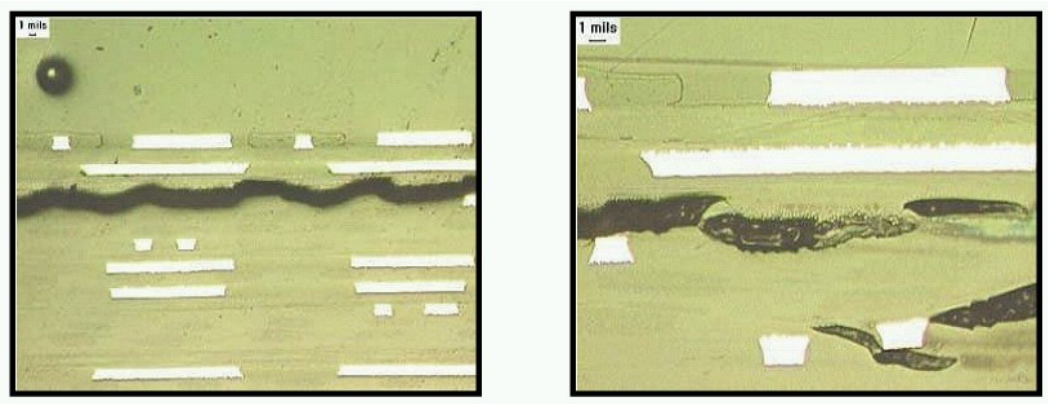


Figure 6 - Solder Shock Delamination of BT /Epoxy Materials

Cray's current material set MCL-LX67Y, made by Hitachi Chemical Co., Ltd, has been subjected to over 18 x cycles and has been in use on our production of both the Node and Router PWBs. It has shown to be the only material to date that can survive the thermal shock requirements and still meet the IST requirements. Further because of the lower dielectric constant of the material set, line widths and spacing could be changed to allow wider trace widths and thicker dielectric spacing between layers; increasing the manufacturing yields and lowering the cost.

IST /CIST Testing

Cray's assembly process requires the bare board to exceed Tg two times. First is an initial reflow of 242°C for 12 seconds with the board remaining above 220 °C for 110 seconds during the bus block attach. Next, SMT reaches a peak temperature of 216°C for 1 second, and stays above 200°C for 40 seconds. Last is the attachment of the 32 edge connectors where localized heating average ~ 40°C for a brief time. The rework cycles for the 42.5 mm BGA sites reach a peak temperature of 212°C; remain above 210°C for 30 seconds, and above 200°C for two minutes.

Traditional Interconnect Stress Test (IST) testing includes running several (3, 5 or 6) preconditioning cycles from 23°C to 230°C, followed by cycling from 23°C to 150°C. This methodology is adequate for lower cost/technology boards and board assemblies, due to the need to understand the impact of assembly and rework conditions, plus understand the influence of the end use environment.

In the case of Cray it was considered that the systems end use environment experienced a low operating temperature delta, reducing concerns related to long term wear out of the interconnect structure. Cray chose to run all IST test coupons from 23°C to 220°C, in order to represent the conditions of multiple assembly and rework cycles. The intention of this testing protocol was to apply high-level strain throughout the interconnect structure and identify the presence of latent failures.

Final Inspection of Coupons

IST

IST Test Equipment

IST condition

Condition	IST Range	Example(1)	Example(2)
No. of samples	1cpn - 6cpns	3cpns	3cpns
Test Temp.	23°C to 260°C	150°C	220°C
Time to Temp.	3 min.	3 min.	3 min.
Time to Cool	Automatic	3 min.	3 min.
Max Res.Change	1-100 %	10%	10%
Number of Cycles	1 – 4000	1000+	42+
Data Collection	Continuous	All Cycles	All Cycles
Test Protocol	Single/Dual Sense	Dual	Dual

Typical IST coupon

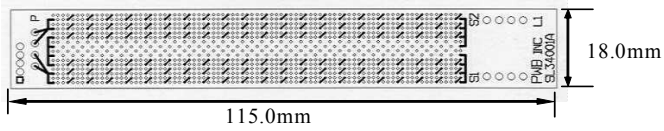


Figure 7 - IST/CIST Requirements

The requirement is to pass a minimum of 10 cycles, without exceeding a 10% resistance increase within the various interconnect structure test circuits. The coupon design included 3 primary structures, which would be stressed simultaneously to determine the hierarchy of failure. The 3 independent circuits include Plated Through Vias (PTV), Buried Vias and the internal interconnect between the copper foils and PTV barrels, located in the upper and lower region of the substrate. During each thermal cycle (heating and cooling) the resistance of all circuits is continuously measured and compared to the initial resistance profile, once failure is determined in 2 of the 3 circuits the testing is stopped.

Following IST testing a report is generated which identifies the performance of each circuit within the coupon. Thermo-graphic analysis (Infra-red imaging) is utilized to identify the locations of specific failure sites; micro-sections can be taken to understand the root cause of coupons failing to meet the minimum criteria. The hierarchy of failure has identified that PTV barrel cracking is the dominant failure mode followed by the internal interconnect (due to pad rotation), the buried vias have proven extremely robust throughout the history of testing.

The graph below shows IST test coupon first failure data for the X1 node boards. The data fits a lognormal distribution with a mean of 20.67 cycles and a sigma (shape parameter) of 0.26. Well over 1,000 coupons have been tested to date, but only 462 samples were included in the graph over a ten-month period of time.

IST test coupons are designed into the borders on all production boards. Each board has four to six test coupons that have a drill hole size of 10-12 mils for PTH vias and 5.9 mils for buried vias. The vias and PTH have a copper plated wall thickness of 0.7 to 1.2 mils. Because Cray uses three different board suppliers, they allow the use of different types of interconnect stress tests.

One supplier used different metallurgies for each of their coupons; copper, electroless nickel electroless gold, electroless nickel electroless palladium, and 63/37 tin lead. Results of the testing are limited and will not be addressed in this paper.

All coupons that fail prior to 10 cycles are cross-sectioned by the suppliers, and failure analysis is conducted. Since production started there have been only 4 boards with coupon failures at our 10 cycle criteria. Two were misregistered via to pad only in the coupon area; the board was acceptable for use. Two were caused by resin cracks and radial micro cavities.

The supplier scrapped these boards. After failure analysis it was determined that these defects were process related and changes were made to ensure reliability in both the drilling and desmear process. Although present in the PWB as seen in Figure 9, they were further subjected to solder shock at 260°C and still at 288°C for 6 times. The micro cracking in the resin did not propagate into the structure and were not progressive in nature. A post drill baking cycle was added and eliminated this problem from future manufacturing lots.

The radial micro cavities were found to be a plating issue, where the thickness of the copper plating had very small cavities and therefore very thin plating. This also was process related and corrections were made to the plating process without any further failures.

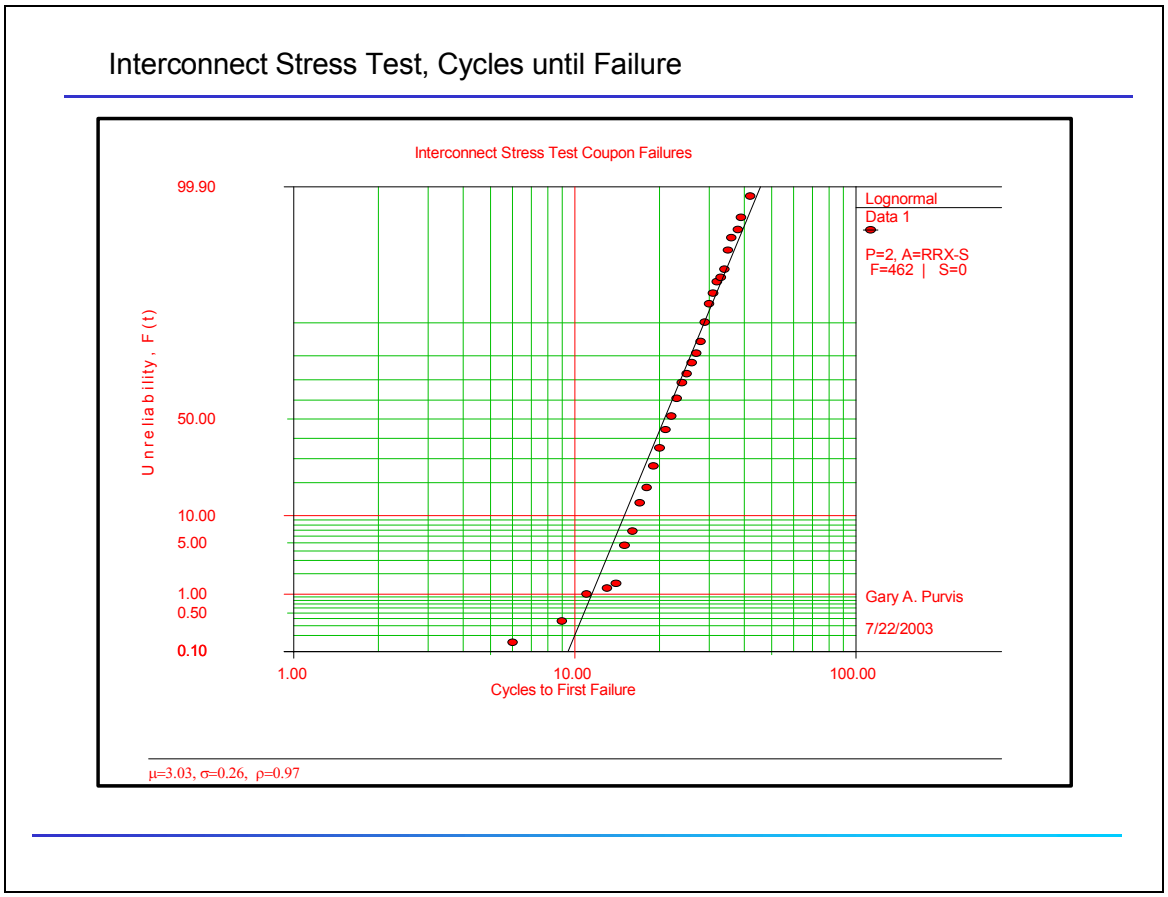


Figure 8 - IST Lognormal Results

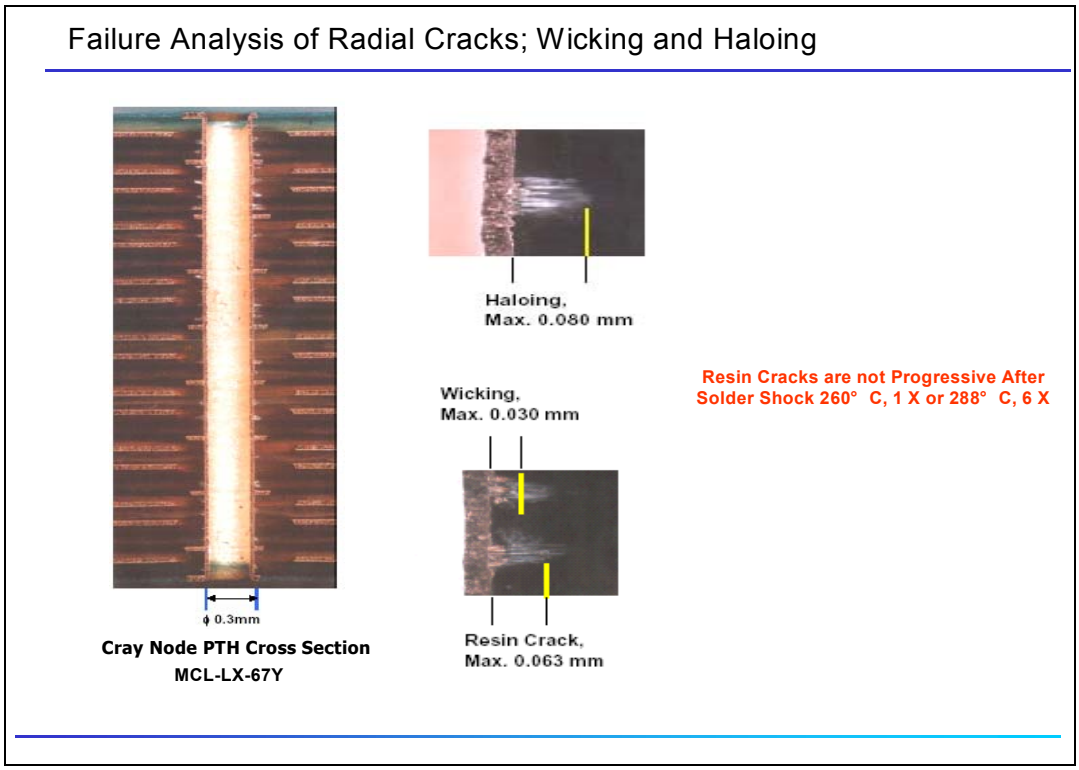


Figure 9 - Failure Analysis Micro Cracking

Figure 10 - Cray X1 Super Computer

Summary

From the launch of X1 Cray has built over 600 assemblies and is extremely satisfied with the performance and reliability of the newest systems. The overall theme used on X1 has been a success. In the past with Military specifications and OEM's over specifying materials and process' to be examined and tested, cost has been a huge factor and has not added to the overall improvement in quality or reliability. By allowing the supply base to choose the appropriate materials, based upon the system requirements, electrical, mechanical, and thermal, Cray has found testing the final product does indeed add to the final quality and achieves the Extreme Reliability they have set out to gain.

References

1. IST, Interconnect Stress Test, used under License from PWB Interconnect Solutions, Inc., Ontario, Canada.
2. LAtest was developed and used under License from IBM, Corporation.
3. Special thanks to Dave Peterson, Elliot Schlimme, and John Burlin-Burns, Cray, Bill Birch, PWB Interconnect Solutions, Inc.