Imprinted Interconnects Technology (I^2T), a Revolutionary Method for the Production of Very-High-Density Interconnects (VHDI)

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Abstract
Today's HDI field of technology is coming under more and more pressure to increase wiring density and, even more importantly, to decrease manufacturing costs. The current technological approach does not permit an adequate response to this challenge and thus new, disruptive manufacturing technologies have to be developed.

Imprinting as a means of forming conductor patterns as well as via holes has been under discussion for several years now. A more crucial issue, however, is to find a method for filling the recessed features reliably and inclusion-free with solid copper, and consequently the overall build-up concept has to be adapted in order to utilize the full potential of this novel technique. This paper describes a new manufacturing approach based on imprinting, a special copper plating process, followed by an etch-back step. This method is capable of producing lines and spaces down to 10µm and thicknesses of up to 40µm. Conductor and via pattern are produced simultaneously, thus making padless designs feasible.

The key elements of this radical new approach are the manufacture of the imprinting stamp, the imprinting itself and the copper filling. Each necessary process step has been verified in a lab environment, and first functional samples have been successfully produced. Continuing further development is underway to bring this technology from lab to fab within a reasonable timeframe.

Introduction
Since the birth of modern PCBs in the late 60s of the last century, the related basic manufacturing processes, instead of changing dramatically, developed slowly but steadily towards more stable materials, finer holes and conductor features, an increased number of conductor layers, higher yield and hence lower manufacturing costs. Even a remarkable event like the transition from THT to SMT was accommodated by the PCB industry without major adjustments.

In the early 90s, when array packages with higher pin counts were introduced, pressure on conventional technology increased considerably and triggered the development of new drill processes with microvia capability. The use of microvias with low aspect ratios led to new build-up architectures, based on conventionally made multilayers that are sandwiched between two or more microvia layers.

Today, the PCB manufacturing industry is being challenged by the widespread use of array packages with constantly decreasing I/O pitches, and microvia technology has almost no leeway left for responding to this challenge except by enabling a further increase in the number of layers. Conductor width and spacing are approaching the limits of the standard photo-definition and subtractive-etching processes. The smallest microvia diameter is given by the filling capability of the copper metalization process, and the via-pad size still needs to be large because it is determined by the alignment accuracy of the drilling and registration processes.

In summary, progress in manufacturing-cost reduction is coming to a standstill and no satisfactory response to future requirements is possible without switching to fundamentally new technologies.

Imprinting combined with an appropriate copper-filling process has to be considered as such a new, disruptive technology, which not only improves the individual process steps but also changes the manufacturing process in its entirety.

Technology
History
Imprinting is a well known technology that has been used in various fields for many years, as well as thoroughly discussed in the PCB community. The process of imprinting seems to be well understood and not overly crucial, provided that proper imprinting tools and appropriate substrate materials are available. However, the imprinting process itself enables, but does not alone constitute, a production technology. Filling the resulting micro-relief with copper at the required degree of long-term quality, as well as developing pattern designs in such a way that reliable circuits result, are additional key processes to be addressed. As in many cases, when a technology approaches its limits, a new breakthrough is not found by a member of

the community, but more likely by an outsider who has an unbiased view of the problem. Elmicron's technological background is in the production of microparts by means of UV-LIGA and electroplating of nickel and other metals – technologies that provide the toolset for the production of imprinting tools, as well as the Cu-filling of imprinted micro-relief structures.

The I^2T-Process

Although, the imprinting process can be applied to virtually any build-up construction, its potential can be utilized best when thin base materials with a thickness of between 25 and 125µm are processed, because imprinting-tool manufacturing limits the maximum height of the pins used for through-hole formation. With regard to thicker substrates, although this technology can still be used for imprinting conductor traces, a conventional technology must be utilized for the subsequent formation of via structures. The following description is based on the assumption that a thin, unreinforced dielectric material is used, e.g. a bare polyimide or LCP film with a thickness between 25 and 125µm. For a double-sided imprinted film with through-via, the basic process sequence is shown in Figure 1.

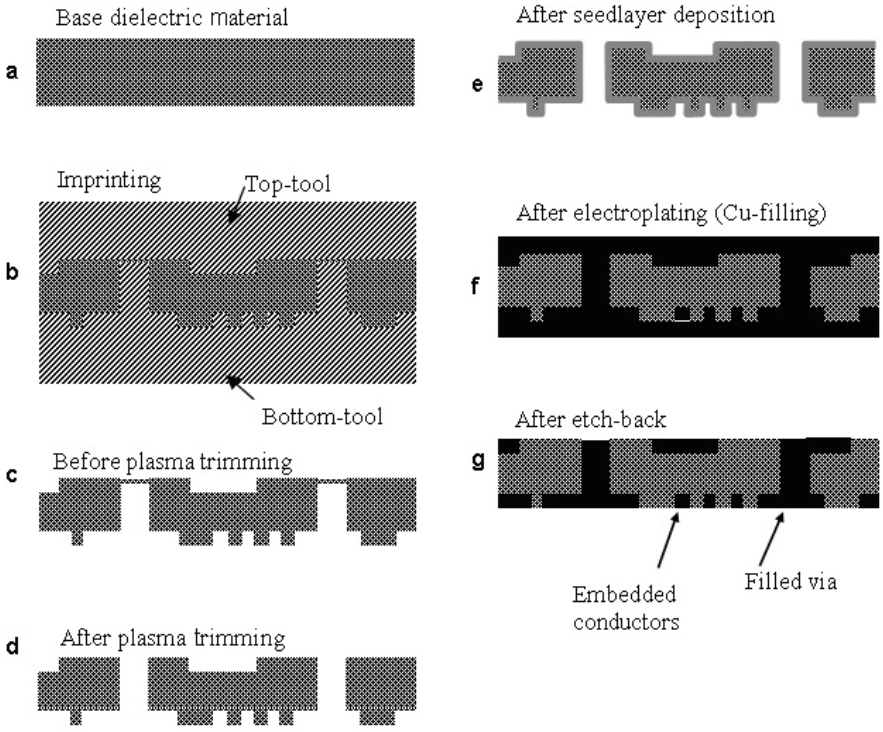


Figure 1 - Basic Process Sequence

The film is placed between the imprinting tools, which have to be precisely aligned with each other (1a). The tools are heated to the required temperature (200°C to 300°C, depending on the material used) and pressed together. The film becomes soft and conforms to the stamps. Then the stamps are cooled to below the glass-transition temperature of the film material, and the imprinted film is ready to be demolded (1b).

As shown in Figure1b, the bottom stamp contains the conductor traces on a first layer, as well as pins for the microvia formation on a second layer. Both patterns are imprinted simultaneously. Here, the top tool consists of one layer only, containing the conductor lines of the top layer and landing targets for the microvias. The size of the landing targets is determined by the alignment accuracy of the press system, and it can be in the same order of magnitude as the conductor width. Another option is to use two-layer tools on both sides and form the through-via by imprinting pins from top and bottom simultaneously.

A short plasma-trimming process (1c) is used as a surface pretreatment to ensure good adhesion of the subsequently deposited metal layer. At the same time, the plasma removes the remaining thin plastic membrane between the via-formation pin and its counterpart (landing target or via).

The subsequent seed-layer deposition (1e) can be accomplished either chemically or by means of a vacuum process, depending on the dielectric material used.

A proprietary electroplating process follows, which is capable of filling the imprinted conductor channels, pads and through-vias inclusion-free with copper. This plating process is optimized to give a considerably higher deposition rate within narrow grooves, caves and holes. Usually, when filling a 30µm-deep conductor channel with copper, only about 6-10µm are deposited on the top surface (1f).

To arrive at the final conductor pattern, a simple chemical etch-back process is applied to remove all electrical shorts between the lines, leaving the recessed copper almost unaffected (1g).
Typical feature dimensions of today's imprinted substrates are conductor width: 20µm; thickness: 30µm; spacing: 20µm; via diameter: 40µm – and the technology's limits have yet to be reached, as can be seen from Figure 4b showing a line width/spacing of 12.5µm. Figure 2 shows a detail of an imprinted, copper-filled and etched-back substrate with 25µm-wide (1 mil) trenches.

Figure 3a shows a cross-section of imprinted and copper-filled traces before etch-back. For the optimized growth behavior to be visualized, the plating process was interrupted three times to show snapshots of the corresponding solid-liquid interfaces. The 38µm deep channels are completely filled, while the overall cladding is roughly 6-8µm thick.

Figure 3b shows a cross-section with lines having a width of approx. 28µm and a gap of approx. 7µm after etch-back for a microcoil application. These photographs provide an impression of the capability of this imprinting process. The replication accuracy is excellent, assuming that proper imprinting equipment and tools are used in combination with a suitable dielectric material.

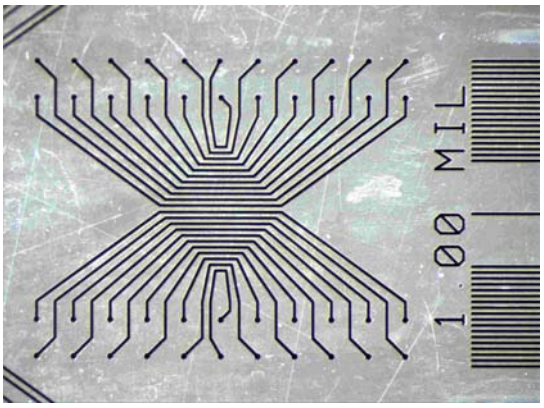
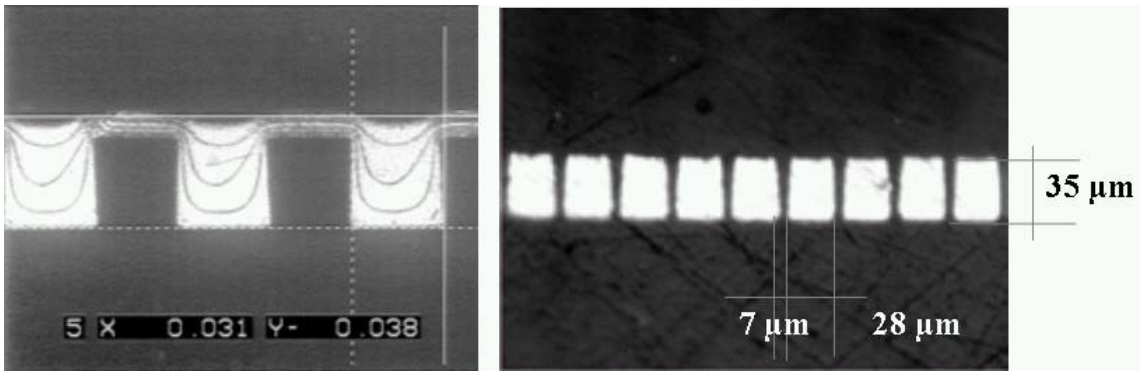


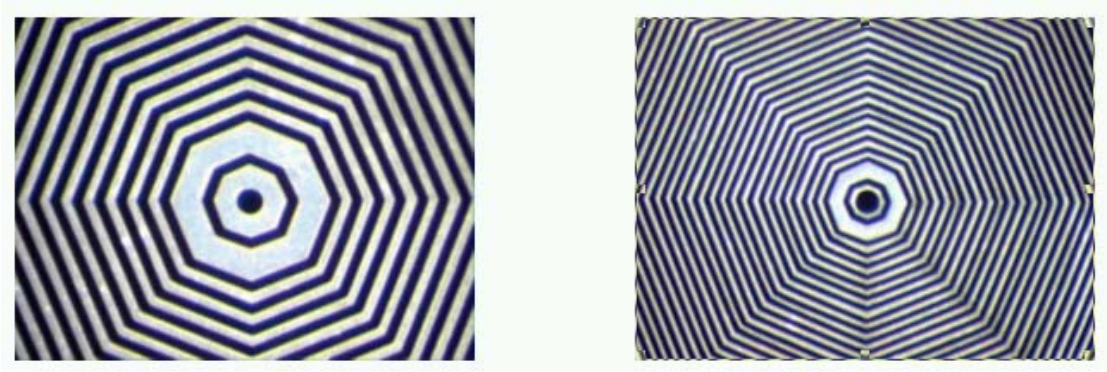
Figure 2 – Imprinted Substrate after Copper-filling and Etch-back



a b

Figure 3 – Cross-section of Copper-filled Channels Showing a) the Growth Dynamic, b) Channel Spacing of Approx. 7µm.

Figure 4 shows a finished substrate with a) 25µm and b) 12.5µm lines and spaces. The photographs clearly verify the fine-line capability of I^2T, as well as the excellent edge definition of the conductor lines.



a b

Figure 4 – I^2T Substrates with a) 25µm and b) 12.5µm Lines and Spaces

Imprinting Tool (Stamp)

The microtools used for imprinting are manufactured by means of the UV-LiGA process and nickel-plating, as shown schematically in Figure 5.

Today, lithography is done on a 6-inch wafer line. Currently being developed are new manufacturing processes that will extend the stamp size to full panel and, going forward, reduce the related manufacturing costs.

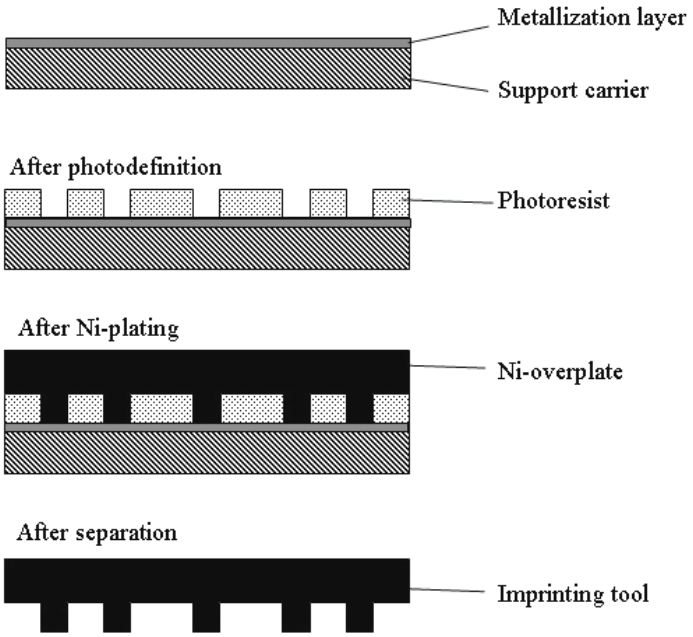


Figure 5 – Process Sequence for Manufacturing Imprinting Stamps

I^2T Build-up architectures

The achievable maximum wiring density is basically limited by the size of via pads and the line pitch. Because microvias are imprinted simultaneously with the conductor pattern, the design can be nearly padless. With lines and spaces around 20µm, a 2-layer design is capable of addressing almost 100% of all possible applications. For instance, this technology enables more than 3000 I/Os of a BGA with a pitch of 0.8mm to be fanned-out on one single layer. With additional PWR and GND planes as the outer layers – which may also include all necessary assembly pads – a 4-layer build-up as shown in Figure 6 is achieved. Containing only coarse features, the outer layers are manufactured using standard techniques. Signal lines can then be connected to the outer layers by means of conventionally laser-drilled microvias.

The 4-layer build-up construction can easily be extended to accommodate more complex architectures, including those that have multiple cores with or without through-connections

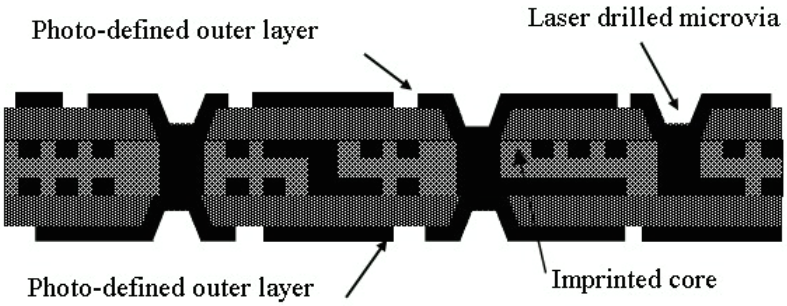


Figure 6 – 4-Layer Build-up with Imprinted Core

Advantages Versus Established Technologies

The potential of this new technology is evident and the benefits are manifold:

- Very high connection density due to ultra-fine patterns
- Padless design by simultaneous formation of conductor and via pattern (Figure 7)
- Even surface and easier lamination due to embedded structures
- Self-alignment of components due to recessed trenches
- Minimum number of layers thanks to high wiring density
- Improved HF – performance the result of excellent edge definition, shorter lines and fewer through-vias
- Good heat extraction due to thin build-up
- Any application from full-flexible to rigid thanks to flex-based technology

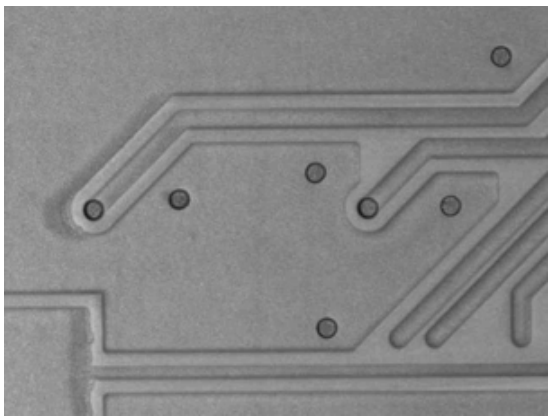


Figure 7 – Close-up of an Imprinted Substrate with Padless Design

Economic aspects:

- The number of processing steps is significantly reduced. Photo-definition and drilling are eliminated.
- Parallel single-shot process for the conductor and microvia generation
- High potential for automated manufacturing
- Savings in material consumption

Environmental aspects

- Less material consumption
- Less chemical waste
- Fully recyclable base materials

Areas of application

In an early stage, this imprinting technology will most likely find application in mainly performance-driven segments of the PWB and semiconductor packaging industry, where the requirements for saving space and weight predominate.

An initial example has been developed in the form of a PWB, packed with multiple BGAs, in which the number of signal layers was reduced from 6 to 2 through redesigning in accordance with the design rules of I^2T while maintaining the same functionality.

Applications that fall into this category include probecards for wafer testing, as well as medical applications such as hearing aids and pacemakers.
Other particularly high-volume applications, in which cost savings are the sole focus of attention, will be addressed at a later stage when the technology has reached a higher degree of maturity and is ready for volume production.

Summary
By combining imprinting technique with a galvanic deposition of copper and a planarization process, the described technological approach is an attractive candidate for complementing or even supplanting conventional production technologies for HDI. In the long run, this technology – thanks to its technical, environmental and commercial advantages – may even set the standards for future interconnect production.

The key processes of I^2T – the imprinting-tools production, the imprinting itself and the copper plating – have proven their feasibility at the lab level and are currently being developed further to accommodate high-volume production.

On its path to higher-volume capability, Elmicron will be working jointly with members of the PCB community.