Trimming Embedded Resistors

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Introduction

The increased need for smaller, faster, and cheaper electronics has led the microelectronics industry to explore a number of new enabling technologies. Embedding passive components into multi-layer printed circuit boards offers the potential to deliver a number of benefits, including saving valuable board surface area, increasing performance, reducing manufacturing costs, improving reliability, and providing opportunities for less expensive substrate materials. As PCB manufacturers embrace this technology, and as requirements for tighter tolerances become more necessary, laser trimming for these components will also become necessary, prompting manufacturers to add embedded passives trimming equipment to their current manufacturing process. Technology for trimming embedded resistors has been recently demonstrated for production applications[1], and the industry is beginning to look more closely at cost models. Cost models are currently available,[2,3] presenting a general overview of the costs, and allowing for comparisons to alternative surface mount technologies. This paper will discuss the process of laser trimming embedded resistors in a production environment, and will investigate the process cost of ownership.

Trimming Resistors on a Large Panel Format

Due to variations in resistor formulations and substrates that are used for printed circuit boards, tolerances of less than +/- 10% are challenging for the industry to achieve in the current embedded passives environment. However, in order to reach consumer demands for "smaller, faster, cheaper", embedded resistor tolerances must be better than +/- 10%. Trimming is a solution to these issues, and laser trim techniques can provide tolerances to better than 1%, over a wide range of materials.[4]

To process a laser trim, the resistor of interest is connected to a high-speed measurement system via a suitable probe system, and a laser is directed to machine a cut through the resistor thickness in a direction generally orthogonal to the current flow (Figure 1). As the laser cut forms, the measurement system detects a decreased current flow relative to applied potential, and interrupts the laser radiation when the desired resistor value (Ohm's Law; E = I * R) has been reached. Application of this technology is very well understood as applied to trimming resistors on ceramic substrates in hybrid circuits and mass production of "chip resistors" for conventional surface mount technology.[5]

A number of diverse materials have emerged as candidates for embedded resistors, as shown in Figure 2. Each material provides various tolerances due to alignment of screening, placement of resistors, and uniformity of material, such as thickness and resistivity. The inherent process tolerances can be approximated by a sum of component tolerances as shown in Table 1.[6,7]

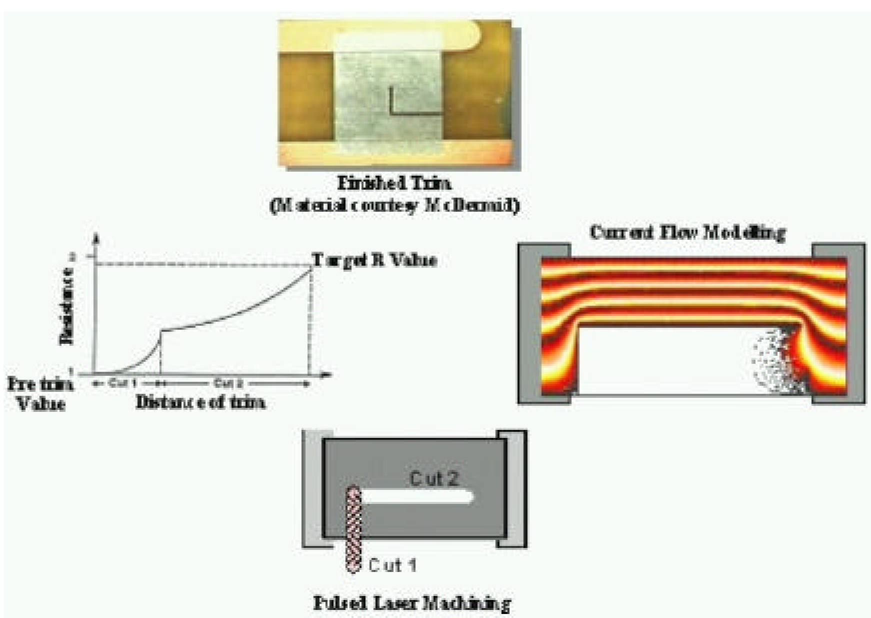

Figure 1 - Laser Trim Basics

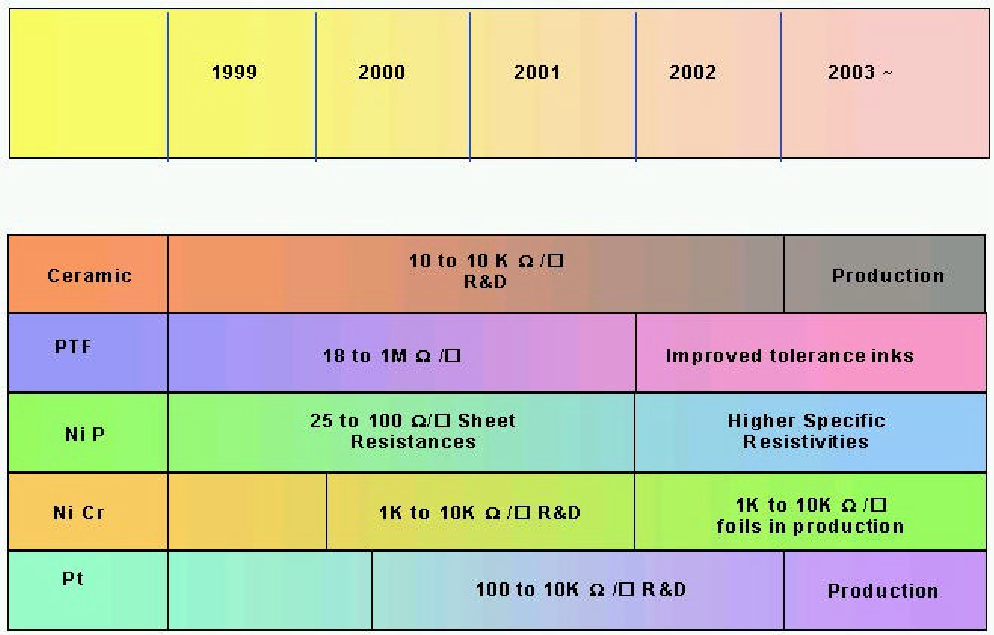

Figure 2 - Resistor Technologies Roadmap

Table 1 - Sum of Errors for As-Formed Resistors

Resistor Type	Specific Resistivity	Thickness	Resistor Geometry	Copper Geometry	Total
Polymer Thick Film	1%	5%	1~5%	5%	12~16%
Metal Thin Film	1%	3%	1~5%	5%	10~14%
Thin Film on Foil	1%	1%	1~5%	5%	8~12%

The geometry of the etched copper may be a limiting factor in determining the final as formed resistance values for all material cases. This value of 5% is a fundamental result of line width tolerances and general etching accuracies of copper features on the inner layer panels. Plating or printing of the resistor materials can be achieved to similar tolerances of 1~5%, while the chemically dependent specific resistivities of the various materials are generally very good at 1~2%. Thickness variations can be large at 1~5% within localized areas, or over the complete panel. By summing all the components, total process errors of 8~16% are predicted for as formed resistor tolerances.[8]

Trim Process Throughput and System Component Utilization

A laser based resistor trimming system has several component processes contributing to the overall process throughput. (See Figure 3.) In general terms, these may be described as:

1. Panel unload and load
   The processed panels are exchanged for fresh panels either manually, or with an autoloader. Manual exchange is typically an order of magnitude slower than the autoloader process, but may be acceptable depending on the overall processing time per panel.
2. Panel alignment
   A panel alignment procedure is required to maintain positional accuracy throughout the step and repeat processes. A manual alignment procedure is possible, but is typically several orders of magnitude slower than an automatic panel position and theta compensation process.
3. Circuit alignment
   An automated circuit alignment procedure helps to maintain probe to pad placement accuracy in a production application. Depending on pad sizes and circuit complexities, the circuit alignment procedures may involve pattern recognition controlled compensations in x, y, and Θ.
4. Galvanometer resistor-to-resistor movement
   The time required to reposition the laser from the end of one cut to the start of next cut on sequential resistors becomes very significant when the resistor count on the circuits increase.
5. Resistor Trim
   The speed at which a laser cuts resistor material is determined by the laser repetition rate (QR, in pulses/second), and the pulse bite size (BS, spot size diameter in µm). Some types of interactions between the laser and resistor or substrate materials may limit the repetition rate. Thus a thermal coefficient of resistivity (TCR) may require relaxation time to ensure accurate resistance measurements at a constant temperature, material deliquescence may lead to mechanical defects such as fractures or mini-eruptions, high relative ablation thresholds may require laser power that is damaging to the

underlying substrate, similar optical absorption coefficients for the resistor material and substrate will make it difficult to remove resistor material without concomitant substrate damage. Generally, the resistor thickness determines the appropriate bite size, as thicker resistors may require a smaller bite size to increase the amount of overlapped pulses. The time to complete a trim (Equation 1) also considers the trim length (L, total cut length in µm) as a function of the resistor size, and selected trim shape.

$t = L / (QR * BS)$ ……………………..(Equation 1)

6. Panel movement (S&R)
   Positioning circuits of a large panel relative to fixed lens and probe systems requires exacting control of a large fast moving mass. The time required to change circuit positions can be significant, and optimal throughput is usually obtained with minimized panel moves.

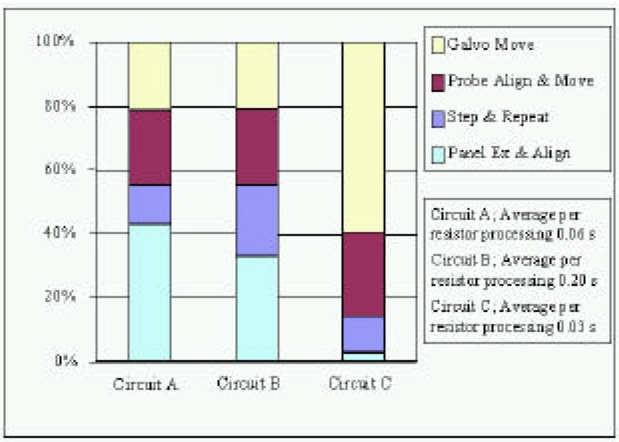

Figure 3 - Laser Trim Component Process Contributions to Throughput; Circuit A; 72 Resistors, 48 up on a 12" x 16" Panel - Circuit B; 25 Resistors, 12 up on an 18" x 24" Panel - Circuit C; 3500 Resistors, 9 up on a 16" x 20" panel

Typically, a production process should be "bottlenecked" by the most critical process or system. Intuitively, the laser trim total process throughput should thus be dominated by the actual resistor trim time as determined by laser galvanometer moves, although the relative contributions from each component process are highly dependent on resistor layout and circuit design.

Integrated Test
A dedicated measurement system, as required to control laser beam position during trimming, conveniently minimizes scrap and rework costs by performing real-time electrical tests before, during, and after laser processing. Thus, initial and final resistor values are readily available, and the appropriate laser parameters can be confidently discerned to ensure that final tolerances are met. Even with high TCR materials, resistors can be trimmed to tolerance with a judicious choice of trim speed. While zero over trim can be confidently avoided, deliquescence, differential optical absorbance, and ablation thresholds need to be carefully considered to avoid electrical issues stemming from mechanical delamination and substrate damage. However, decades of experience in hybrid circuit trimming has shown that integrated test and trim will provide a high yield of known good parts.[4,5]

Trim Results
A wide variety of materials and resistivity ranges have been trimmed, including but not exclusive to polymer thick-films, ceramics, and metal thin-films. Some, but not all of these materials were made available from MacDermid Inc. and Dupont i-Technologies through the Advanced Embedded Passives Technologies Consortium, with the data published elsewhere.[9,10] Typical samples were single layer FR4 large panels (12" x 16" to 20" x 24"), with multi-up boards, and resistor counts of 100 to 10,000 per panel.

A summary of test and trim data for two different resistivity polymer thick films is provided by Table 2. In both cases, the pre trim nominal values were about 15 ~ 20% lower than target, but they were readily trimmed to within 1 % of target (3σ for a dataset of 1137 resistors on a single panel). Accounting for offset and distribution errors, both resistor sets were trimmed to value with final Cpk values greater than 2.0 at 1% tolerance, and greater than 10 at 5% tolerances.

Table 2 - Pre Test and Post Trim Data for Carbon Loaded Poly Epoxy Thick Film Resistors

Statistical Parameter	R1	R2
N =	1137	1137
Target =	70.0 Ω	3900.0 Ω
Average Initial Value =	57.2 Ω	3346 Ω
Average Final Value =	70.1 Ω	3888.8 Ω
Initial Error =	18.3%	14.2%
Final Error =	0.19%	-0.29%
Final 3 σ=	0.3%	0.2%
Final Cpk 1 % =	2.416	3.045
Final Cpk 5 % =	14.338	20.164

As with the polymer thick film resistors, thin film resistors can be readily trimmed to within 1 % tolerances; however as Figure 5 illustrates, laser trim can be used to increase resistance values only. As a result, effective use of laser trim requires that nominal pre trim resistance values are all lower than the target values. Typically, the targets for as plated or as printed resistors should be 15 ~ 20 % below the final desired values (depending on process distribution, see Table 1 and Figure 4 for examples) to allow laser trim to bring all resistors to value within tolerance.

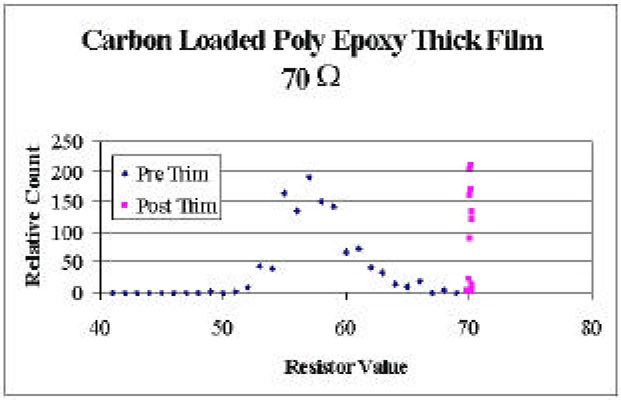

Figure 4 - Pre and Post Trim Distributions for 70 W Polymer Thick Film Resistors

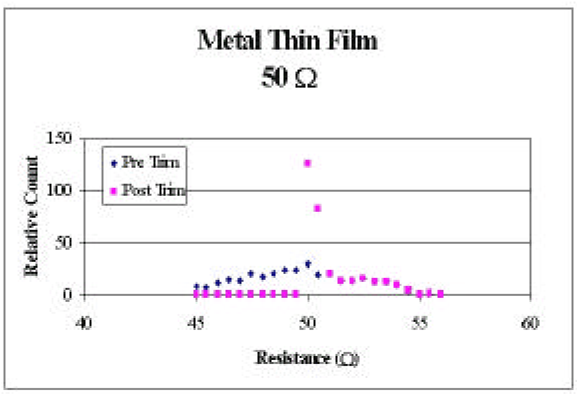

Figure 5 - Pre and Post Trim Resistance Values Metal Thin Film Resistors

Cost of Ownership Model

While laser trimming of resistors on hybrid ceramic substrates is well known,[4,5] laser trimming of resistors on large panel organic substrates is less practiced and less understood. Acceptance of the laser trimming process applied to surface printed or embedded resistors on large panel organic substrates may be dependent on understanding a specific application of the general Cost of Ownership model as in Figure 6.

The generally accepted models for Cost of Ownership tend to be of the form:[11,12]

$$COO = (C_F + C_V + C_P + C_Y) \qquad \text{(Equation 2)}$$

where the component terms expressed per unit are

C_F = fixed cost,
C_V = variable cost,
C_P = processing cost,
C_Y = yield cost.

Fixed Costs are derived from original purchase of equipment, interest on capital, corporate overhead (i.e. floor cost), installation, and training. Variable Costs include labor, consumables, periodic maintenance, and demand utilities (such as power). Processing Costs arise from throughput and utilization considerations, such as processing rates and equipment availability relative to the standard fab operation. Less tangible, but significant is the Yield Cost resulting from the effects of scrap and rework.[13]

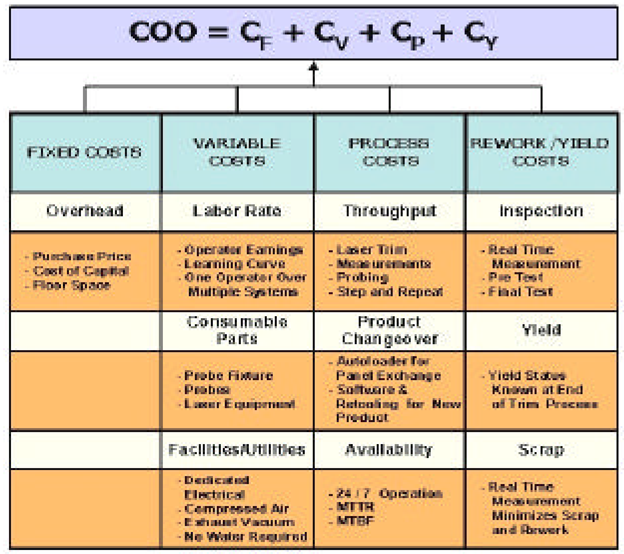

Figure 6 - Cost of Ownership Model for Resistor Trim on Large Panel Format

Cost of Ownership Results

With representative data from several sources, a cost of ownership model has been used to determine the relative impact of several general and specific factors on the cost of laser trim per unit resistor. Figure 7 depicts a typical series of normalized cost sensitivity curves for a specific product circuit design (100% nominal represents a system operating under typical conditions), where it becomes evident that the per unit trim costs are dominated by specific processes such as system utilization, panel format and circuit layout, and to a lesser degree, throughput. The model also predicts that the per unit trim costs are relatively insensitive to fixed and variable costs such as capital, labor and facilities costs. With a circuit designed in consideration of the need for laser trim, the overall cost of laser trim can be less than $ 0.001 per resistor.

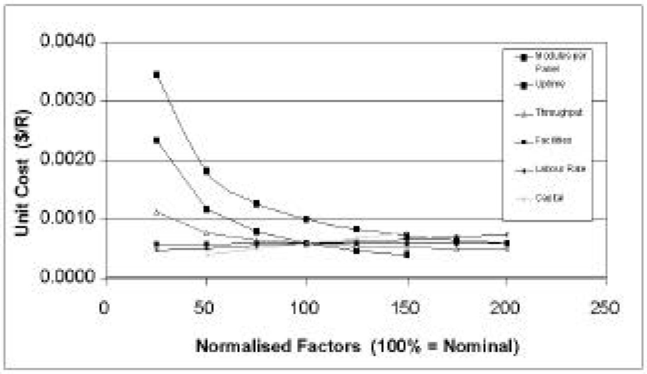

Figure 7 - Cost Model Sensitivities

Conclusions

Equipment and methodologies have been developed to accurately adjust values of embedded resistors on inner layer panels prior to board lamination. The laser based trim process has been evaluated over a wide range of potential materials, and has been shown to provide better than 1 % tolerances on final values for resistors based on polymer thick films, metal thin films, and ceramics.

A cost of ownership model has also been developed with consideration of several factors for laser trimming of resistors printed on large format organic substrate panels. This model has been used to demonstrate the cost effectiveness of the trim process in a production environment.

Acknowledgement

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References

1. Kim Fjeldsted, Stacey Chase. “Embedded Passives: Laser Trimmed Resistors.” *CircuiTree*, **March 2002**
2. P. Sandborn, B. Etienne, D. Becker. “Analysis of the Cost of Embedded Passives in Printed Circuit Boards.” *Proceedings of the IPC Annual Meeting (Orlando, FL)*, **October 2001**
3. M. Realff, C. Power. “Technical Cost Modeling for Decisions in Integrated vs. Surface Mount Passives.” *Proc. IMAPS 3rd Advanced Technology Workshop on Integrated Passives Technology (Denver, CO)*, **April 1998**.
4. Visit Electro Scientific Industries at www.esi.com for more details.
5. R. Dwight, P. DeLuca, Y. L. Sun. “Trimming.” *Laser Institute of America; Handbook of Laser Materials Processing* J.F. Ready (Editor) **2001**.
6. G. Lucas. “Fundamentals of Buried passive Components.” *Proceedings of the IPC Annual Meeting, (Orlando FL)*. **October 2001**
7. J. Wang, R. Hilburn, S. Clouser, R. Greenlee. “Manufacturing Embedded Resistors” These proceedings.
8. Tolerance capabilities may vary somewhat with material and process experience
9. J.J. Felton, W. J. Borland. “Embedded Ceramic Passives in PWB’s: Process Development” *IPC Printed Circuits EXPO* **April 2001.**
10. Visit the Advanced Embedded Passives Technology consortium at http://www.aept.ncms.org for more details
11. T. Niebeling. “COO for 300mm FOUPS” *Solid State Technology*, **August 2001**
12. A.F. Schreiner, N. Hofmann, K. Phillips, R. Kumar, B. Varnell, D. Bedner, J. Carlton. “Comparison of Laser Processes for Microvia Formation in RCF, FR-4, and ‘Thermount.’” *PC Fab* **April 2002.**
13. P. Sandborn, “An Assessment of the Applicability of Embedded Resistor Trimming and Rework” submitted to *IEEE Transactions on Electronics Packaging Manufacturing*, **August 2002.**