Fundamentals of Buried Passive Components

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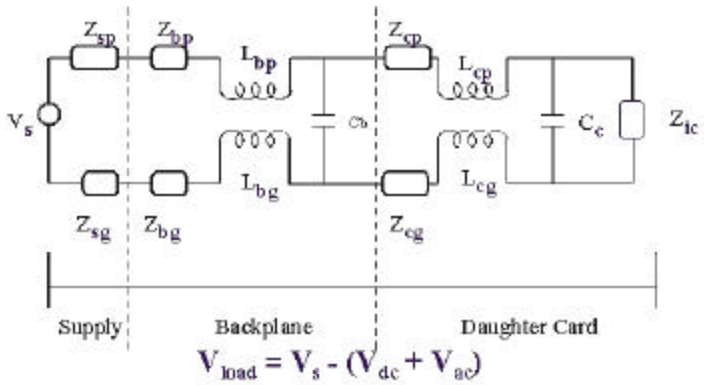
Abstract
Several factors are driving the need for buried passive components in printed circuit boards and chip carriers. Increasing frequency increases the difficulty in quieting noise by the use of surface mounted discrete capacitors and resistors. Decreasing voltage makes transmission lines more sensitive and signal integrity more difficult to maintain. Increasing power consumption by silicon devices drives the need for lower inductance, and higher capacitance power distribution in close proximity to the to the silicon device. A larger number of active silicon devices per unit of surface area decrease available space for passives.

Buried Distributed Capacitance
Figure 1 below depicts a lumped element diagram of a typical electronic system. Starting at the left, there is an input power supply V_s. Along the top of the diagram, we find the supply power bus impedance, Z_{sp}, the backplane power bus impedance, Z_bp, the power plane inductance, L_{bp}, the backplane interplanar capacitance, C_c, the daughter card power plane impedance, Z_{cp}, the card power plane inductance, L_{cp}, and the card interplanar capacitance, C_c, and finally the load or active silicon device. Tracing across the bottom portion of the diagram we find the same elements for the ground bus structure. Not depicted are the dc resistance elements, which also exist for each of these segments.

The following equation defines the voltage, V_{load}, needed to fire the device Zic shown in Figure 1.

We are assuming a perfect connector to keep things simple.



$$V_{load} = V_s - (V_{dc} + V_{ac})$$

$V_{dc} = I_{dc}(R_s + R_b + R_c)$ = the dc voltage drop through the system.
I_{dc} is the dc current
R_s is the source resistance
R_b is the backplane resistance
R_c is the card resistance

$V_{ac} = I_{ac}(Z_s + Z_b + Z_c)$ = the ac voltage drop through the system with corresponding impedances relating to each section of the system.

Figure 1 – Lumped Element Diagram of a Typical Electronic System

As our system is currently structured when the device calls for power it must come through all these obstacles to get there. If we assume this is a device with bus frequency at 100 megahertz it will not get what it needs and it will not send out a proper signal. The energy it needs will be lost along the way, some of it radiated as noise.

When the device calls for power it needs that power through a spectrum of frequency reaching into the gigahertz region. Our system as currently structured will deal only with the very low frequency portion of that spectrum. The remedy for this problem in the high frequency region is to add a decoupling (bypass) capacitor near the device as in Figure 2. Decoupling capacitors and the inherent (parasitic) inductance in the circuit act together in a frequency dependent manner.

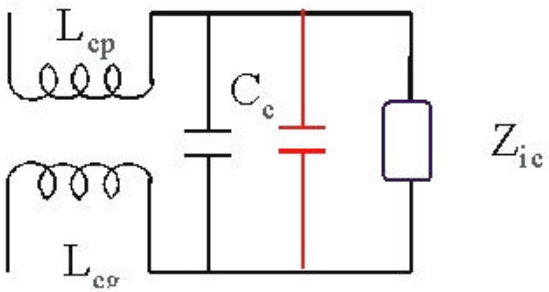


Figure 2 – Decoupling (bypass) Capacitor

The impedance in the circuit between the device and the SMT capacitor is given as:

$$Z_{cap} = \sqrt{R_{cap}^{\ 2} + X_L^{\ 2} - X_C^{\ 2}}$$

$$R_{cap} = \text{DC resistance}$$

$$X_L = 2 * \pi * f * L_C = \text{Inductance Reactance}$$

$$X_C = \frac{1}{2\pi * f * C_C} = \text{Capacitance Reactance}$$

$$f = \text{frequency}$$

Notice that inductive reactance is proportional to frequency and capacitive reactance is inversely proportional to frequency. Assuming that the dc resistance is reasonably low the impedance at high frequency will be essentially the inductive reactance. In Figure 3, we see graphically how the impedance has a low (resonant) frequency for each different capacitor value and then "rolls up" with increasing frequency; therefore is dominated by inductive reactance.

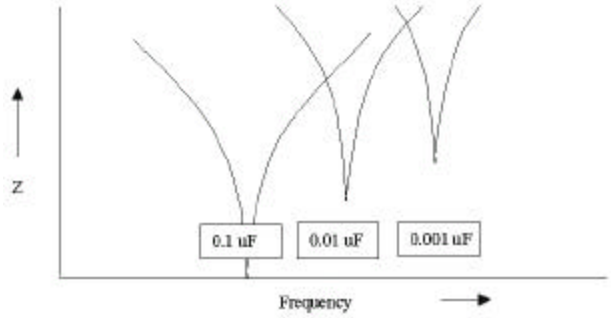


Figure 3 – Low Resonant Frequency

BC-2000®[1], a technology used under license from Sanmina, is the current volume production buried distributed capacitive alternative to the SMT decoupling capacitor; it's structure is depicted in Figure 4.

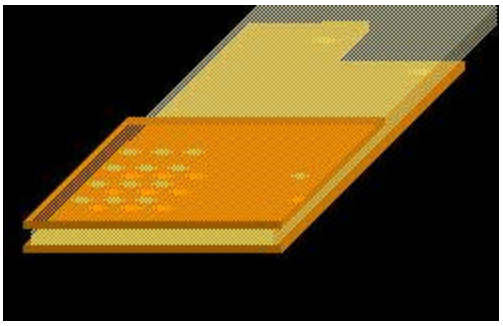


Figure 4 - SMT decoupling capacitor

The capacitance is calculated as:

$$C = 225 * D_k * \frac{A_S}{t}$$

The inductance is calculated as:

$$L \approx \frac{t}{w}$$

Where:

C = Capacitance

L = Inductance

D_k = Dielectric Constant

A_S = Surface Area of opposing planes

t = Dielectric thickness

w = width

225 = Plank's constant

It is very important to note that even though the calculated available capacitance is small (~ 500 picofarads per in^2) it is only going to supply the very high frequency portion of the spectrum. Also the nature of distributed capacitance is that capacitance is borrowed from the plane pair surrounding area. It is typical to have this capacitive structure at layers 2/3 and n-1/n-2. These are acting in parallel to double the available capacitance.

It is equally important to note that the inductance is low compared to a narrow trace leading out to an SMT cap. The connection is normally a short distance by way of a via from the device attachment point down to ground at layer two or power at layer three. Once again the normal structure would have a parallel structure at layers n-1/n-2 further reducing the interplanar inductance. Parallel structures halve the effective inductance except for via length.

Emerging Alternative Distributed Options

A number of suppliers to the PCB industry are bringing to market alternative distributed capacitance products. The theme is to use powdered barium titanate as a filler to epoxy or polyimide polymers to raise the available capacitance by raising the Dielectric constant (see Figure 5). In most cases these alternatives have a lower dielectric thickness, which reduces the interplanar inductance as well. It is clearly advantageous to have a higher level of capacitance on small format circuit boards or chip carriers where BC-2000 has a problem with it's low per square inch capacitance value. In all cases a lower dielectric

thickness between the ground and power planes is advantageous in that the interplanar inductance is directly proportional to this thickness.

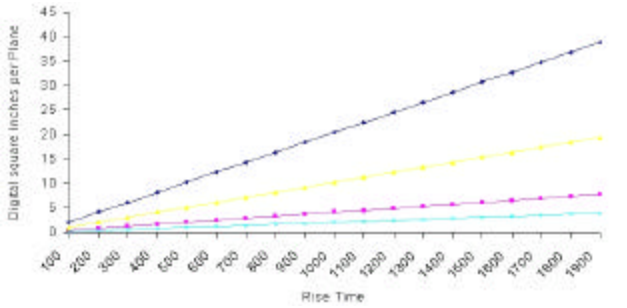


Figure 5 – Dielectric Constant

Experience has shown that even BC-2000 with glass reinforcement suffers from dimensional stability issues in certain situations. When there are a significant number of parts on an 18x24 panel the segmenting of the copper planes decreases the ability to maintain effective registration between the drilled hole pattern and the internal BC-2000 planes. In cases of the emerging non-reinforced dielectrics less than two mils in thickness both dimensional stability and handling issues will be exacerbated. Figure 6 highlights the inductance in a positive way for these new capacitive structures and dimensional stability and handling in a negative direction. It will no doubt be necessary to make some modification to the standard process to accommodate these effects.

	Capacitance	Inductance	Dim Stability	Handling	Voltage Withstanding	Distributed or Discrete
BC-2000™	Low	Low	Moderate	Acceptable	High	Distributed
Thick film High D_k	High	Very Low	Low	Difficult	Low	Discrete or Distributed
Encap™	High	High	Moderate	Difficult	High	Distributed
Thin Film	Very High	Very Low	NA	NA	Very Low	Discrete

Figure 6 – Highlights the Inductance in a Positive Way

Embedded Resistors

The current volume production capable technology for embedding resistors in PCBs and chip carriers is Ohmega-Ply®[2]. This method has been in use for over twenty years and has proven reliability characteristics. In this discussion we will use that as our standard for comparison purposes. The Ohmega-Ply process is to electroplate a nickel phosphorus layer onto the copper foil prior to lamination of the copper onto the dielectric. The thickness of the plated nickel phosphorus layer determines the ohm per square resistivity. The copper circuit pattern is printed and etched into the copper, which leaves the layer of resistive material covering the dielectric. This exposed resistive material is removed in a copper sulfate solution and then another print and etch operation is used to selectively removes copper and leave the underlying nickel phosphorus layer.

Resistance Calculation

For square or rectangle resistors the formula for resistance is:

$$R = \left(\frac{R_m}{t}\right)\frac{l}{w} = R_s\frac{l}{w}$$

R = Resistance
R_m = Resistivity of material
t = Thickness of material
R_s = Sheet resistivity
l = length of resistor
w = width of resistor

In Figure 7, there are two squares so the resistance value is two times the sheet resistivity. If the sheet resistivity is 50 ohms per square we have a 100 ohm resistor.

For annular resistors such as in Figure 8, the calculation is a little more complex

Figure 7 – Two Square

Figure 8 – Annular Resistors

$$R = R_s \ln\left(\frac{D_2}{D_1}\right)$$

R = Resistance
R_s = Sheet Resistivity
D_2 = Diameter of Clearance
D_1 = Diameter of Capture Pad

Emerging Technologies

Three basic approaches are being used in an attempt to advance buried resister technologies: 1) coating a resistive layer onto the copper foil and subsequently processing in a manner very much like Ohmega-Ply but utilizing different materials. 2) Forming discrete resistors on the copper foil prior to it being laminated onto the dielectric.

3) Screening the resistors on the surface of the laminate after the copper geometries have been formed.

In a paper presented at IPC EXPO in April of 2001 Jiangtao Wang and Sid Clouser of Gould[3] describe a process for using roll-to-roll sputtering to deposit Ni/Cr or NI/Cr/Al/Si on the copper foil. The foil is then laminated onto the dielectric and processed in a manner similar to the Ohmega-Ply process. The copper features are etched and the exposed resistive material chemically removed. A second print and etch process selectively exposes the resistive material at the desired locations.

John Felton and William J. Borland of Dupont[4] describe a process for creating discrete resistors on the backside of the foil using thick film material fired at 900°C. A coating is applied to improve durability and then the foil is laminated to the dielectric material resistors facing the dielectric; such as pictured below in Figure 9.

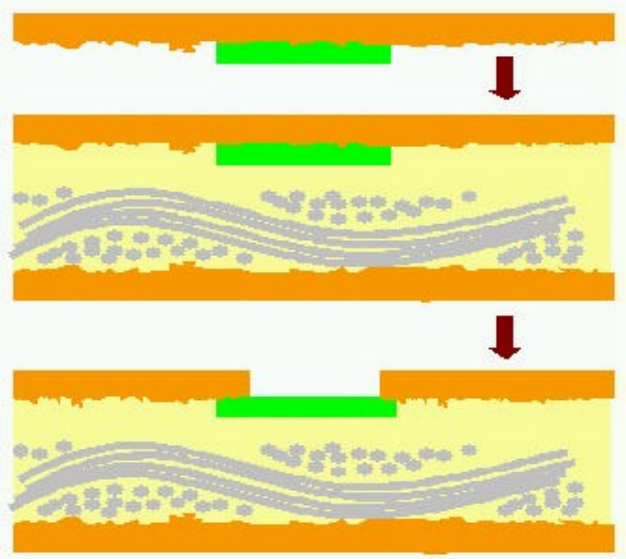


Figure 9 – Applied Coating for Improved Durability

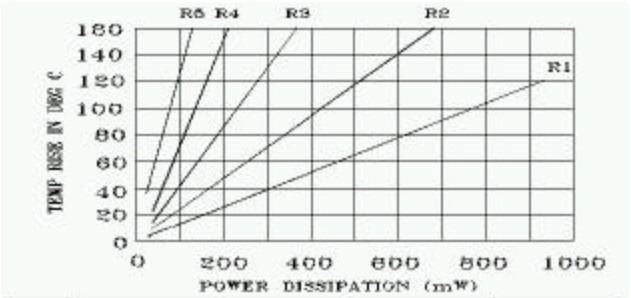
Sanmina is developing a process whereby low temperature curing thick film polymer resistive material is added into the etched clearances of planes between the capture pad and the edge of the clearance.

A number of folks over the years have applied rectangular thick film resistors to the surface layers or internal layers of PCBs. MacDermid is working on a process to electroplate discrete Ni/P resistors at specific locations on internal or external layers.

Heat Dissipation

By their nature resistors are heat-generating devices. In most if not all cases and types of embedded resistors the management of this heat has to do with the area surrounding the resistor as well as the resistor itself. Once again the Ohmega-Ply information on this subject is very helpful. The graph in Figure 10 shows the effect of resistor size on heat generation; the larger the resistor the easier it is for it to dissipate heat. In Figure 11, we see some of the effect of the surrounding area. R1 shows extreme temperature rise. This is a 250 ohm resistor with no copper on an adjacent layer to absorb and redistribute heat. R2 on the other hand has copper 0.0025" away on the adjacent plane and the heat is dissipated much more effectively.

Ohmega-Ply Technologies Inc has studied for years now the effect of heat on the resistors and offers the ability to balance heat generation and tolerancing using a spread sheet. This capability is available on-line at their website, www.ohmega.com



#	Resistor size (Ω)	Length (inches)	Width (inches)	Area (inches²)
R1	25	0.500	0.500	0.2500
R2	25	0.250	0.250	0.0625
R3	25	0.125	0.125	0.0156
R4	25	0.063	0.063	0.0039
R5	25	0.031	0.031	0.0010

Figure 10 – Effect of Resistor Size of Heat Generation

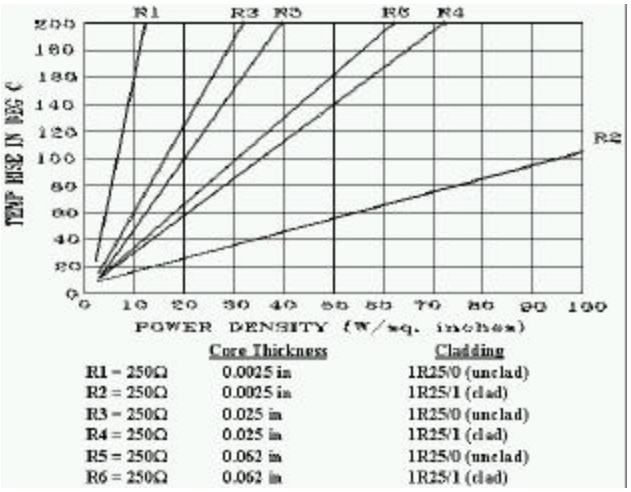


Figure 11 – Effect of Surrounding Area

Tolerancing

There is a great deal of debate over the required tolerance. Ideally the tolerance would be consistent with discrete SMT resistors at one or two percent. Generally embedded resistor technology as it stands today is in the vicinity of fifteen percent. There is about five percent tolerance for the resistive materials and another ten percent due to the process of forming the resistors (screen printing or printing and etching). As with heat dissipation there is advantage to larger dimensions. Printed circuit

manufacturers are capable of holding a dimension for a feature at plus or minus one half mil. If the feature size for a resistor is 10 mils this means a built in tolerance of five percent. If the resistors are formed on cores and subsequently processed through oxide or oxide alternative some additional change in resistance will be experienced. Likewise the lamination process itself can have an effect. All of these factors are responsible for the inherent estimated tolerance of fifteen percent.

Laser trimming is a popular option in cases where tight tolerances are needed. The resistor is designed to yield a lower than desired resistance and then trimmed to the desired value. Assuming the correct type of laser, and proper settings for the material set, carbonization of the dielectric polymer can be avoided in most cases. Carbonatious residues have conductivity. According to Tim Estes of CAT Inc., the best approach (based on his experience at Sandia Labs) is an "L" cut (Figure 12). The laser machine first measures the resistance, ablates a calculated amount across the resistor to get within 2-3% and then under constant measurement it makes a cut 90 degrees from the first cut bring the resistance within 1% of target. If the shift in resistance due to subsequent lamination processes is known it can be factored in.

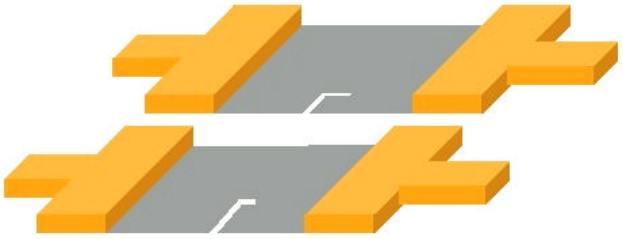


Figure 12 – "L" Cut

Summary

The current standard for buried distributed capacitance, BC-2000, is seeing some emerging competition. Generally these emerging technologies have higher levels of capacitance and lower levels of inductance. They are, however, more likely to experience difficulties in handling and registration due to their very thin non-reinforced nature.

The current standard for embedded resistors, Ohmega-Ply, is also seeing some emerging competition. In some cases these are quite similar in nature to Ohmega-Ply and in some cases quite unique approaches. In general these emerging technologies have heat dissipation requirements and tolerance capability similar to Ohmega-Ply.

References

1 BC-2000 is a registered trademark of Sanmina Corporation.

2 Ohmega-Ply is a registered trademark of Ohmega Technologies Inc.

3 Jiangtao Wang and Sid Clouser, "Thin Film Embedded Resistors" Technical Proceedings of IPC EXPO 2001, SO8-1-1 to SO8-1-5

4 John J. Felton and William J. Borland, "Embedded Ceramic Passives: Process Development", Technical Proceedings of IPC EXPO 2002, SO8-2-1 to SO8-2-4