FUNDAMENTALS OF EMBEDDED PASSIVE COMPONENTS

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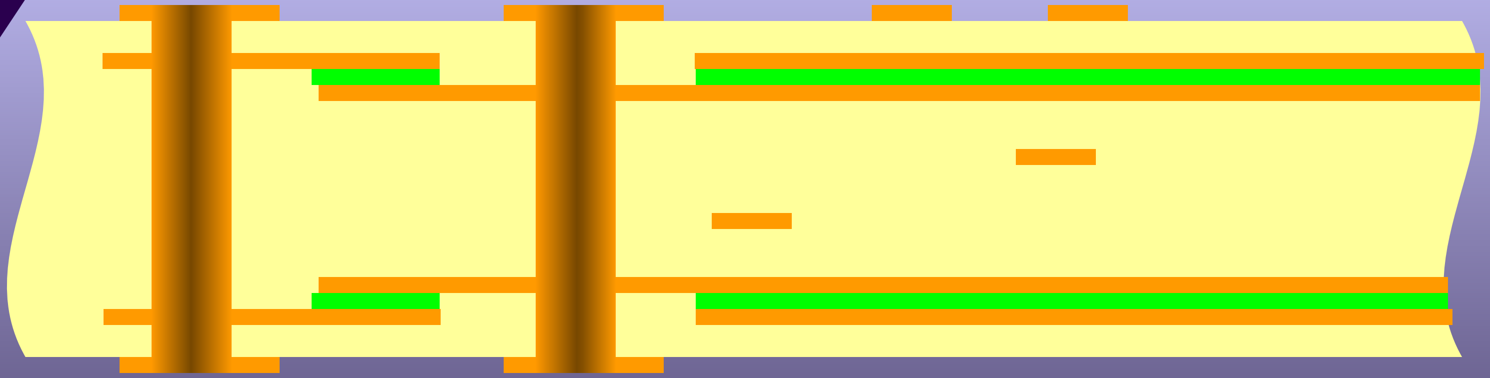
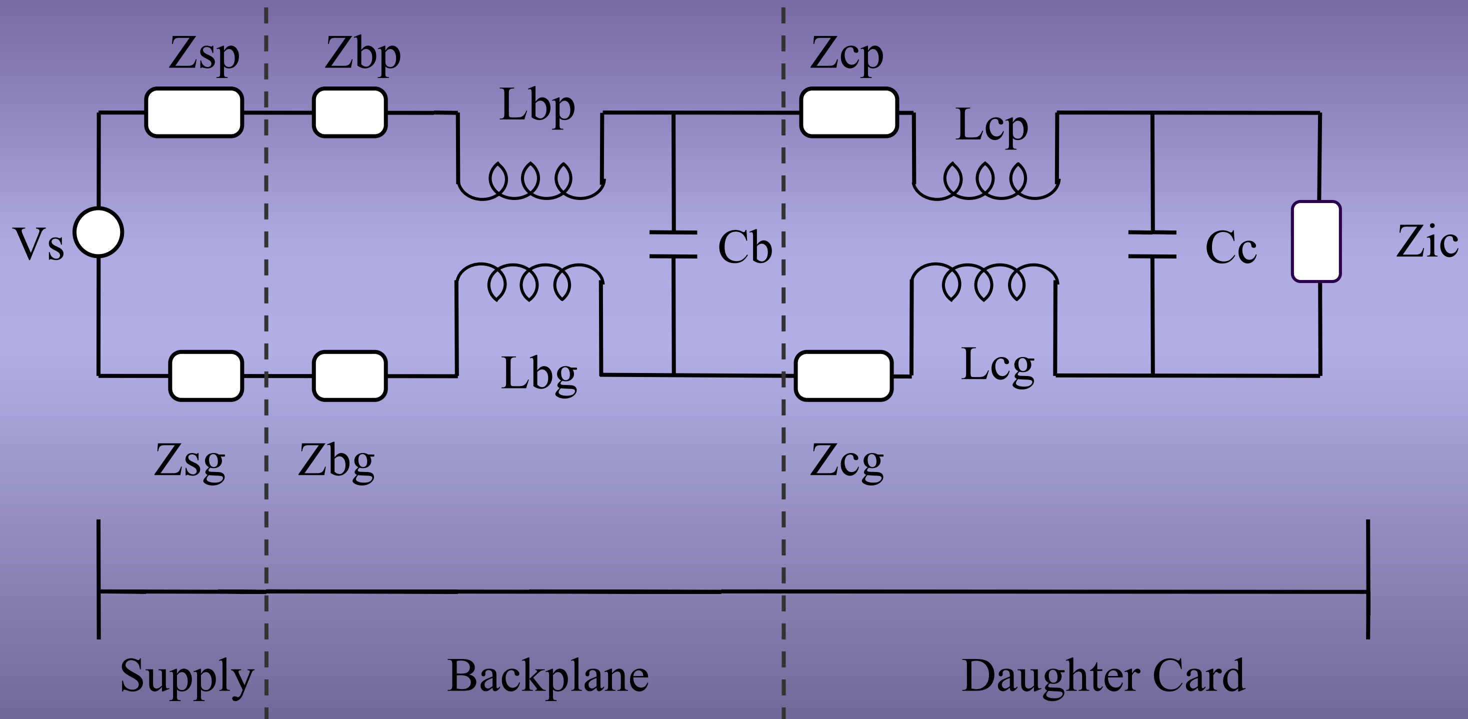
Topsearch Printed Circuits LTD

BURIED CAPACITANCE



Power Distribution Model



$$V_{load} = Vs - (V_{dc} + V_{ac})$$

Power Distribution Model

$$V_{load} = Vs - (V_{dc} + V_{ac})$$

$V_{dc} = I_{dc}(R_s + R_b + R_c)$ = the dc voltage drop through the system.

I_{dc} is the dc current

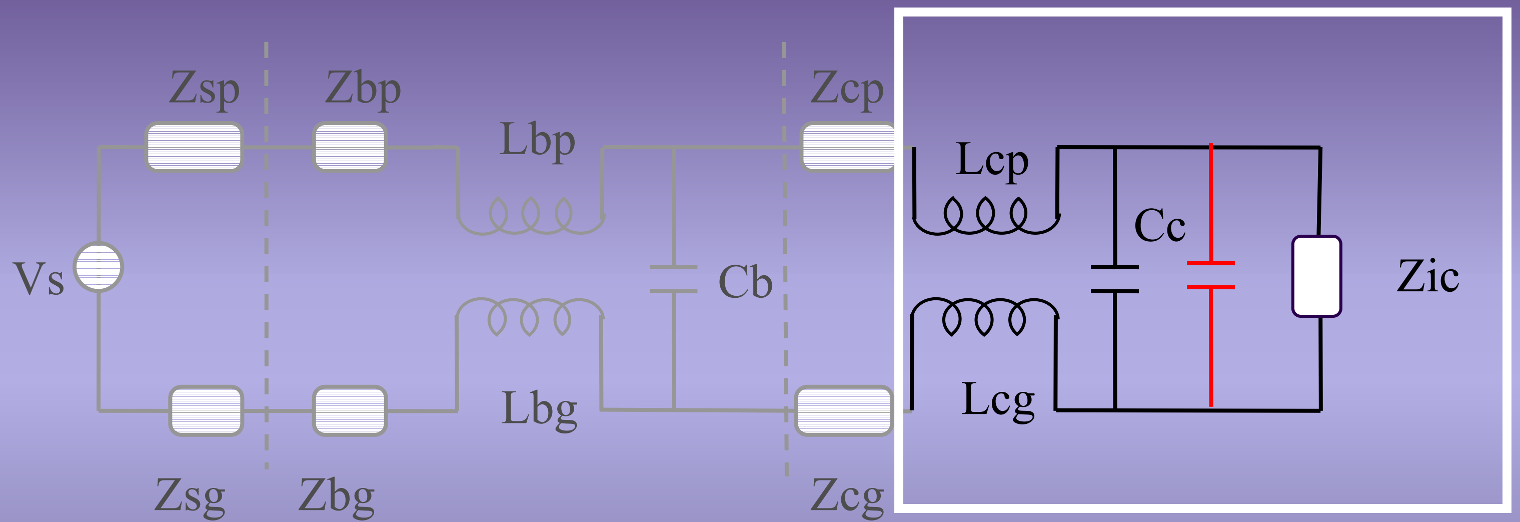
R_s is the source resistance

R_b is the backplane resistance

R_c is the card resistance

$V_{ac} = I_{ac}\,(Z_s + Z_b + Z_c)$ = the ac voltage drop through the system with corresponding impedances relating to each section of the system.

Add SMT Capacitor



Examine the cap circuit

The Cap Circuit

$$Z_{cap} = \sqrt{R_{cap}{}^2 + X_L{}^2 - X_C{}^2}$$

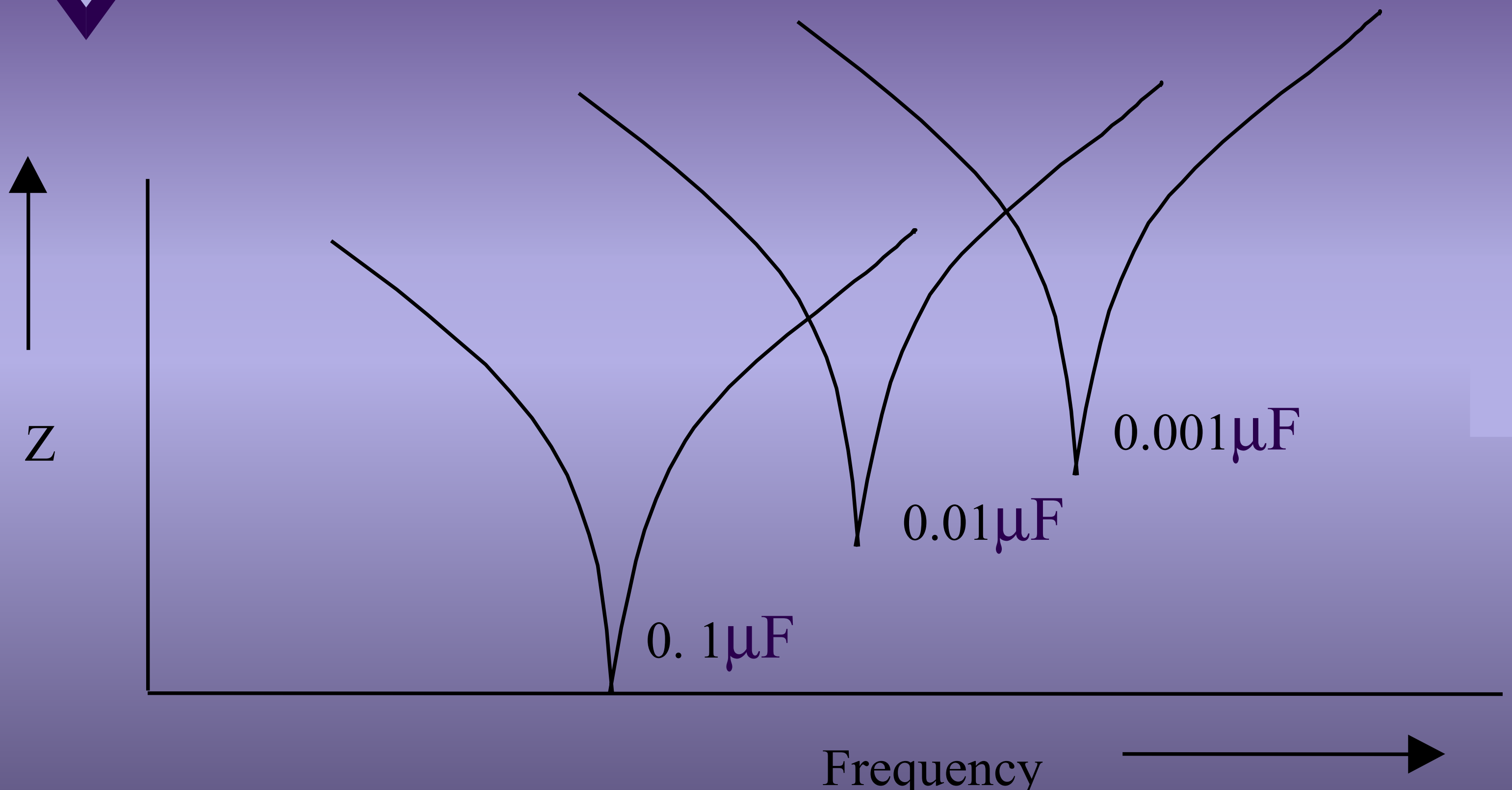
R_{cap} = DC resistance

$X_L = 2 * \pi * f * L_C$ = Inductive Reactance

$X_C = \dfrac{1}{2\pi * f * C_C}$ = Capacitive Reactance

f = frequency

Add SMT Capacitor



At high frequencies

$$Z_{cap} = \sqrt{(R_{cap}{}^2 + (X_L{}^2 - X_C{}^2))} \approx 2 * \pi * f * L_C$$

R_{cap} = DC resistance

$X_L = 2 * \pi * f * L_C$ = Inductive Reactance

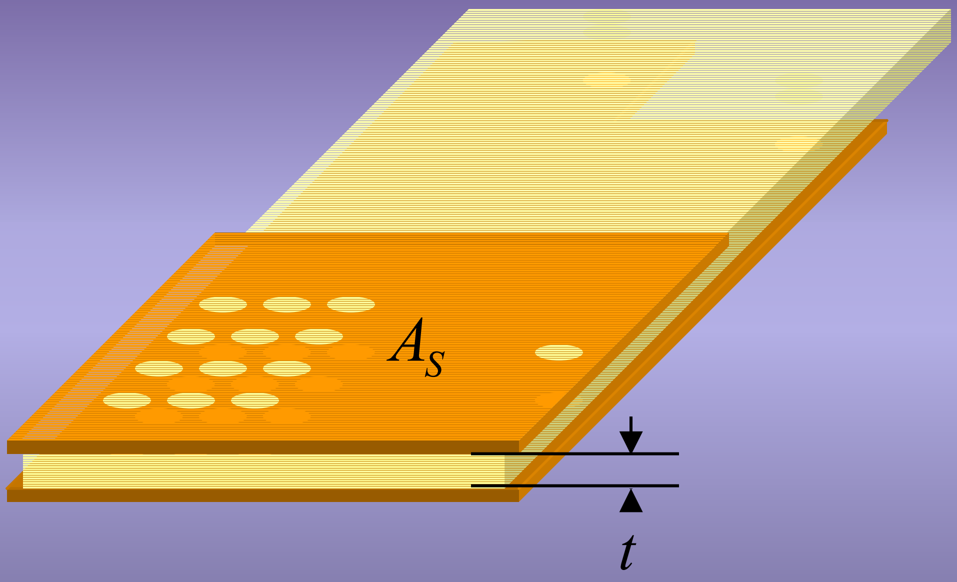
$X_C = \dfrac{1}{2\pi * f * C_C}$ = Capacitive Reactance

f = frequency

Buried Capacitance

$$C = 225 * D_k * \frac{A_S}{t}$$

$$L \approx \frac{t}{w}$$



C = Capacitance

L = Inductance

D_k = Dielectric Constant

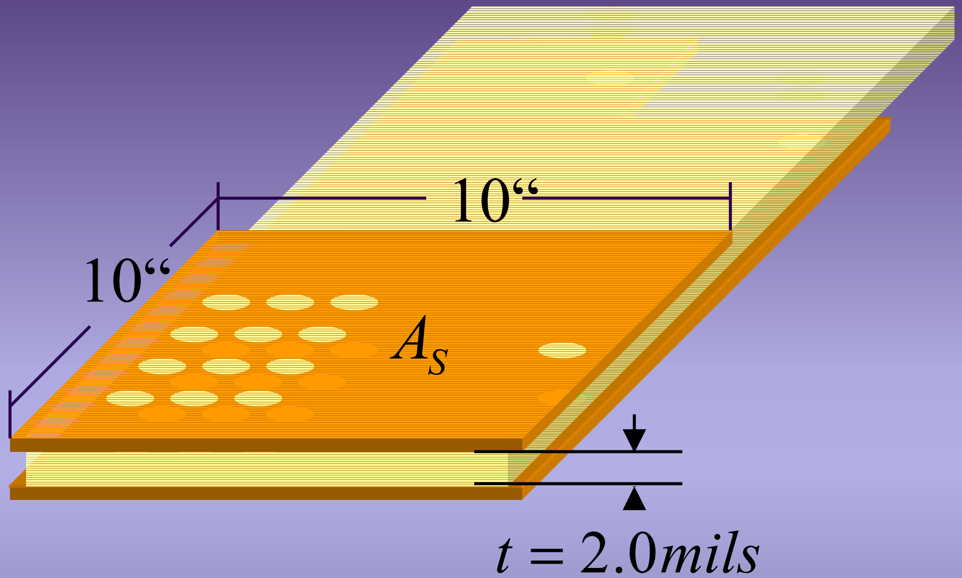
A_S = Surface Area of opposing planes

t = Dielectric thickness

w = width

225 = Faraday's constant

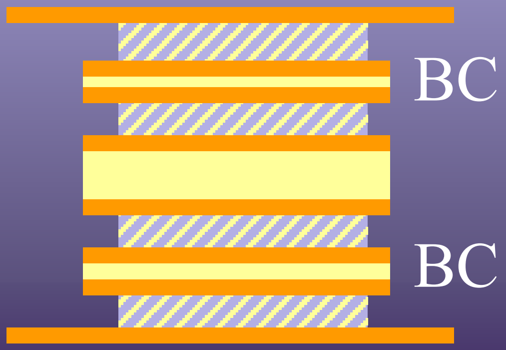
BC-2000™



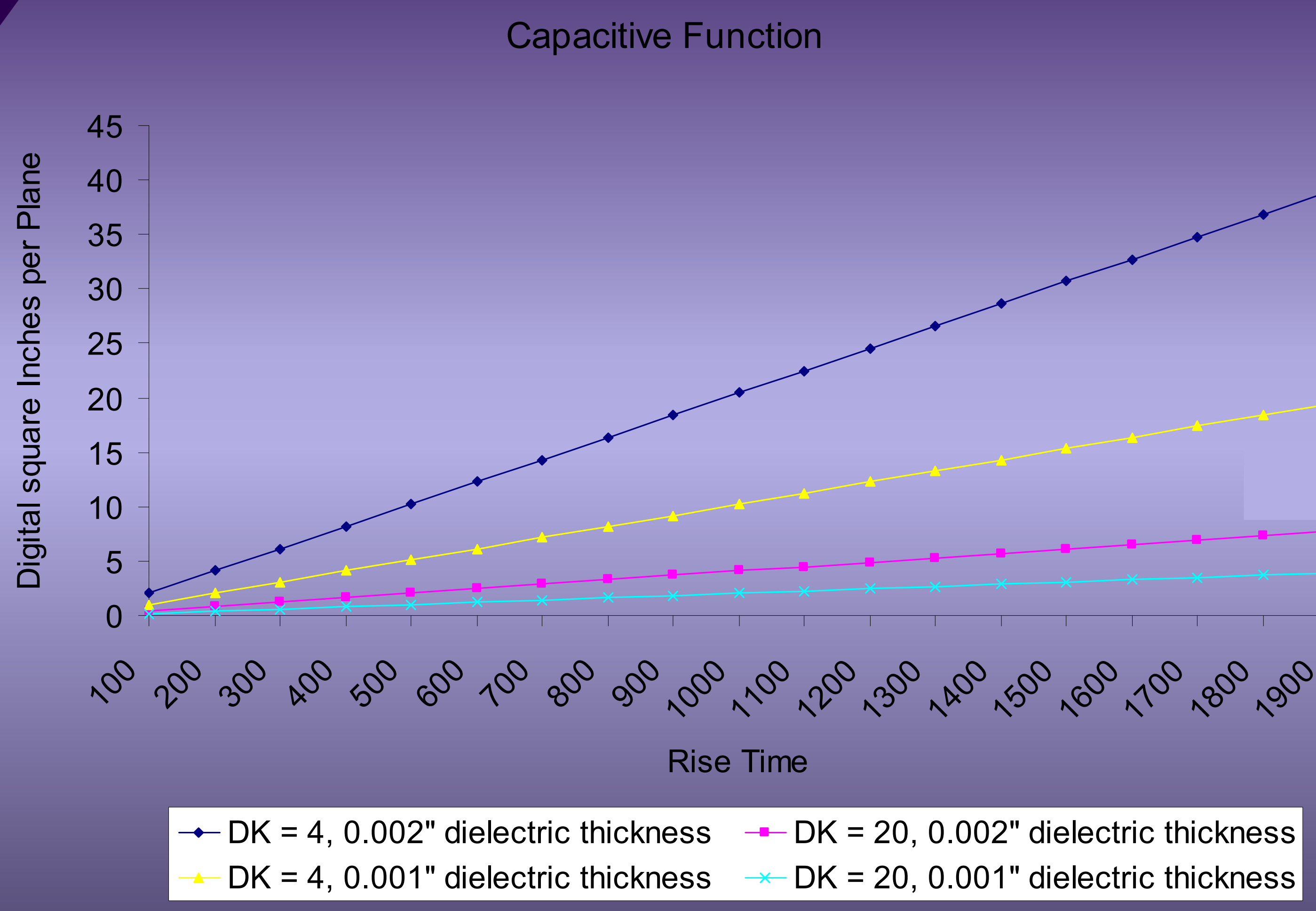
$$C = 225 * D_k * \frac{A_S}{t}$$

$$e.g.: 225 * 4.5 * \frac{10\text{"}*10\text{"}*2 \text{ planes}}{2}$$

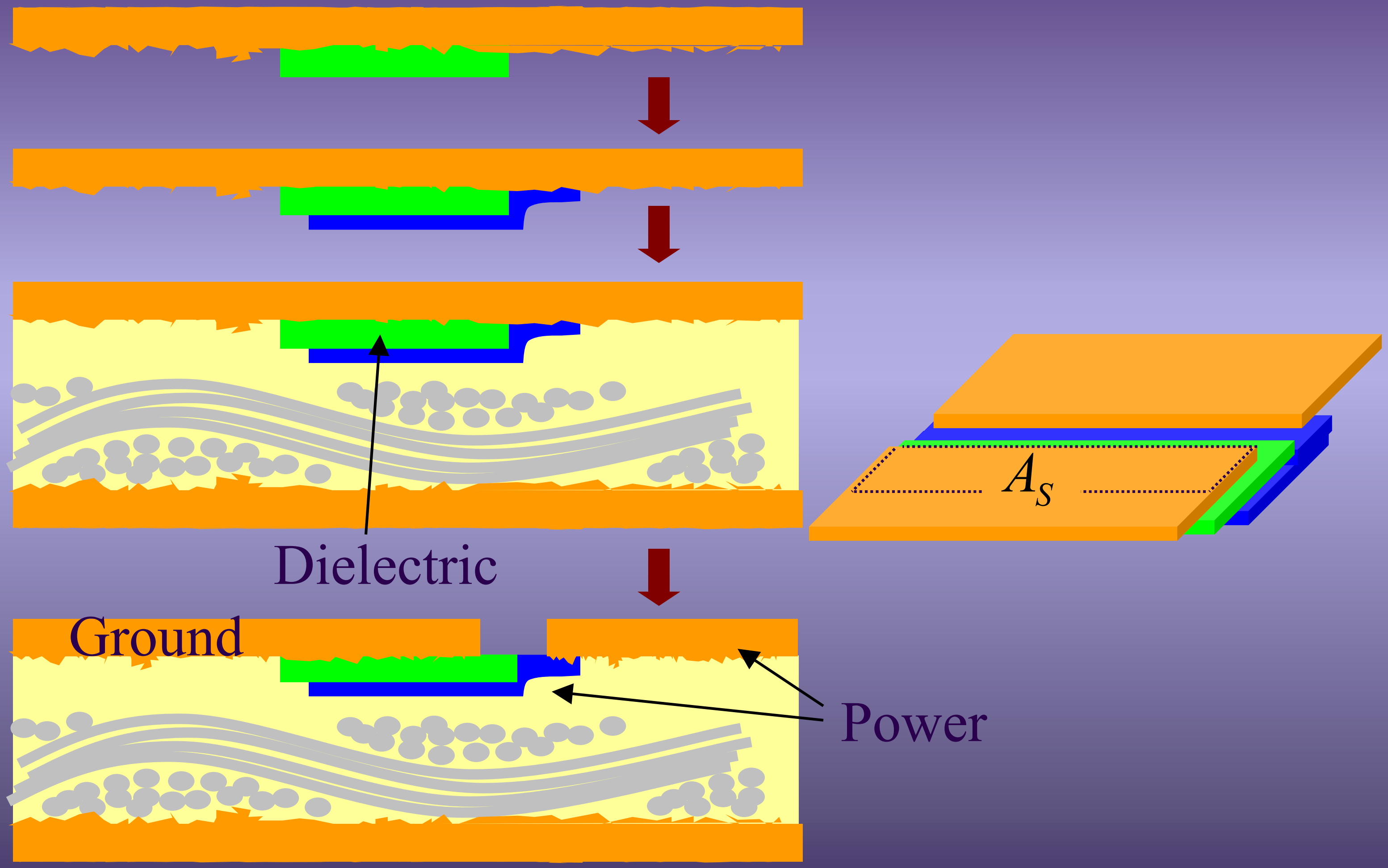
$$= 101{,}250\, pF \text{ or } 0.1 \mu F$$



Capacitance Effects



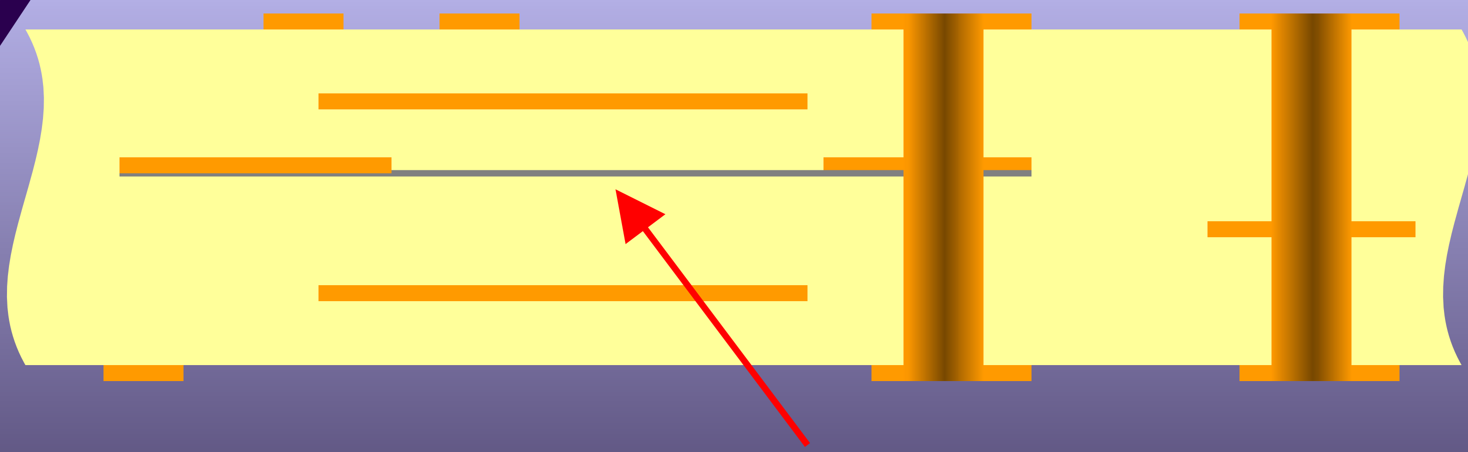
Thick Film Technology



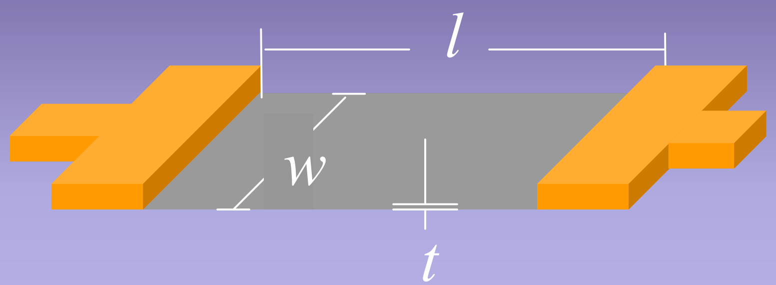
EMERGING TECHNOLOGIES

	Capacitance	Inductance	Dim Stability	Handling	Voltage With-standing	Distributed or Discrete
BC-2000™	Low	Low	Moderate	Acceptable	High	Distributed
Thick film High D_K	High	Very Low	Low	Difficult	Low	Discrete or Distributed
Emcap™	High	High	Moderate	Difficult	High	Distributed
Thin Film	Very High	Very Low	NA	NA	Very Low	Discrete

BURIED RESISTORS



Rectangular Resistor Values



$$R = \left(\frac{R_m}{t}\right)\frac{l}{w} = R_s\,\frac{l}{w}$$

$R =$ Resistance

$R_m =$ Resistivity of material

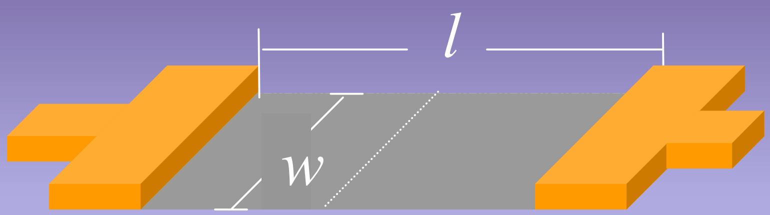
$t =$ Thickness of material

$R_s =$ Sheet resistivity

$l =$ length of resistor

$w =$ width of resistor

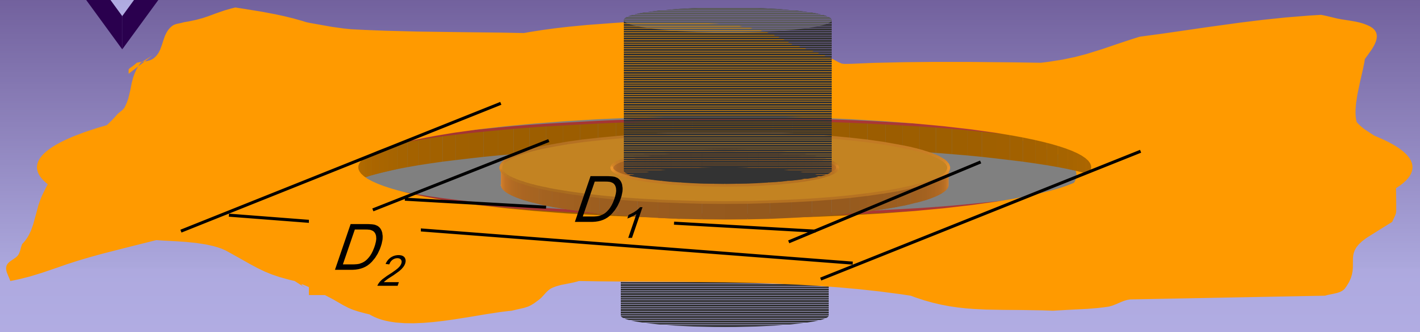
Rectangular Resistor Values



$$R = R_s \frac{l}{w}$$

R_s	l	w	R
(Ohms)	(μm)	(μm)	(Ohms)
50	500	250	**100**
100	500	250	**200**
150	500	250	**300**
50	250	250	**50**
50	500	250	**25**

Annular Resistor Values



$$R = R_s \ln\left(\frac{D_2}{D_1}\right)$$

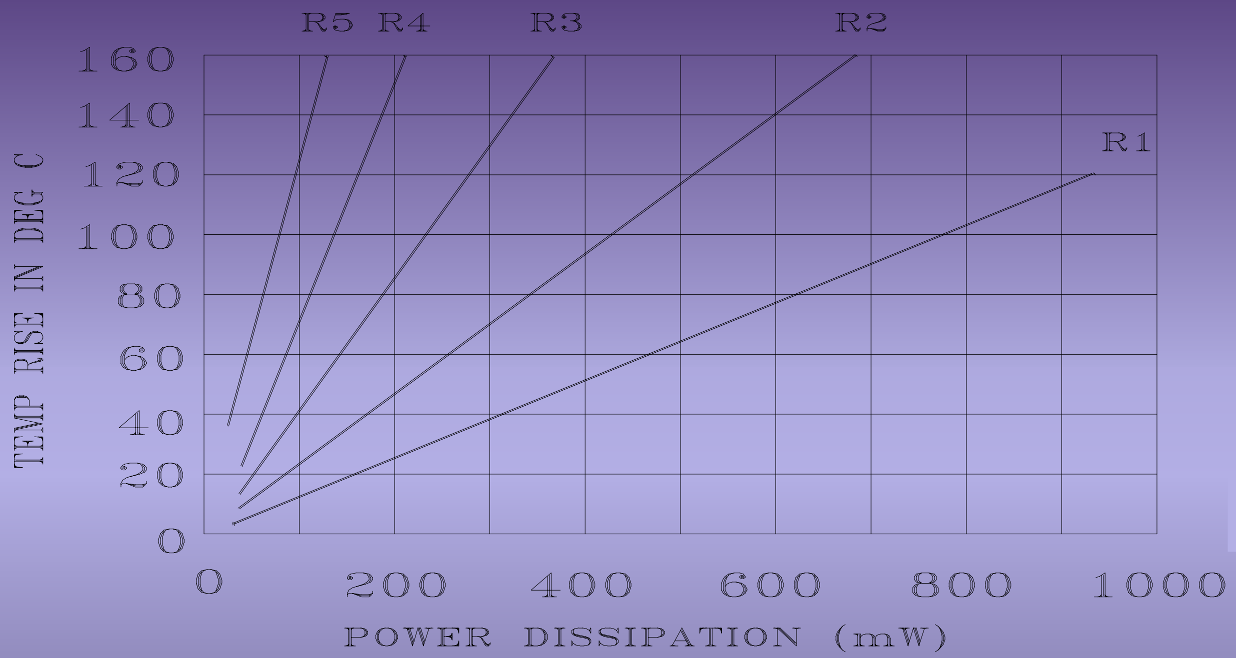
$R =$ Resistance

$R_s =$ Sheet Resistivity

$D_2 =$ Diameter of Clearance

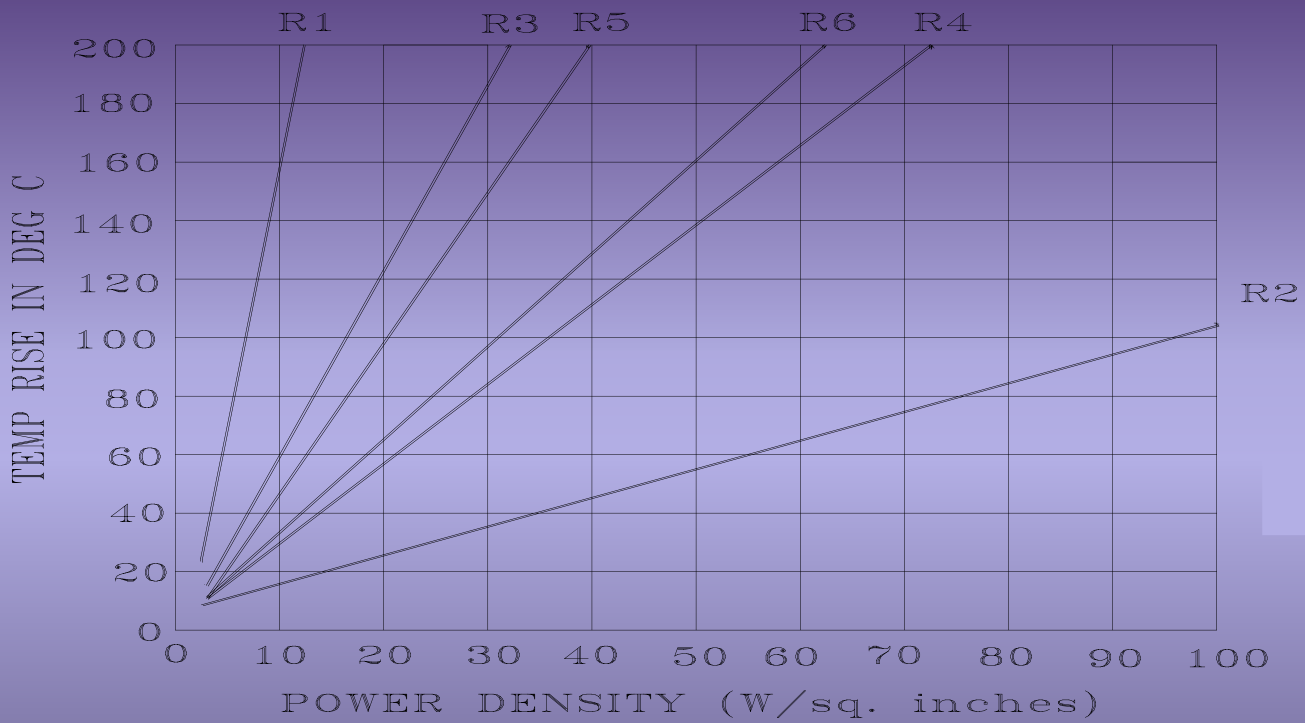
$D_1 =$ Diameter of Capture Pad

Temperature Rise vs Power Density for Different Areas



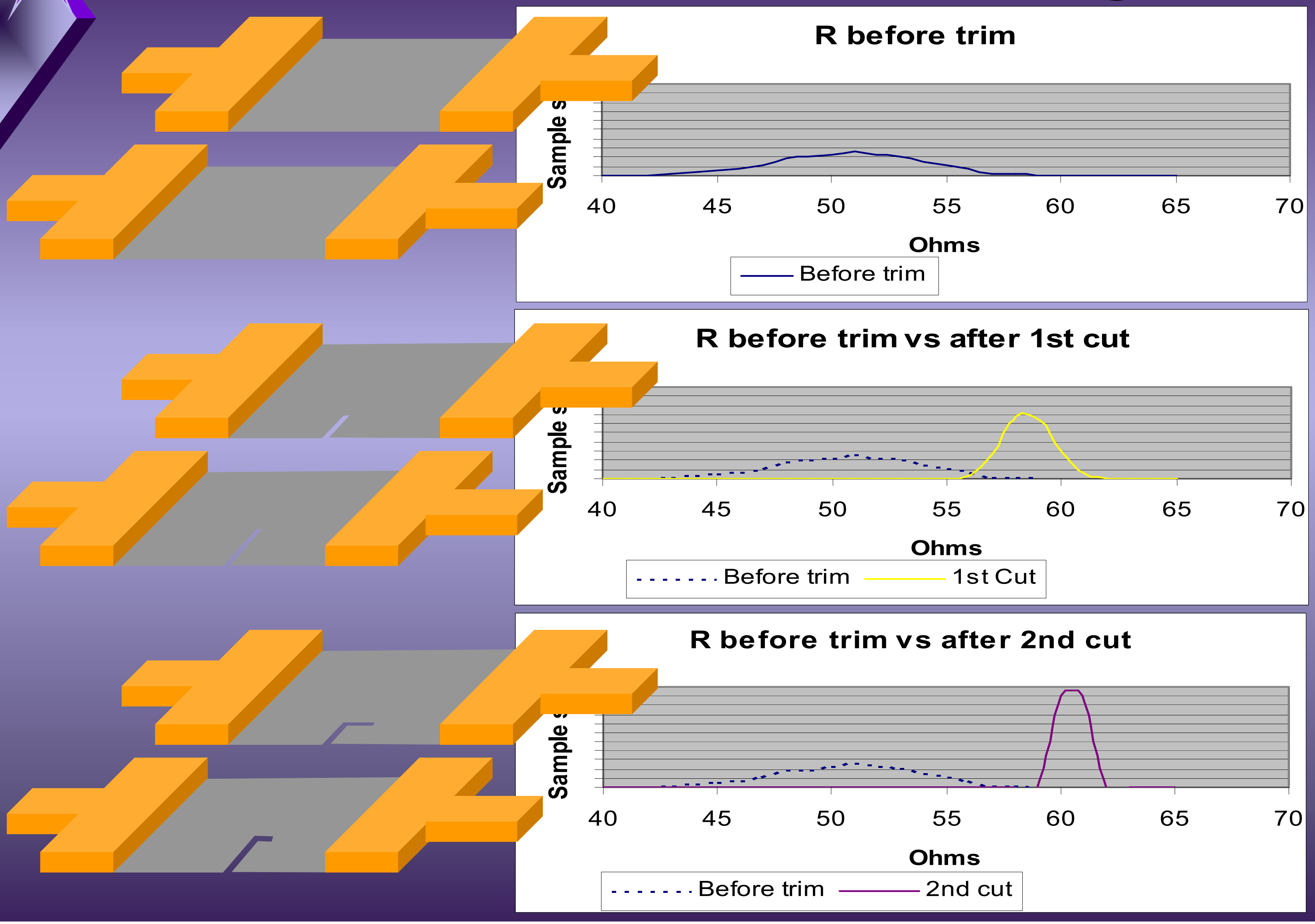
R1 = 25Ω area of R1 = 0.500 x 0.500 = 0.2500 in^2
R2 = 25Ω area of R2 = 0.250 x 0.250 = 0.0625 in^2
R3 = 25Ω area of R3 = 0.125 x 0.125 = 0.0156 in^2
R4 = 25Ω area of R4 = 0.063 x 0.063 = 0.0039 in^2
R5 = 25Ω area of R5 = 0.031 x 0.031 = 0.0010 in^2

Temperature Rise vs Power Density for Different Core Thickness and Cladding



	Core Thickness	Cladding
R1 = 250Ω	0.0025 in	1R25/0 (unclad)
R2 = 250Ω	0.0025 in	1R25/1 (clad)
R3 = 250Ω	0.025 in	1R25/0 (unclad)
R4 = 250Ω	0.025 in	1R25/1 (clad)
R5 = 250Ω	0.062 in	1R25/0 (unclad)
R6 = 250Ω	0.062 in	1R25/1 (clad)

R Tolerance Laser Trimming



R Tolerance

	Resistivity	Thickness	R Geometry	Cu Geometry	Total	After Triming
Plated	2%	3%	5%	5%	15%	<1%
PTF	1%	5%	0-5%	5%	11-16%	<1%
Thin Film	0-1%	1%	1%	1%	3-4%	<1%
TF on Foil	0-1%	1%	1-5%	5%	3-12%	<1%

Assumptions:

0.010 - 0.012” smallest dimension

18”x24” panel