Development of High Density and High Frequency Substrate Using B^{2}it^{TM} Technology for Next Generation Packaging

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Abstract
For faster, smaller, and high performance integrated circuits the new concept of buried bump interconnect substrates is required. We have developed B^{2}it^{TM} (buried bump interconnection technology) for this technical trend. The fine phase ? of this interconnection technology carries out the build up of the fine wiring layer of Cu/BCB on all buried bump interconnection technology wiring boards for high-density and high performance. This paper reports the results that focus on the fine wiring layer formation process technology and the high frequency transmission characteristic of the fine phase ? as a result of a fine wiring formation process' adopting BCB as dielectric material and the sputter semi additives method. The limitation of the minimum pitch was 10µ m (L/S=6 /4). Filled via process was possible for a 20µ m via diameter. Electromagnetic simulation was performed to research the dependence of the signal transmission characteristic on the pitch of fine lines. When the pitch becomes small at 10µ m or less, it turns out that transmission loss becomes large due to the influence of contiguity wiring. As high frequency correspondence aptitude, a result of the S parameter with micro strip line structure, it was –3dB in 16GHz. From this, as a design rule for fine wiring layers, a pitch of 15µ m (L/S=7.5/ 7.5), and 20µ m for filled via diameters are optimal designs. The fine wiring technology was developed and designed for a high density and high-speed substrate, utilizing this buried bump interconnection technology.

Introduction
As electric products become smaller and lighter with an increasing number of functions, the demand for high-density printing wiring substrates becomes stronger. According to the SIA road map, the flip chip pad pitch and the high frequency characteristic which are demanded from a semiconductor technical node are shown in a Table 1.[1] As for the flip chip pad pitch, it is shown about the trend of high-density required 0.15mm level and high speed clock frequency required 3GHz in 2004. Based on this, we compute the frequency characteristic and wiring width which are needed for a next generation substrate. The wiring width calculated is shown in Figure 1. This data computed along with same rules. First, fan out is carried out in F.C.0.15mm pad pitch. Land is 0.075mm. Via structure is stack type. Second, each pad has lines. Lines must be fanned out from FC area using pad space. This result indicates that under 10µ m line width needed for high-density substrate after 2004. For example, 0.15mm padpitch, 3600 pin count FC-package needs 8.3µ m line width by 4 layer. Conventional plated-through-hole substrates are insufficient to meet this demand. High speed clock require 3GHz On-Chip perfomance. High frequency transmission characterstics of substrate is required –3dB in9GHz.

Table 1 Technology Nodes for High Density Packaging Substrate

	2002	2004	2005	2007	2010	2016
Technology Nodes (nm) MPU/ASIC	180	90	80	65	50	26
Needs for						
BGA Ball-Pitch (mm)	0.4	0.4	0.4	0.3	0.3	0.25
FcpadPitch (mm)	0.16	0.15	0.13	0.12	0.09	0.07
Line(µ m)	10.7	10.7	9.2	9.2	6.4	5.0
Space(µ m)	10.7	10.7	9.3	9.3	6.4	5.0
Performance						
On-chip(GHz)	2.32	3.09	5.17	6.74	12	29
Performance Chip-to-Board For peripheral Buses (GHz)	1.87	2.26	2.49	3.01	4.0	7.1

Source ITRS2001 Edition

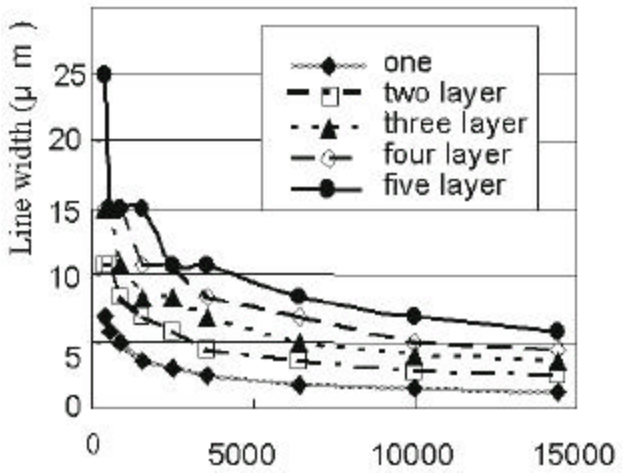

Figure 1 - Calculated Result of Required Line Width

We have developed this buried bump interconnection technology for this technical trend.[2] The fine phase ? aspect of this technology carries out the build up the fine wiring layer of Cu/BCB on all buried bump interconnection technology wiring boards for the further high-density and high performance.[3] This paper reports the results that focus on the fine wiring layer formation process technology and the high frequency transmission characteristic of the fine phase ? .

Feature

We have developed this buried bump interconnection technology substrate L/S30/30μ m or less high-density board. The design rules for the current (standard) and future interconnection technology are shown in Table 2. Line and space can not respond in the conventional process any longer. We have proposed a combination of conventional thick film technology and the thin film technology which can be fine wired. We achieved this by using the all buried bump interconnection technology printed wiring board as a core substrate and then generating thin layer of Cu/BCB (benzo cycro butene) on the top of the all buried bump interconnection technology wiring board. That is, we show all the IVH layer structures according to thick film technology. Only a necessary minimum layer overly carries out additional formation of the fine wiring with thin film technology at the surface. (Figure 2) It can be a fine and high-density pad pitch compared with the conventional method. And also compares with conventional plugged double side wiring substrate in the same network by this, the number of wiring layers can be reduced.

Table 2 - Buried Bump Interconnection Technology Design Rules

	Standard	Fine f 1	Fine f 2	Fine f 3
Build up layer				
L/S	-	-	-	7.5 /7.5
Via/Land	-	-	-	20/30 stack
Core				
L/S	100 /100	75 /75	50 /50	30 /30
Bump Diameter	300	150	100	100
Pad Diameter	500	300	200	200
Bump Pitch	600	400	300	300

(μ m)

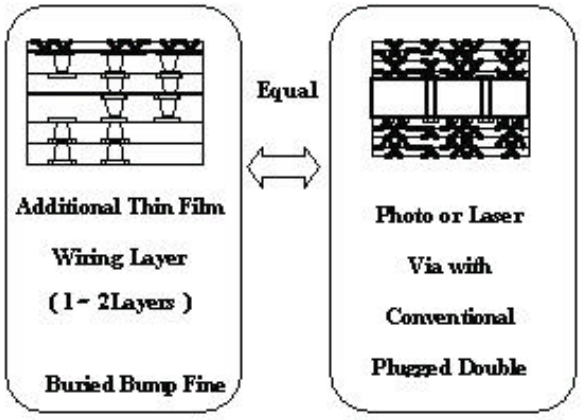

Figure 2 - The concept of Finef ?

Process

The basic process of the buried bump interconnection technology fine phase ? is shown in Figure 3. The all interconnection technology wiring board of all layer IVH structures are prepared as core substrate. First, a photosensitive BCB is applied to the core substrate using spin coater for planarization, and then a photosensitive BCB is subsequently coated, exposed, developed, and cured. This is the 1st insulation layer. Second, seed metal layers are coated 0.23μ m by sputtering method. Third, liquid resist is applied to the substrate using a spin coater. After exposure and development, the Cu conductor was grown up to 4μ m thick by using a fountain type electroplater. Finally, the resist is stripped and the seed layer is removed by etching. A multilayer wiring layer is then formed by repeating the above mentioned process. Figure 4 depicts a finished buried bump interconnection.

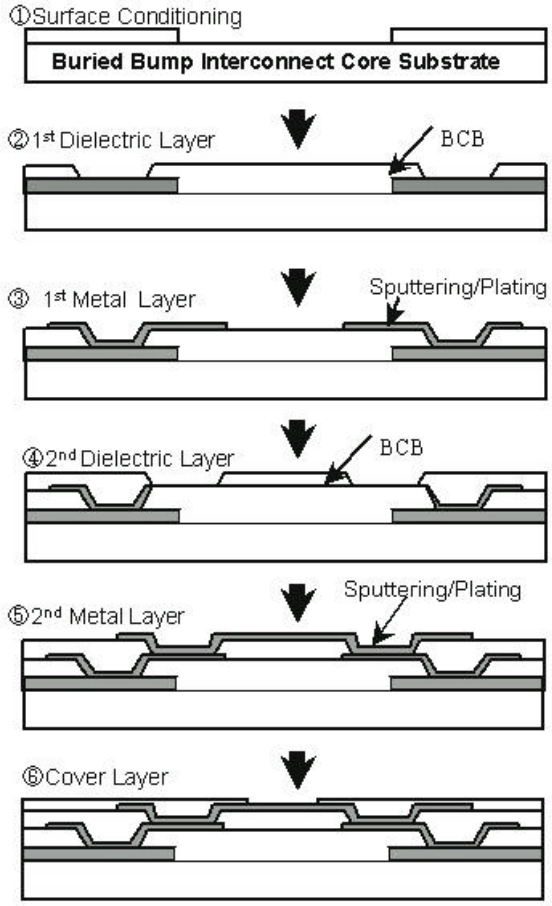

Figure3 - Fabrication Process

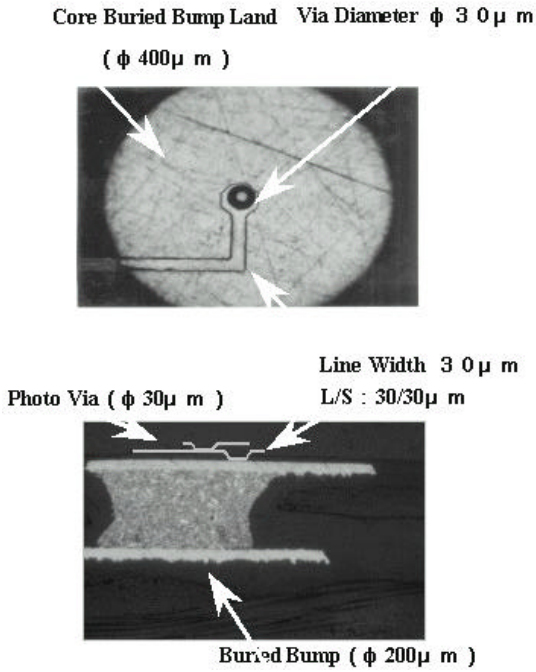

Figure 4 - Interconnection Over View

A core Substrate

A core substrate uses a buried bump interconnect board. The fundamental manufacturing process of a core substrate is shown in Figure 5. Thus, a manufacturing process is simple and various structures and the number of layers is obtained. The result which investigated the basic characteris tic as a substrate is shown in a table 3.

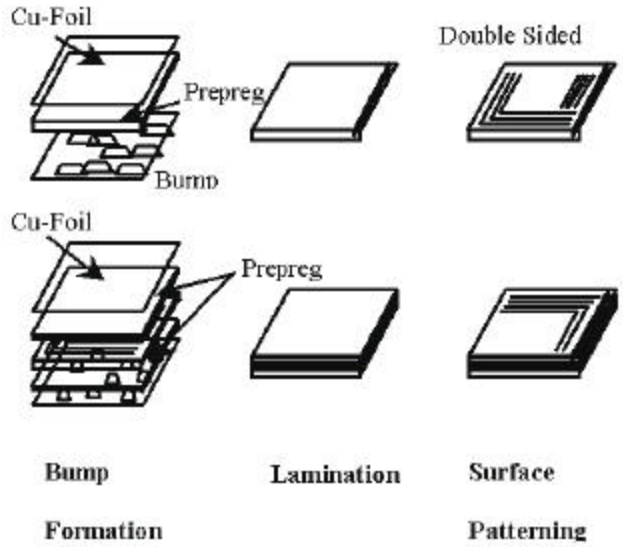

Figure5 - Buried Bump Interconnect Manufacturing Process

Table 3 - Reliability Test Results of Buried Bump Interconnect Core Substrate

Item	Condition	Criteria	Result
Dielectric Strength	DC500V 1min	? 100M0	Passed
Temp /Himid	25 ? ? 65? 90~ 98% 10cyc.	? 100M0	Passed
THBT	85? 85% DC12/65V 500h	? 100M0	Passed
TC	-65 ? ? 125? 1000cyc	< 10%	Passed
HAST	130? /85% DC10V 100h	< 10^{-10}A	Passed

Fine Wiring Layer and Formation Process

Our fine wiring formation method adopted the sputter semi additive method. If a wiring pitch is under 20μ m or less, by the etching method, wiring formation will become very difficult since wet Cu etching goes on isotropic. If the semi additive method were adopted, wiring width would mostly be oriented by the resolution of a photo resist. 20 μ m pitch would be possible. A thin film by way

sputtering was used for the seed layer. It is flat and smooth in a resin surface, excels in fine pitch wiring formation, and the high frequency characteristic. Figure 6 shows pre treatment Ar treatment before sputtering good effect on resin surface. We show a result of forming two-layer wiring with a thickness of 4μm on BT resin core board. Also, by investigating line width reproducibility, a stable formation of wiring pitch 10μm (L/S=6/4) was noted. Photograph and line width accuracy of wiring is shown in Figure 7.

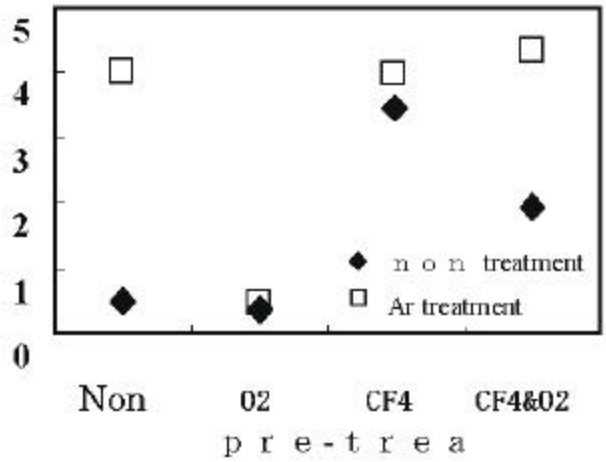

Figure 6 - Pre-treatment Condition for Sputtering

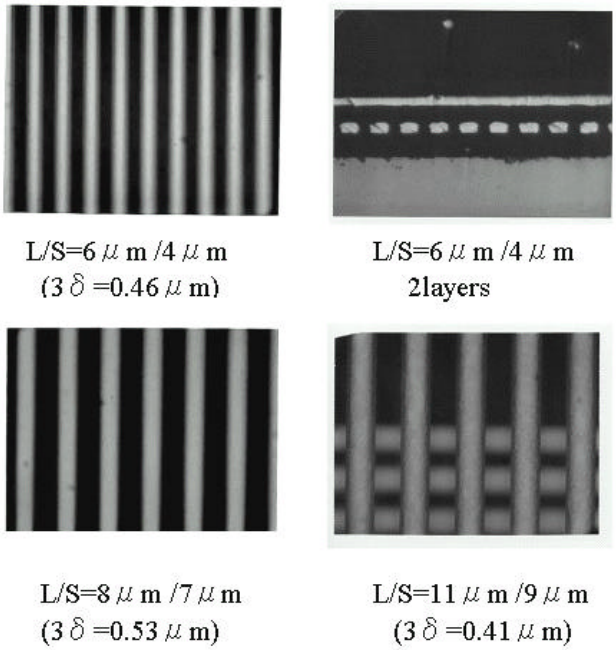

Figure 7 - Photographs of Fine Line

We examined the via-on-via stacked structure by the filled plating process. (See Figure 8.) It becomes advantageous to design for high-density wiring substrate. Filled plating was able to form a via of a diameter of 20μm by 4μm of electroplating thickness, and 6μm of via pad thickness. A via section is shown in Figure 8.

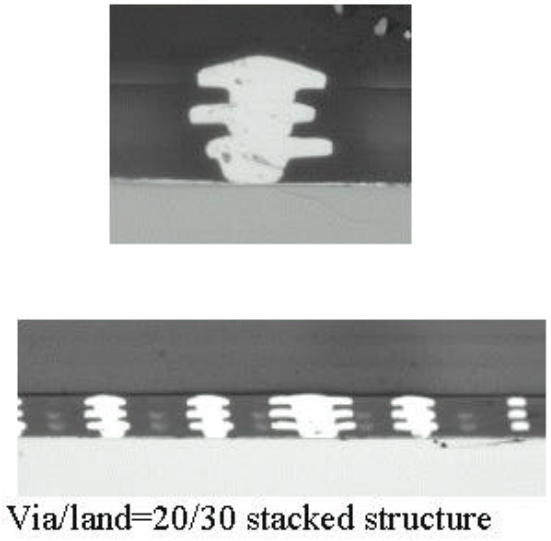

Figure 8 - Photograph of Via

The insulated layer had photosensitive BCB from various-kinds of photosensitive insulation materials selected. BCB made it possible to obtain a stablevia opening of 20μm in diameter. Impedance matching was carried out by a microstrip line model. We show optimal thickness of insulator using a micro strip structure and 50 0 adjustment (Figure 9).

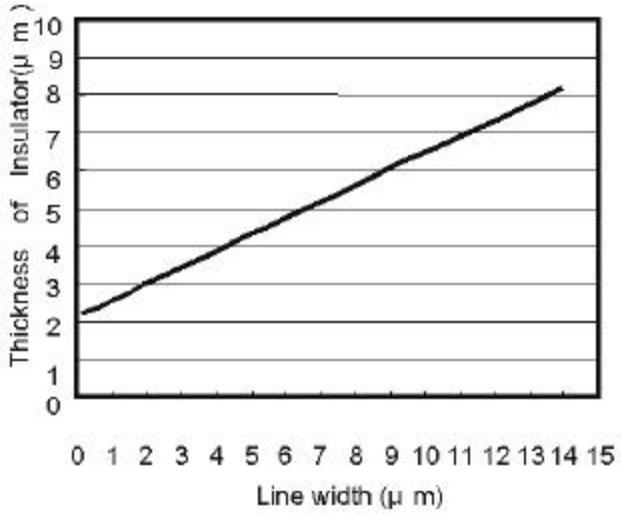

Figure 9 - Optimal Thickness of Insulator for Impedance Matching of Micro Strip Line Model

We calculated transmission loss and dielectric loss with the dielectric constant of each material. The dielectric constant of each material, and dielectric loss are adopted at 1GHz. A simulator made from ANSOFT, HFSS (3-dimensional high frequency electromagnetic boundary simulator), performed with a wiring width of 10μm, and wiring thickness 4μm micro strip line structure, 500 adjustment from the result of Figure 9 and 5mm of wiring length. The result carried out by the simulation is shown

in Figures 10 and 11. A simulation shows that BCB is advantageous for high-speed transmission.

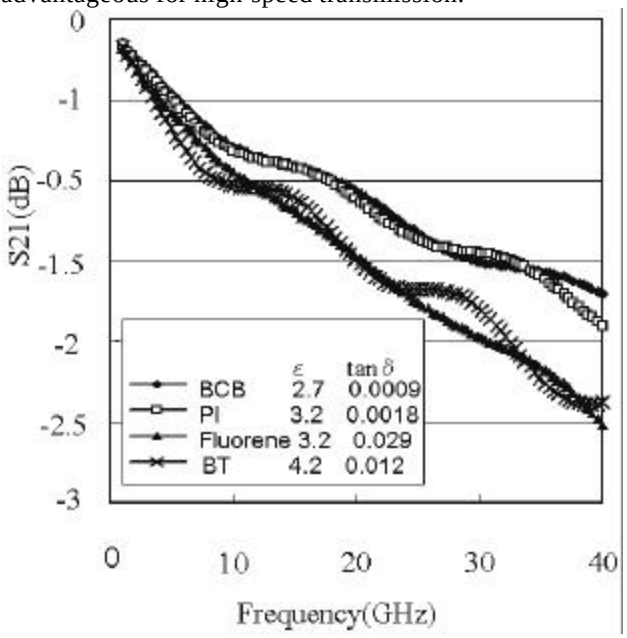

Figure 10 - Simulation Result of Transmission Characteristic 1

The High-Speed Transmission Characteristic

If the wiring pitch becomes fine, we will be anxious about the influence of contiguity wiring. The relation between a wiring pitch and a transmission characteristic was investigated. An HFSS simulator performed with various wiring pitches from 6μ m to 28μ m, with a three strip line structure with cover layer. When the pitch becomes small at 10μ m or less, it turns out that transmission loss becomes large due to the influence of contiguity wiring.

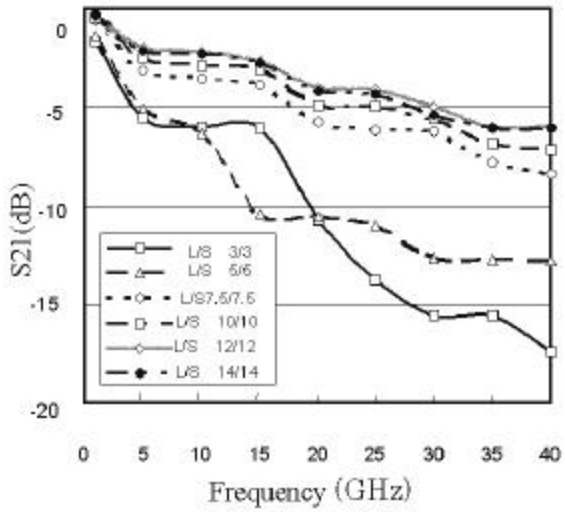

Figure 11 - Simulation Result of Transmission Characteristic 2

The TEG of a wiring layer was produced to measure S-parameter of a fine wiring layer. (See Figures 12 and 13.) The S-parameter was measured using an Agilent technology HP8722ES network analyzer. The measurement was carried out by using a wiring width of 11,8,6μ m, and 4μ m micro strip line structure, and 15mm of wiring length. (See Figure 14.) A result of the S-parameter measurement with micro strip line structure was a –3dB attenuation at 16GHz. This demonstrated excellent high frequency transmission characteristic.

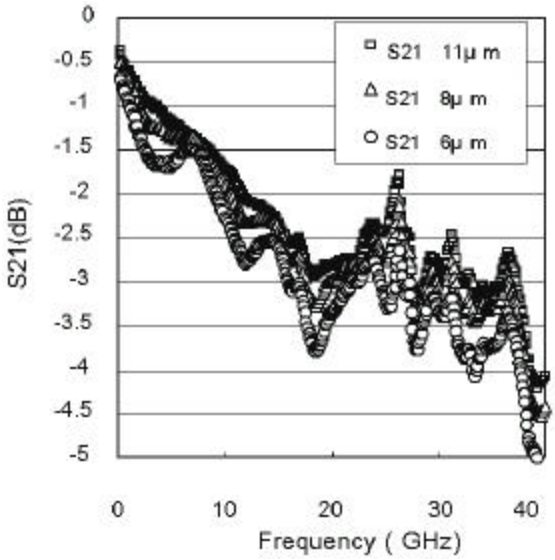

Figure 12 - Measurement Result of S-Parameter 1

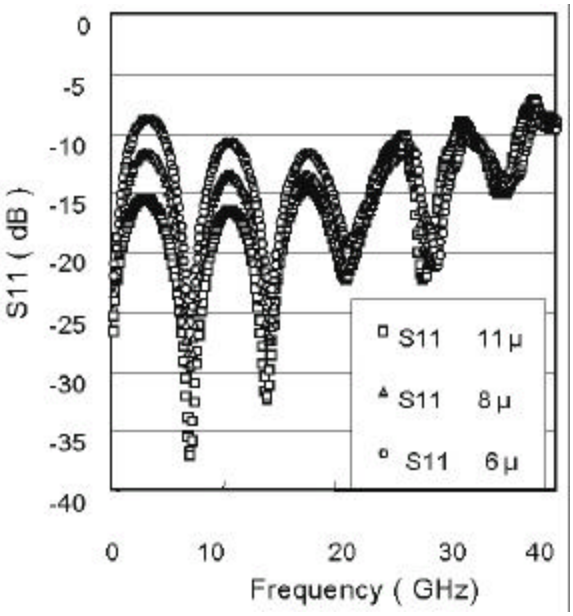

Figure 13 - Measurement Result of S-Parameter 2

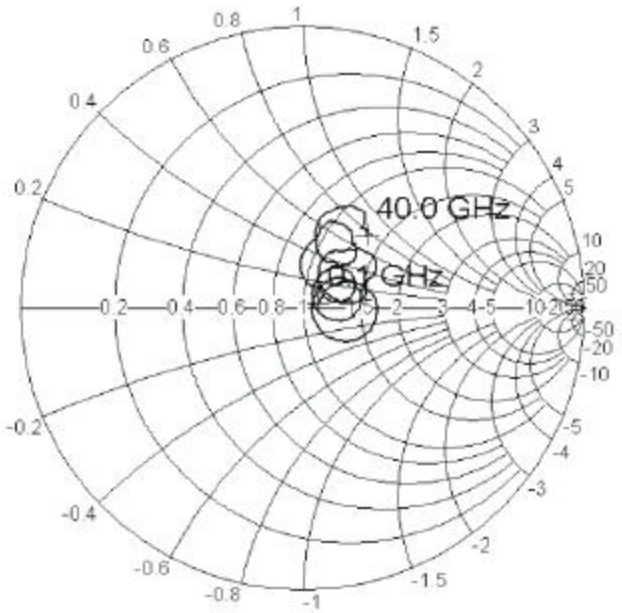

Figure 14 - Smith Chart of S11 8µ m

Summary

As a result of the fine wiring formation process' adopting BCB as the dielectric material and semi additives process with a sputtering method, very fine pitch Cu conductors on BCB were developed. The limitation of the minimum pitch was 10µ m
(L/S=6 /4).

Filled via process was possible for 20µ m via diameter on BCB.

An excellent high frequency transmission characteristic, a result of the S parameter with micro strip line structure, was –3dB at 16GHz.

Electromagnetic simulation was performed to research the dependence of the signal transmission characteristic on the pitch of fine lines. When the pitch became 10µ m or less, it turns out that transmission loss becomes large due to the influence of contiguity wiring.

From the above, as a optimal design rule of the fine wiring layer, a pitch of 15µ m (L/S=7.5 / 7.5), and 20µ m of diameters filled via are the optimal designs, with insulator thickness being 6.5µ m. The fine wiring technology was developed and designed for a high density and high-speed substrate using buried bump interconnection technology fine phase? .

Reference

1. International Technology Roadmap for Semiconductors; 2001edition.
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3. Y.Fukuoka: "High-Density Build-up Printed wiring Boards by the combined technology between thick and thin film technology ",Journal of Japan institute of electronics packaging, pp. 563-568, vol.3, No7, A,2000